SONY

Diagonal 8.8 mm (Type 1/1.8) CMOS solid-state Image Sensor with Square Pixel for Color Cameras

IMX548-AAQJ-C

Pregius S

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1. Description

The IMX548-AAQJ-C is a diagonal 8.8 mm (Type 1/1.8) CMOS active pixel type solid-state image sensor with a square pixel array and 5.10 M effective pixels. This chip features a global shutter with variable charge-integration time. This chip operates with analog 3.3 V, 2.9V, digital 1.1 V, and interface 1.8 V quadruple power supply. High sensitivity and low dark current characteristics are achieved.
(Applications: FA cameras, ITS cameras)

2. Features

- ◆CMOS active pixel type dots
- ◆Built-in timing adjustment circuit, H/V driver and serial communication circuit
- ◆Global shutter function
- ◆Input frequency 37.125 MHz / 74.25 MHz / 54 MHz
- ◆Number of recommended recording pixels: 2448 (H) × 2048 (V) approx. 5.01 M pixels
- ◆Readout mode
  All-pixel scan mode
  Vertical / Horizontal 1/2 Subsampling mode
  ROI mode
  Vertical / Horizontal - Normal / Inverted readout mode
- ◆Readout rate
  Maximum frame rate in

  All-pixel scan mode: 8 bit 114.8 frame/s, 10 bit 93.4 frame/s, 12 bit 84.0 frame/s
  (*) At high frame rates, control so as not to exceed Tj = +100 °C
- ◆Variable-speed shutter function (resolution 1 H units)
- ◆Pulse Output Function

  The monitor output for Exposure period (TOUT0)
  Programmable pulse output (TOUT1 and TOUT2)
- ◆8-bit / 10-bit / 12-bit A/D converter
- ◆CDS / PGA function
  0 dB to 24 dB: Analog Gain (0.1 dB step)
  24.1 dB to 48 dB: Analog Gain: 24 dB + Digital Gain: 0.1 dB to 24 dB (0.1 dB step)
- ◆I/O interface
  SLVS (2 ch / 4 ch / 8 ch switching) output
- ◆Recommended lens F number: 2.8 or more (Close side)

E21704

3. Device Structure

◆ CMOS image sensor

◆ Image size

Diagonal 8.8 mm (Type 1/1.8) Approx. 5.10 M pixels

◆ Total number of pixels

2472 (H) × 2128 (V) Approx. 5.26 M pixels

◆ Number of effective pixels

2472 (H) × 2064 (V) Approx. 5.10 M pixels

◆ Number of active pixels

2472 (H) × 2064 (V) Approx. 5.10 M pixels

◆ Number of recommended recording pixels

2448 (H) × 2048 (V) Approx. 5.01 M pixels

◆ Unit cell size

2.74 µm (H) × 2.74 µm (V)

◆ Optical black

Horizontal (H) direction: Front 0 pixels, rear 0 pixels
Vertical (V) direction: Front 64 pixels, rear 0 pixels

◆ Substrate material

Silicon

4. Absolute Maximum Ratings

Item	Symbol	Rating			Unit	Remarks
Supply voltage (Analog 3.3 V)	$AV_{DD}1$	-0.3	～	4.65	V	
Supply voltage (Analog 2.9 V)	$AV_{DD}2$	-0.3	～	4.65	V	
Supply voltage (Interface 1.8 V)	OV_{DD}	-0.3	～	4.65	V	
Supply voltage (Digital 1.1 V)	DV_{DD}	-0.3	～	1.65	V	
Input voltage	VI	-0.3	～	OV_{DD} + 0.3	V	Do not exceed 4.65 V
Output voltage	VO	-0.3	～	OV_{DD} + 0.3	V	Do not exceed 4.65 V
Operating temperature	Topr	-30	to	+75	˚C	High temperature side: Tj = +100°C *1
Storage temperature	Tstg	-40	to	+85	˚C	

*1 Please control not to exceed "Tj = + 100 °C" using the thermometer function built in the image sensor. For the thermometer function, refer to the application note of "Thermometer".

5. Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (Analog 3.3 V)	$AV_{DD}1$	3.15	3.3	3.45	V
Supply voltage (Analog 2.9 V)	$AV_{DD}2$	2.75	2.9	3.05	V
Supply voltage (Interface 1.8 V)	OV_{DD}	1.7	1.8	1.9	V
Supply voltage (Digital 1.1 V)	DV_{DD}	1.0	1.1	1.2	V
Performance guarantee temperature	Tspec	-10	–	+60	˚C

6. USE RESTRICTION NOTICE

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General-0.0.9

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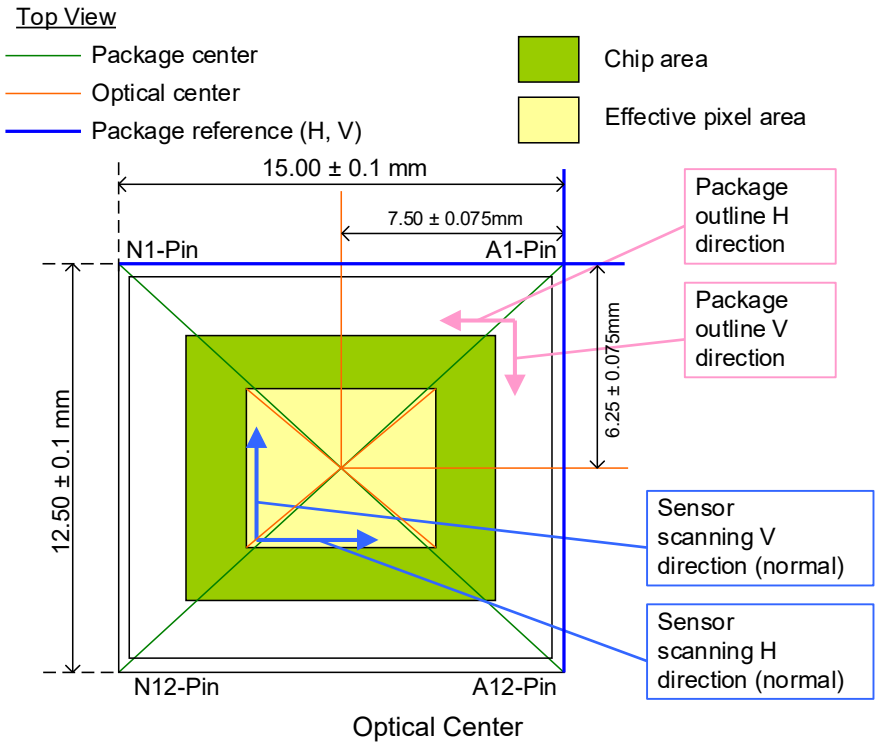
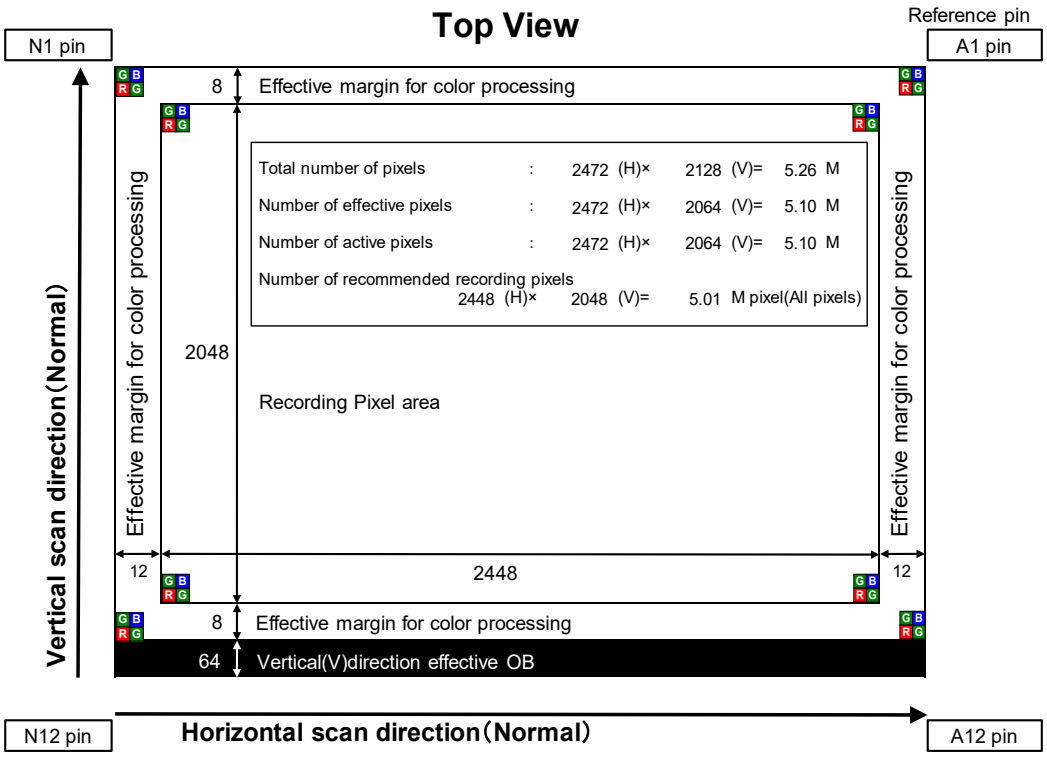
7. Chip Center and Optical Center



8. Pixel Arrangement

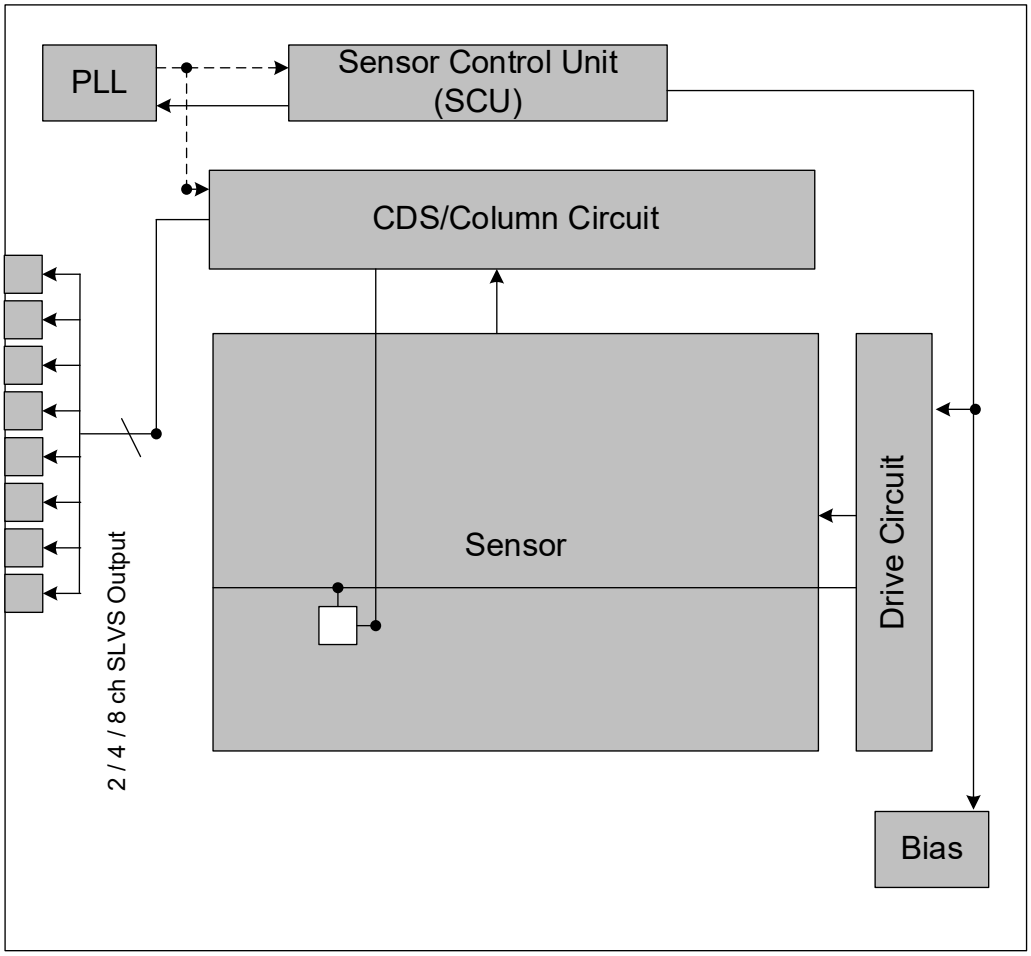


* Reference pin number is consecutive numbering of package pin array.
See the Pin Configuration for the number of each pin.

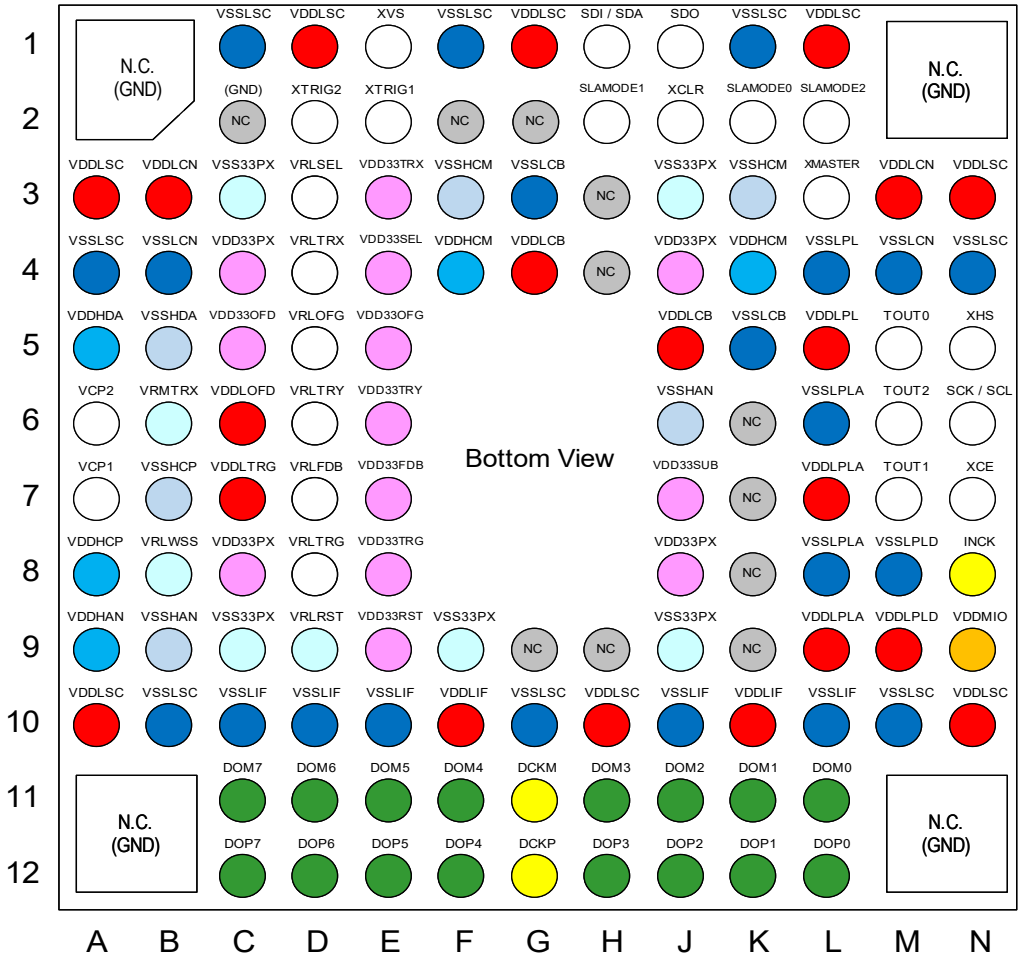
Pixel Arrangement

9. Block Diagram and Pin Configuration

(Top View)



Block Diagram



3.3 V Power Supply
2.9 V Power Supply
1.8 V Power Supply
1.1 V Power Supply
Clock
N.C.
3.3 V GND
2.9 V GND
1.8 V GND
1.1 V GND
Data output
Signal I/O

*The N.C. pin with (GND) can be connected to GND.

Pin Configuration

10. Pin Description

No.	Pin No.	I/O	Analog / Digital	Symbol	Description
1	A1	—	—	N.C.	GND connection is allowed
2	A3	Power	D	VDDLSC	1.1 V power supply
3	A4	GND	D	VSSLSC	1.1 V GND
4	A5	Power	A	VDDHDA	2.9 V power supply
5	A6	O	A	VCP2	Connect to VRLOFG, VRLSEL, VRLFDB, VRLTRX, VRLTRY (Connect 4.7 µF × 2 to GND)
6	A7	O	A	VCP1	Connect to VRLTRG(Connect 4.7 µF × 2 to GND)
7	A8	Power	A	VDDHCP	2.9 V power supply
8	A9	Power	A	VDDHAN	2.9 V power supply
9	A10	Power	D	VDDLSC	1.1 V power supply
10	A12	—	—	N.C.	GND connection is allowed
11	B3	Power	D	VDDLCN	1.1 V power supply
12	B4	GND	D	VSSLCN	1.1 V GND
13	B5	GND	A	VSSHDA	2.9 V GND
14	B6	GND	A	VRMTRX	3.3 V GND
15	B7	GND	A	VSSHCP	2.9 V GND
16	B8	GND	A	VRLWSS	3.3 V GND
17	B9	GND	A	VSSHAN	2.9 V GND
18	B10	GND	D	VSSLSC	1.1 V GND
19	C1	GND	D	VSSLSC	1.1 V GND
20	C2	—	—	N.C.	GND connection is allowed
21	C3	GND	A	VSS33PX	3.3 V GND
22	C4	Power	A	VDD33PX	3.3 V power supply
23	C5	Power	A	VDD33OFD	3.3 V power supply
24	C6	Power	A	VDDLOFD	1.1 V power supply
25	C7	Power	A	VDDLTRG	1.1 V power supply
26	C8	Power	A	VDD33PX	3.3 V power supply
27	C9	GND	A	VSS33PX	3.3 V GND
28	C10	GND	D	VSSLIF	1.1 V GND
29	C11	O	D	DOM7	SLVS IF output (Data)
30	C12	O	D	DOP7	SLVS IF output (Data)
31	D1	Power	D	VDDLSC	1.1 V power supply
32	D2	I	D	XTRIG2	Trigger input 2
33	D3	I	A	VRLSEL	Connect to VCP2
34	D4	I	A	VRLTRX	Connect to VCP2
35	D5	I	A	VRLOFG	Connect to VCP2
36	D6	I	A	VRLTRY	Connect to VCP2
37	D7	I	A	VRLFDB	Connect to VCP2
38	D8	I	A	VRLTRG	Connect to VCP1
39	D9	GND	A	VRLRST	3.3 V GND
40	D10	GND	D	VSSLIF	1.1 V GND
41	D11	O	D	DOM6	SLVS IF output (Data)
42	D12	O	D	DOP6	SLVS IF output (Data)
43	E1	I/O	D	XVS	Vertical sync signal
44	E2	I	D	XTRIG1	Trigger input 1
45	E3	Power	A	VDD33TRX	3.3 V power supply
46	E4	Power	A	VDD33SEL	3.3 V power supply
47	E5	Power	A	VDD33OFG	3.3 V power supply
48	E6	Power	A	VDD33TRY	3.3 V power supply
49	E7	Power	A	VDD33FDB	3.3 V power supply
50	E8	Power	A	VDD33TRG	3.3 V power supply
51	E9	Power	A	VDD33RST	3.3 V power supply
52	E10	GND	D	VSSLIF	1.1 V GND
53	E11	O	D	DOM5	SLVS IF output (Data)

No.	Pin No.	I/O	Analog / Digital	Symbol	Description
54	E12	O	D	DOP5	SLVS IF output (Data)
55	F1	GND	D	VSSLSC	1.1 V GND
56	F2	–	–	N.C.	–
57	F3	GND	A	VSSHCM	2.9 V GND
58	F4	Power	A	VDDHCM	2.9 V power supply
59	F9	GND	A	VSS33PX	3.3 V GND
60	F10	Power	D	VDDLIF	1.1 V power supply
61	F11	O	D	DOM4	SLVS IF output (Data)
62	F12	O	D	DOP4	SLVS IF output (Data)
63	G1	Power	D	VDDLSC	1.1 V power supply
64	G2	–	–	N.C.	–
65	G3	GND	A	VSSLCB	1.1 V GND
66	G4	Power	A	VDDLCB	1.1 V power supply
67	G9	–	–	N.C.	–
68	G10	GND	D	VSSLSC	1.1 V GND
69	G11	O	D	DCKM	Digital output timing clock
70	G12	O	D	DCKP	Digital output timing clock
71	H1	I/O	D	SDI / SDA	4-wire: Serial communication I/F SDI pin I^2C: Serial data line
72	H2	I	D	SLAMODE1	Slave address select
73	H3	–	–	N.C.	–
74	H4	–	–	N.C.	–
75	H9	–	–	N.C.	–
76	H10	Power	D	VDDLSC	1.1 V power supply
77	H11	O	D	DOM3	SLVS IF output (Data)
78	H12	O	D	DOP3	SLVS IF output (Data)
79	J1	O	D	SDO	4-wire: Serial communication I/F SDO pin I^2C: OPEN
80	J2	I	D	XCLR	System clear (Normal: High, Clear: Low)
81	J3	GND	A	VSS33PX	3.3 V GND
82	J4	Power	A	VDD33PX	3.3 V power supply
83	J5	Power	A	VDDLCB	1.1 V power supply
84	J6	GND	A	VSSHAN	2.9 V GND
85	J7	Power	A	VDD33SUB	3.3 V power supply
86	J8	Power	A	VDD33PX	3.3 V power supply
87	J9	GND	A	VSS33PX	3.3 V GND
88	J10	GND	D	VSSLIF	1.1 V GND
89	J11	O	D	DOM2	SLVS IF output (Data)
90	J12	O	D	DOP2	SLVS IF output (Data)
91	K1	GND	D	VSSLSC	1.1 V GND
92	K2	I	D	SLAMODE0	Slave address select
93	K3	GND	A	VSSHCM	2.9 V GND
94	K4	Power	A	VDDHCM	2.9 V power supply
95	K5	GND	A	VSSLCB	1.1 V GND
96	K6	–	–	N.C.	–
97	K7	–	–	N.C.	–
98	K8	–	–	N.C.	–
99	K9	–	–	N.C.	–
100	K10	Power	D	VDDLIF	1.1 V power supply
101	K11	O	D	DOM1	SLVS IF output (Data)
102	K12	O	D	DOP1	SLVS IF output (Data)
103	L1	Power	D	VDDLSC	1.1 V power supply
104	L2	I	D	SLAMODE2	Slave address select
105	L3	I	D	XMASTER	Master / Slave select (Slave Mode: High, Master Mode: Low)
106	L4	GND	D	VSSLPL	1.1 V GND
107	L5	Power	D	VDDLPL	1.1 V power supply
108	L6	GND	D	VSSLPLA	1.1 V GND

No.	Pin No.	I/O	Analog / Digital	Symbol	Description
109	L7	Power	D	VDDLPLA	1.1 V power supply
110	L8	GND	D	VSSLPLA	1.1 V GND
111	L9	Power	D	VDDLPLA	1.1 V power supply
112	L10	GND	D	VSSLIF	1.1 V GND
113	L11	O	D	DOM0	SLVS IF output (Data)
114	L12	O	D	DOP0	SLVS IF output (Data)
115	M3	Power	D	VDDLCN	1.1 V power supply
116	M4	GND	D	VSSLCN	1.1 V GND
117	M5	O	D	TOUT0	Pulse0 output pin
118	M6	O	D	TOUT2	Pulse2 output pin
119	M7	O	D	TOUT1	Pulse1 output pin
120	M8	GND	D	VSSLPLD	1.1 V GND
121	M9	Power	D	VDDLPLD	1.1 V power supply
122	M10	GND	D	VSSLSC	1.1 V GND
123	N1	–	–	N.C.	GND connection is allowed
124	N3	Power	D	VDDLSC	1.1 V power supply
125	N4	GND	D	VSSLSC	1.1 V GND
126	N5	I/O	D	XHS	Horizontal sync signal
127	N6	I	D	SCK / SCL	4-wire: Serial communication I/F SCK pin I^2C: Serial clock line
128	N7	I	D	XCE	4-wire: Serial communication I/F XCE pin I^2C: Fixed to High
129	N8	I	D	INCK	Master clock input
130	N9	Power	D	VDDMIO	1.8 V power supply
131	N10	Power	D	VDDLSC	1.1 V power supply
132	N12	–	–	N.C.	GND connection is allowed

* N.C. pins in the table above should be left open on the board.

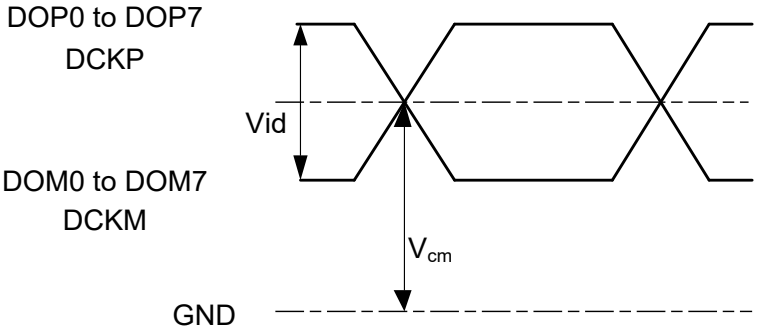
11. Electrical Characteristics

11.1. DC Characteristics

Item		Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Analog	V_{DD}33x	AV_{DD}1	—	3.15	3.3	3.45	V
	Analog	V_{DD}Hx	AV_{DD}2	—	2.75	2.9	3.05	V
	Digital	V_{DD}Mx	OV_{DD}	—	1.7	1.8	1.9	V
	Digital	V_{DD}Lx	DV_{DD}	—	1.0	1.1	1.2	V
Digital input voltage		XHS XVS XCLR INCK XMASTER SLAMODE0 SLAMODE1 SLAMODE2 SCK SDI XCE XTRIG1 XTRIG2	VIH	XVS / XHS in Slave mode	0.7 × OV_{DD}	—	—	V
			VIL		—	—	0.3 × OV_{DD}	V
Digital output voltage		XHS XVS SDO TOUT0 TOUT1 TOUT2	VOH	XVS / XHS in Master mode	OV_{DD} – 0.2	—	—	V
			VOL		—	—	0.2	V

11.1.1. SLVS Output DC Characteristics

Single end output



Definition of the characteristics of SLVS (Single end output)

Symbol	Item	Min.	Typ.	Max.	Unit	Remarks
Ro	Sensor output impedance	30	—	60	Ω	—
Vcm	Voltage center	150	—	250	mV	*1
|Vid|	Differential voltage	140	—	300	mV	*1

*1 Rin = 100Ω.

11.2. Power Consumption

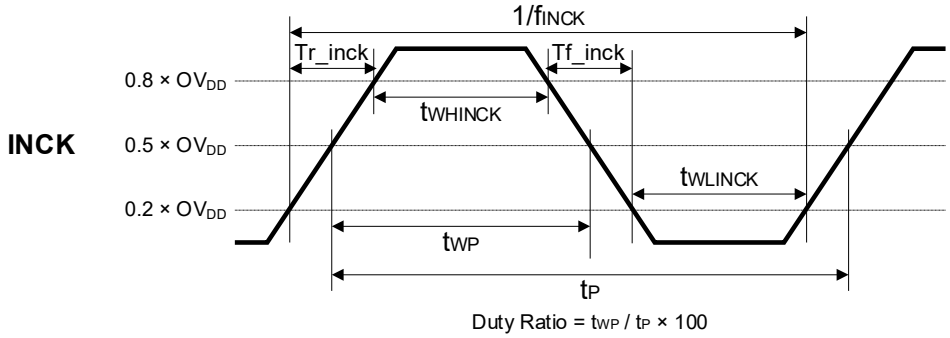
Item	Pins	Symbol	Typ.	Max.	Unit
Operating current SLVS 8 ch 12 bit 84.0 frame/s	$V_{DD}33$	$IAV_{DD}1$	28	45	mA
	$V_{DD}H$	$IAV_{DD}2$	79	125	mA
	$V_{DD}M$	IOV_{DD}	0.1	2	mA
	$V_{DD}L$	IDV_{DD}	166	285	mA
Standby current	$V_{DD}33$	$IAV_{DD}1$	—	0.1	mA
	$V_{DD}H$	$IAV_{DD}2$	—	0.1	mA
	$V_{DD}M$	IOV_{DD}_STB	—	0.05	mA
	$V_{DD}L$	IDV_{DD}_STB	—	200	mA

Operating current:
(Typical value condition) : Supply voltage: 3.3 V / 2.9 V / 1.8 V / 1.1 V, Tj = 25 ˚C
(Maximum value condition) : Supply voltage: 3.45 V / 3.05 V / 1.9 V / 1.2 V, Tj = 60 ˚C
Worst state of internal circuit operating current consumption.

Standby current:
(Maximum value condition) : Supply voltage: 3.45 V / 3.05 V / 1.9 V / 1.2 V, Tj = 60 ˚C, INCK = 0 V,
The device in the light-obstructed state.

11.3. AC Characteristics

11.3.1. Master Clock (INCK)

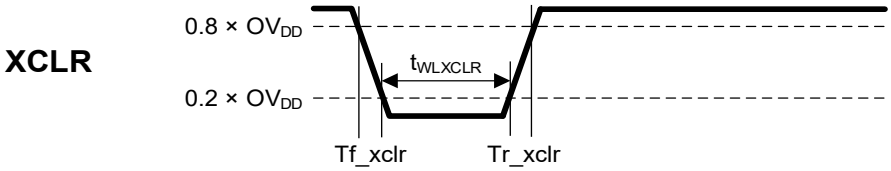


Duty Ratio = t_{WP} / t_P × 100

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	f_{INCK} × 0.96	f_{INCK}	f_{INCK} × 1.02	MHz	f_{INCK} = 37.125 MHz, 74.25 MHz, 54 MHz
INCK Low level pulse width	t_{WLINCK}	4	—	—	ns	
INCK High level pulse width	t_{WHINCK}	4	—	—	ns	
INCK clock duty	—	40.0	50.0	60.0	%	Define with 0.5 × OV_{DD}
INCK Rise time	Tr_inck	—	—	5	ns	20 % to 80 %
INCK Fall time	Tf_inck	—	—	5	ns	20 % to 80 %

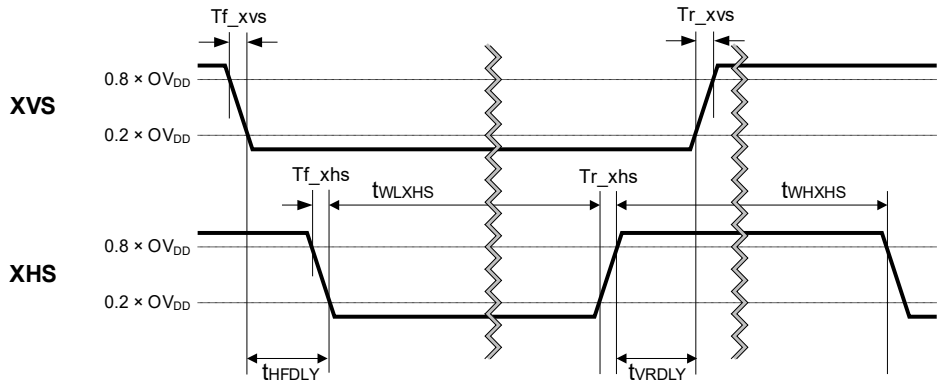
* The INCK fluctuation affects the frame rate.

11.3.2. System Clear (XCLR)



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XCLR Low level pulse width	t_{WLXCLR}	$4/f_{INCK}$	—	—	ns	f_{INCK} = 37.125 MHz, 74.25 MHz, 54 MHz
XCLR Fall time	Tf_xclr	—	—	5	ns	80 % to 20 %
XCLR Rise time	Tr_xclr	—	—	5	ns	20 % to 80 %

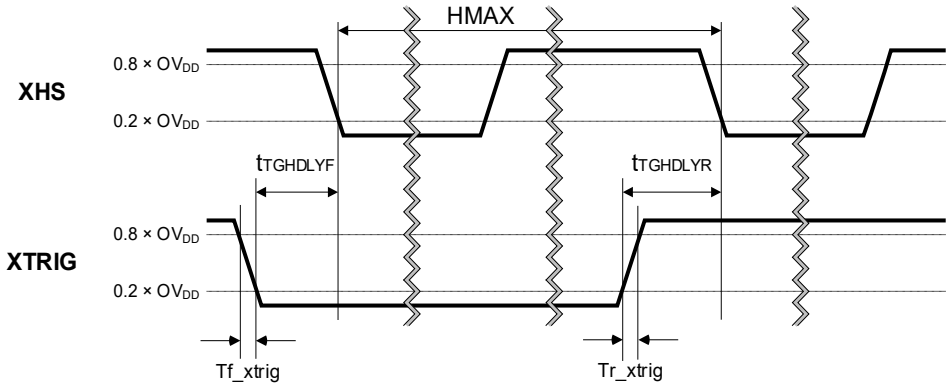
11.3.3. XVS / XHS Input Characteristics in Slave Mode (XMASTER = High)



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XHS Low level pulse width	t_{WLXHS}	$4/f_{INCK}$	—	—	ns	
XHS High level pulse width	t_{WHXHS}	$4/f_{INCK}$	—	—	ns	
XVS - XHS fall width	t_{HFDLY}	$1/f_{INCK}$	—	—	ns	
XHS - XVS rise width	t_{VRDLY}	$1/f_{INCK}$	—	—	ns	
XVS Fall time	Tf_xvs	—	—	5	ns	80 % to 20 %
XVS Rise time	Tr_xvs	—	—	5	ns	20 % to 80 %
XHS Fall time	Tf_xhs	—	—	5	ns	80 % to 20 %
XHS Rise time	Tr_xhs	—	—	5	ns	20 % to 80 %

Synchronization cannot be performed from XVS and XHS signal in mater mode. Detect the sync code.

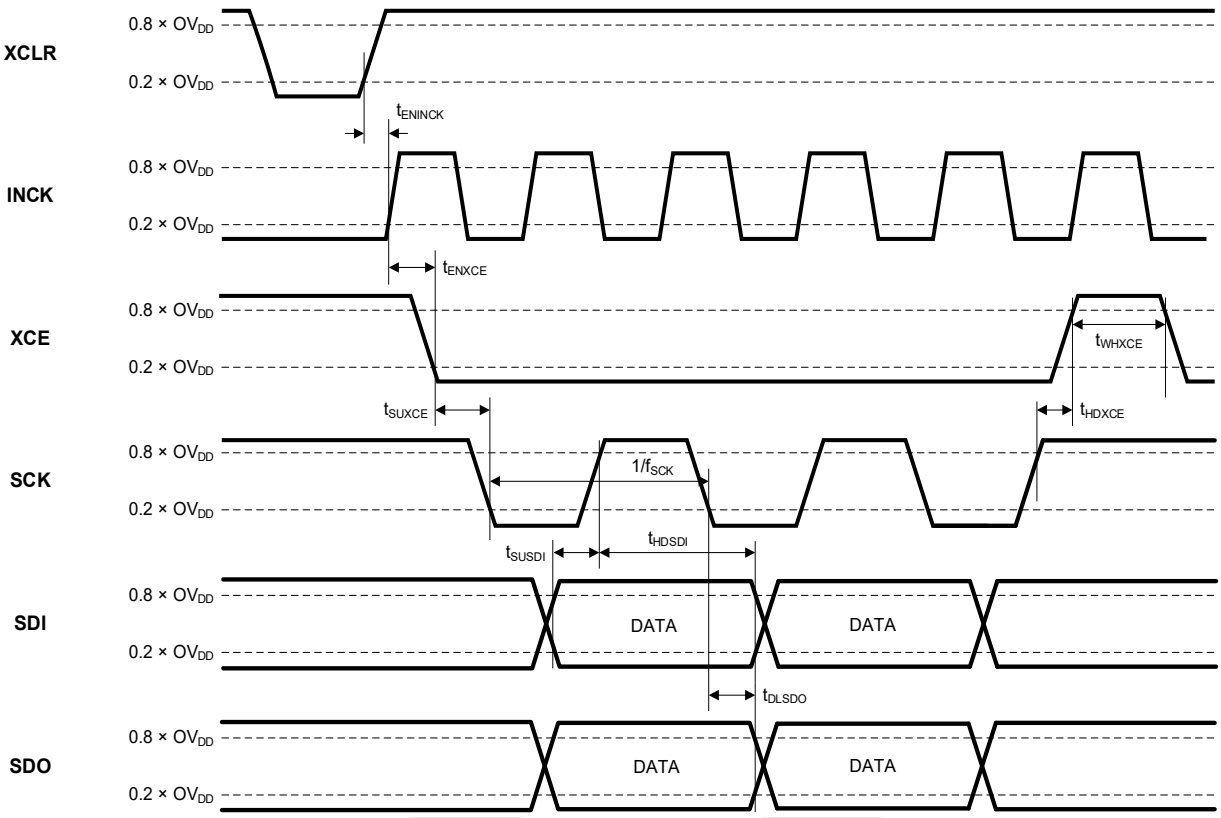
11.3.4. XTRIG Input Characteristics in Slave Mode (XMASTER = High) only



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XTRIG fall - XHS fall width	$t_{TGHDLYF}$	10	—	HMAX-10	INCK	
XTRIG rise - XHS fall width	$t_{TGHDLYR}$	10	—	HMAX-10	INCK	
XTRIG Fall time	Tf_xtrig	—	—	5	ns	80 % to 20 %
XTRIG Rise time	Tr_xtrig	—	—	5	ns	20 % to 80 %

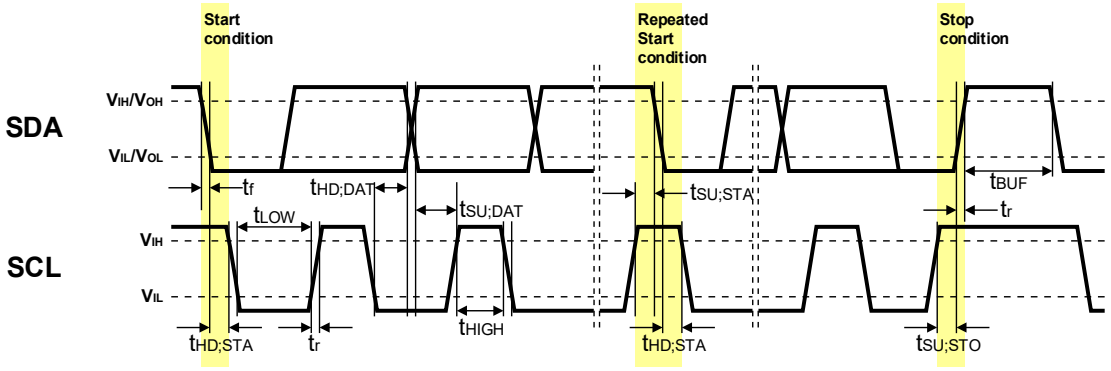
11.3.5. Serial Communication

4-wire



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCK clock frequency	f_{SCK}	—	—	13.5	MHz	
INCK effective margin	t_{ENINCK}	1	—	—	μs	
XCE effective margin	t_{ENXCE}	20	—	—	μs	
XCE input setup time	t_{SUXCE}	20	—	—	ns	
XCE input hold time	t_{HDXCE}	20	—	—	ns	
XCE High level pulse width	t_{WHXCE}	20	—	—	ns	
SDI input setup time	t_{SUSDI}	10	—	—	ns	
SDI input hold time	t_{HDSDI}	10	—	—	ns	
SDO output delay time	t_{DLSDO}	0	—	25	ns	Output load capacitance: 20 pF

I²C



I²C Specification

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Low level input voltage	V_{IL}	-0.3	—	0.3 × OV_{DD}	V	
High level input voltage	V_{IH}	0.7 × OV_{DD}	—	1.9	V	
Low level output voltage	V_{OL}	0	—	0.2 × OV_{DD}	V	OV_{DD} < 2 V, Sink 3 mA
High level output voltage	V_{OH}	0.8 × OV_{DD}	—	—	V	
Output fall time from VI_{Hmin} to V_{ILmax}	tof	—	—	250	ns	Load 10 pF – 400 pF, 0.7 × OV_{DD} – 0.3 × OV_{DD}
Input current	Ii	-10	—	10	µA	0.1 × OV_{DD} – 0.9 × OV_{DD}
Capacitance for SCK (/SCL) , SDI (/SDA)	Ci	—	—	10	pF	

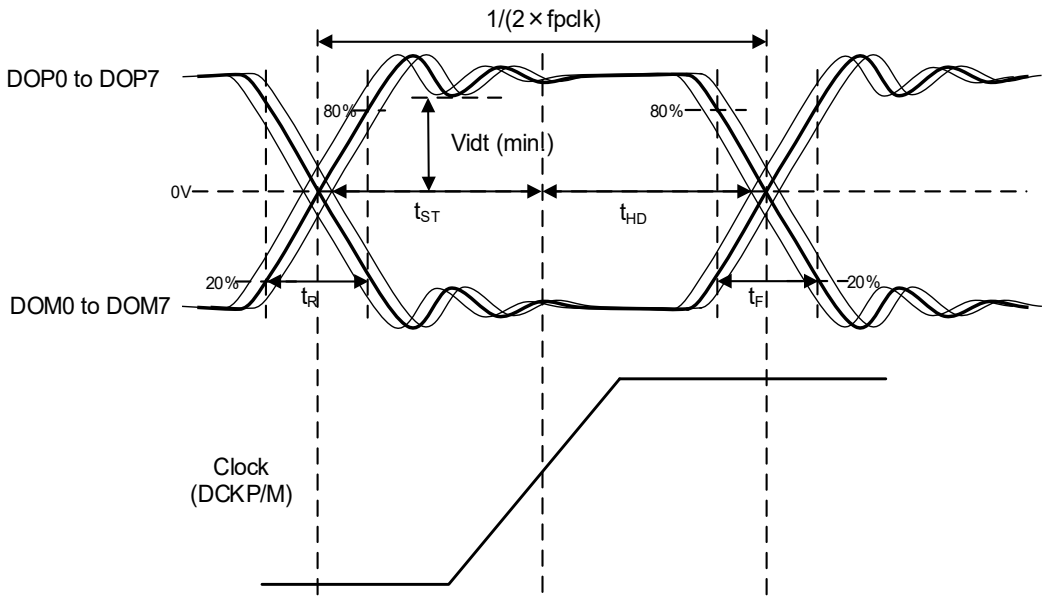
I²C AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	400	kHz
Hold time (Start Condition)	t_{HDSTA}	0.6	—	—	µs
Low period of the SCL clock	t_{LOW}	1.3	—	—	µs
High period of the SCL clock	t_{HIGH}	0.6	—	—	µs
Set-up time (Repeated Start Condition)	t_{SUSTA}	0.6	—	—	µs
Data hold time	t_{HDDAT}	0	—	0.9	µs
Data set-up time	t_{SUDAT}	100	—	—	ns
Rise time of both SDA and SCL signals	t_R	—	—	300	ns
Fall time of both SDA and SCL signals	t_F	—	—	300	ns
Set-up time (Stop Condition)	t_{SUSTO}	0.6	—	—	µs
Bus free time between a Stop and Start Condition	t_{BUF}	1.3	—	—	µs

11.3.6. SLVS Output AC Characteristics

Symbol	Item	Min.	Typ.	Max.	Unit	Remarks
f_{clk}	Output frequency	—	891	—	Mbps	—
f_{pclk}	Clock frequency	—	445.5	—	MHz	—
t_{ST}	Setup time	300	—	—	ps	*1
t_{HD}	Hold time	300	—	—	ps	*1
t_R	DOP/DOM rise time	—	—	300	ps	*1, *2
t_F	DOP/DOM fall time	—	—	300	ps	*1, *2
|Vidt|	Differential voltage	140	—	—	mV	*1

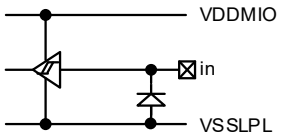
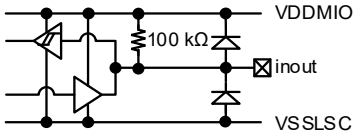
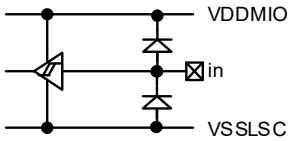
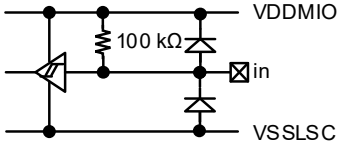
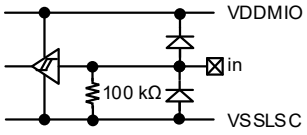
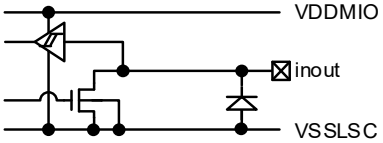
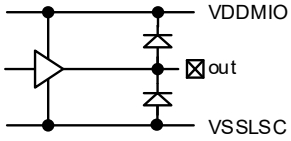
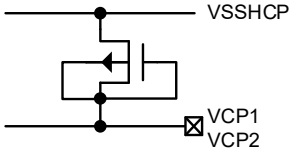
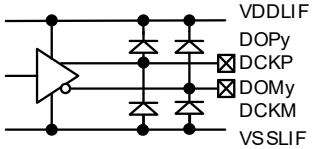
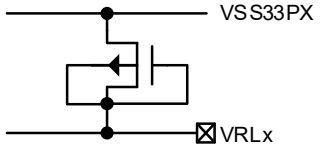
*1 Rin = 100Ω
*2 Differential 20% - 80%



Define of the characteristics of the SLVS

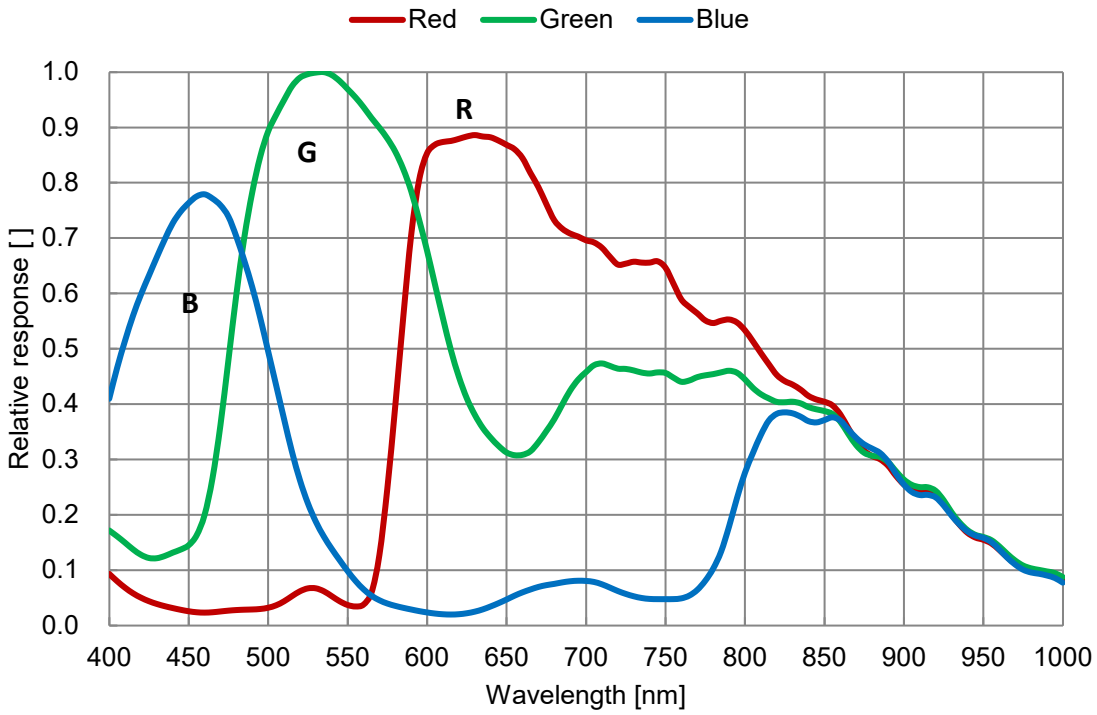
12. I/O Equivalent Circuit Diagram

□ : External pin

Symbol	Equivalent circuit	Symbol	Equivalent circuit
INCK		XVS XHS	
XCLR XCE XMASTER		XTRIG1, 2	
SLAMODE 0, 1, 2		SDI / SDA SCK / SCL	
SDO		VCP1 VCP2	
DOPy DOMy DCKP DCKM y : 0 to 7		VRLFDB VRLOFG VRLSEL VRLTRG VRLTRX VRLTRY	 VRLx: VRLFDB, VRLOFG, VRLSEL, VRLTRG, VRLTRX and VRLTRY

13. Spectral Sensitivity Characteristics

(Characteristics in the wafer status)



14. Image Sensor Characteristics

($AV_{DD}1$ = 3.3 V, $AV_{DD}2$ = 2.9 V, OV_{DD} = 1.8 V, DV_{DD} = 1.1 V, All-pixel scan mode, AD: 12 bit, Tj = 60 ˚C, Gain = 0 dB)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity		S	7327 (1337)	8620 (1574)	—	Digit/lx/s (mV/lx/s)	1	12 bit converted value
Sensitivity ratio	R / G	RG	0.36	—	0.51	—	2	
	B / G	BG	0.26	—	0.41	—		
Saturation signal		Vsat2D	4094 (748[*1])	—	—	Digit (mV)	3	
Video signal shading		SH01	—	—	20	%	4	
		SH2D	—	—	25	%		
Dark signal		Vdt	—	—	0.82 (0.15)	Digit (mV)	5	1/30 s storage
Dark signal shading		ΔVdt	—	—	1.37 (0.25)	Digit (mV)	6	1/30 s storage
PLS (Parasitic Light Sensitivity)		Sm	—	—	-72	dB	7	

Note) 1. Converted value into mV using 1Digit = 0.1826 mV for 12-bit output, 1Digit = 0.7304 mV for 10-bit output and 1Digit = 0.7304 mV for 8-bit output.
2. The video signal shading is the measured value in the wafer status and does not include characteristics of the seal glass.

[*1] In case of 8 bit, Vsat2D becomes 1/4 of it at 12 bit.

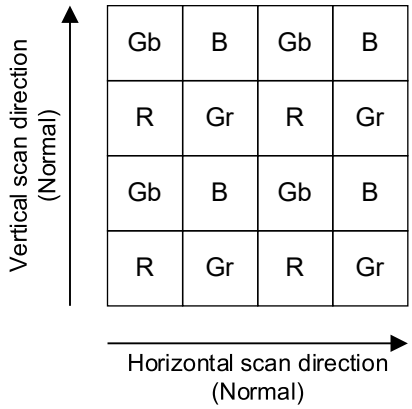
15. Image Sensor Characteristics Measurement Method

15.1. Measurement Conditions

In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the signal output of the measurement system.

15.2. Color Coding of Physical Pixel Array

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb represent the G signal on the same line as the R and B signals, respectively. The R signal and Gr signal lines and the Gb signal and B signal lines are output successively.



Color Coding Diagram

15.3. Definition of standard imaging conditions

◆ Standard imaging condition I:
Using a purple excitation LED light source with a color temperature of 2850 K, an IR cut filter CM700 (t = 1.0 mm) is placed between the LED light source and the sensor receiving surface to irradiate substantially parallel light.

◆ Standard image condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM700 (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard image condition III:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens (exit pupil distance -100 mm) with CM700 (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

15.4. Measurement Method

(1) Sensitivity
Set the measurement condition to the standard imaging condition I, and calculate using the illuminance (Ev) of the sensor receiving surface, the signal values (VGr, VGb, VR, VB) at the center of the screen, and the integration time (T).

VG = (VGr + VGb) / 2
Sg = VG / (Ev × T) [Digit/lx/s]

(2) Sensitivity ratio
By Using the R and B signal outputs (VR, VB) obtained from the sensitivity measurement, substitute the values into the following formulas.

RG = VR / VG
BG = VB / VG

(3) Saturation signal
Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr and Gb signal outputs, 562 mV, measure the minimum values of the Gr, Gb, R and B signal outputs.

(4) Video signal shading
Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs are 562 mV. Then measure the maximum value (Gmax [mV]) and the minimum value (Gmin [mV]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

SH = (Gmax – Gmin) / 562 × 100 [%]

(5) Dark signal
With the device junction temperature of 60 ˚C and the device in the light-obstructed state, divide the output difference between 1/3 s integration at 3 frame/s and 1/30 s integration at 30 frame/s by 9, and calculate the signal output converted to 1/30 s integration. Measure the average value of this output (Vdt [mV]).

(6) Dark signal shading
Measure the maximum value (Vdmax [mV]) and the minimum value (Vdmin [mV]) of the dark signal output with the device junction temperature of 60 ˚C and the device in the light-obstructed state and 1/30 s integration. The measuring values substitute into the following formula.

ΔVdt = Vdmax – Vdmin [mV]

(7) PLS
Set the measurement condition to the standard imaging condition II, the Gr and Gb output signal Vave measured by standard image condition. Then, adjust the luminous intensity to 500 times the intensity with average value of the Gr and Gb signal output, Vave. When the charge drain is executed be the electronic shutter and the condition that not be readout from photo diode to analog memory, readout by dropping to 30 frame/s.

Sm = 20 × log ((Vsm / Vave) × (1 / 500) × (10 / 33.3)) [dB]

16. Setting Registers Using Serial Communication

This sensor can write and read the setting values of the various registers shown in the Register Map by 4-wire serial communication and I^2C communication. See the Register Map for the addresses and setting values to be set. Because the two communication systems are judged at the first communication, once they are judged, the communication cannot be switched until sensor reset. The pin for 4-wire serial communication and I^2C communication is shared, so the external pin XCE must be fixed to power supply side when using I^2C communication.

16.1. Description of Setting Registers (4-wire)

The serial data input order is LSB-first transfer. The table below shows the various data types and descriptions.

Serial Data Transfer Order

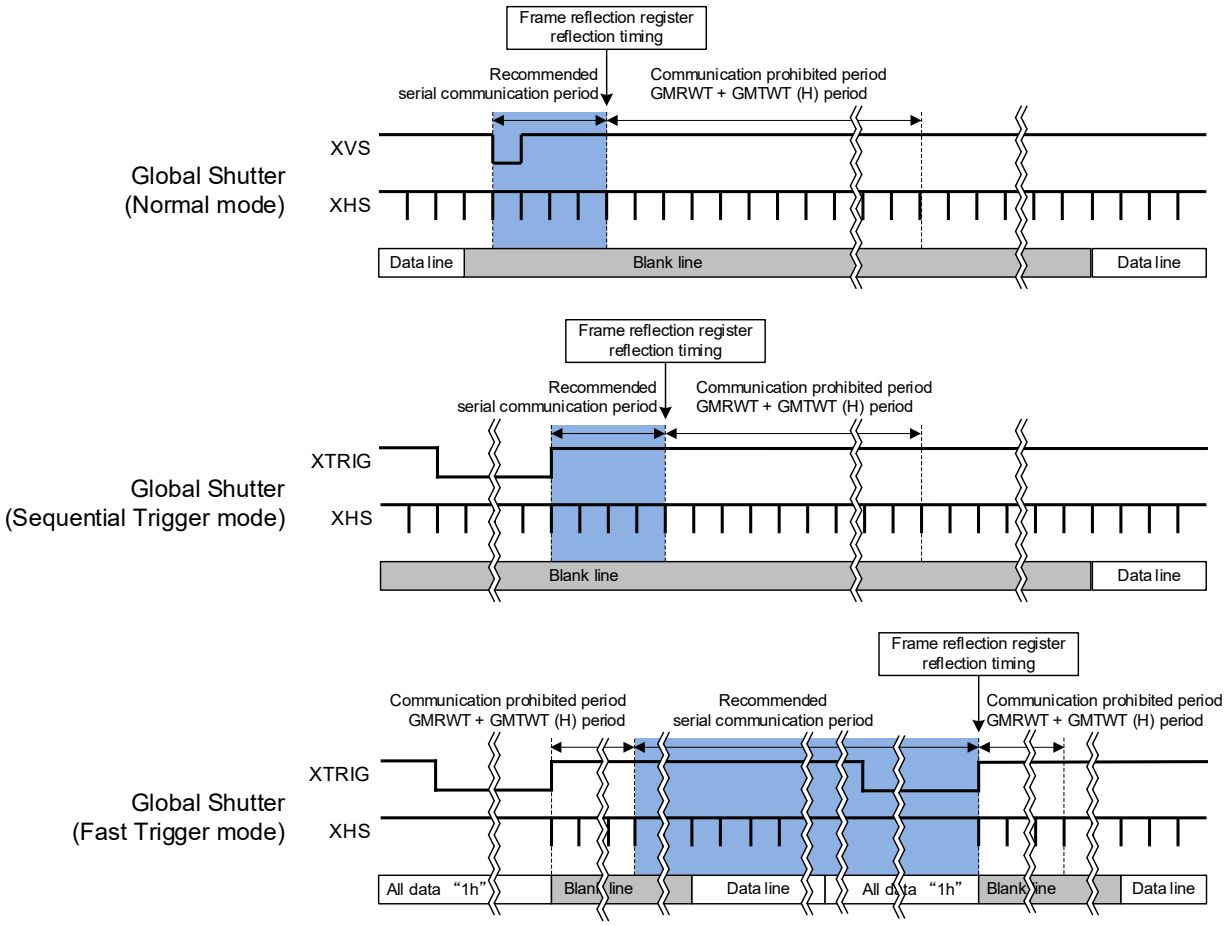
Chip ID	Start address	Data	Data	Data	…
(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)

Type and Description

Type	Description
Chip ID	Chip ID: 02 Write: 02h / Read: 82h
	Chip ID: 03 Write: 03h / Read: 83h
	Chip ID: 04 Write: 04h / Read: 84h
	Chip ID: 05 Write: 05h / Read: 85h
	Chip ID: 06 Write: 06h / Read: 86h
	Chip ID: 07 Write: 07h / Read: 87h
	Chip ID: 08 Write: 08h / Read: 88h
	Chip ID: 09 Write: 09h / Read: 89h
	Chip ID: 0A Write: 0Ah / Read: 8Ah
	Chip ID: 0B Write: 0Bh / Read: 8Bh
	Chip ID: 0C Write: 0Ch / Read: 8Ch
	Chip ID: 0D Write: 0Dh / Read: 8Dh
	Chip ID: 10 Write: 10h / Read: 90h
	Chip ID: 11 Write: 11h / Read: 91h
	Chip ID: 12 Write: 12h / Read: 92h
	Chip ID: 13 Write: 13h / Read: 93h
	Chip ID: 14 Write: 14h / Read: 94h
	Chip ID: 15 Write: 15h / Read: 95h
	Chip ID: 16 Write: 16h / Read: 96h
	Chip ID: 17 Write: 17h / Read: 97h
	Chip ID: 18 Write: 18h / Read: 98h
	Chip ID: 19 Write: 19h / Read: 99h
	Chip ID: 1A Write: 1Ah / Read: 9Ah
	Chip ID: 1B Write: 1Bh / Read: 9Bh
	Chip ID: 1C Write: 1Ch / Read: 9Ch
	Chip ID: 1E Write: 1Eh / Read: 9Eh
Address	Designate the address according to the Register Map. When using a communication method that designates continuous addresses, the address is automatically incremented from the previously transmitted address.
Data	Input the setting values according to the Register Map.

16.2. Register Communication Timing (4-wire)

Perform serial communication in sensor standby mode or within communication period. For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by frame reflection timing. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed.
For GMRWT and GMTWT, refer to the register list of each readout mode.



Communication Timing and Register Reflection Timing

16.3. Register Write and Read (4-wire)

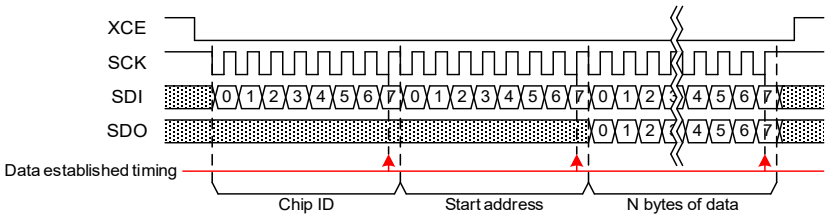
◆ Follow the communication procedure below when writing registers.

(1) Set XCE Low to enable the chip's communication function. Serial data input is executed using SCK and SDI.
(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
(3) Input the Chip ID (CID = 02h to 0Dh, 10h to 1Ch, 1Eh) to the first byte. If the Chip ID differs, subsequent data is ignored.
(4) Input the start address to the second byte. The address is automatically incremented.
(5) Input the data to the third and subsequent bytes. The data in the third byte is written to the register address designated by the second byte, and the register address is automatically incremented thereafter when writing the data for the fourth and subsequent bytes. Normal register data is loaded to the inside of the sensor and established in 8-bit units.
(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The register values before the write operation are output. The actual register values are the input data.
(7) Set XCE High to end communication.

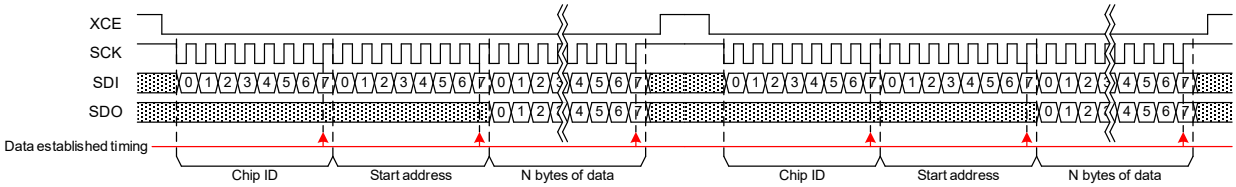
◆ Follow the communication procedure below when reading registers.

(1) Set XCE Low to enable the chip's communication function. Serial data input is executed using SCK and SDI.
(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
(3) Input Chip ID (CID = 82h to 8Dh, 90h to 9Ch, 9Eh) to the first byte. If the Chip ID differs, subsequent data is ignored.
(4) Input the start address to the second byte. The address is automatically incremented.
(5) Input data to the third and subsequent bytes. Input dummy data in order to read the registers. The dummy data is not written to the registers. To read continuous data, input the necessary number of bytes of dummy data.
(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The input data is not written, so the actual register values are output.
(7) Set XCE High to end communication.

Note) When writing data to multiple registers with discontinuous addresses, access to undesired registers can be avoided by repeating the above procedure multiple times.



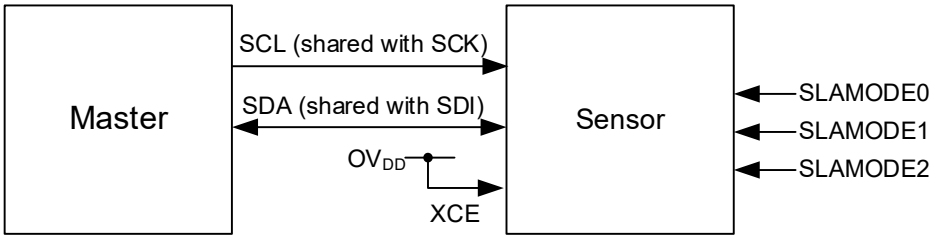
Serial Communication (Continuous Addresses)



Serial Communication (Discontinuous Addresses)

16.4. Description of Setting Registers (I^2C)

The serial data input order is MSB-first transfer. The table below shows the various data types and descriptions.



Pin connection of serial communication

The sensor can use two kinds of slave addresses by switching the polarity of SLAMODE0, SLAMODE1 and SLAMODE2 Pins for one I^2C bus, and can use a common slave address in both polarities of SLAMODE [2:0] Pins for one I^2C bus.

1st SLAVE Address (SLAMODE [2:0])

SLAMODE [2:0]	MSB							LSB
0h	0	1	1	0	1	1	0	R / W
1h	0	1	1	0	1	1	1	R / W
2h	0	1	1	1	0	0	0	R / W
3h	0	1	1	1	0	0	1	R / W
4h	0	1	1	1	0	1	0	R / W
5h	0	1	1	1	0	1	1	R / W
6h	0	1	1	1	1	0	0	R / W
7h	0	1	1	1	1	0	1	R / W

2nd SLAVE Address (Common in all SLAMODE [2:0])

MSB							LSB
0	0	1	1	0	1	0	R / W

* R/W is data direction bit

R/W

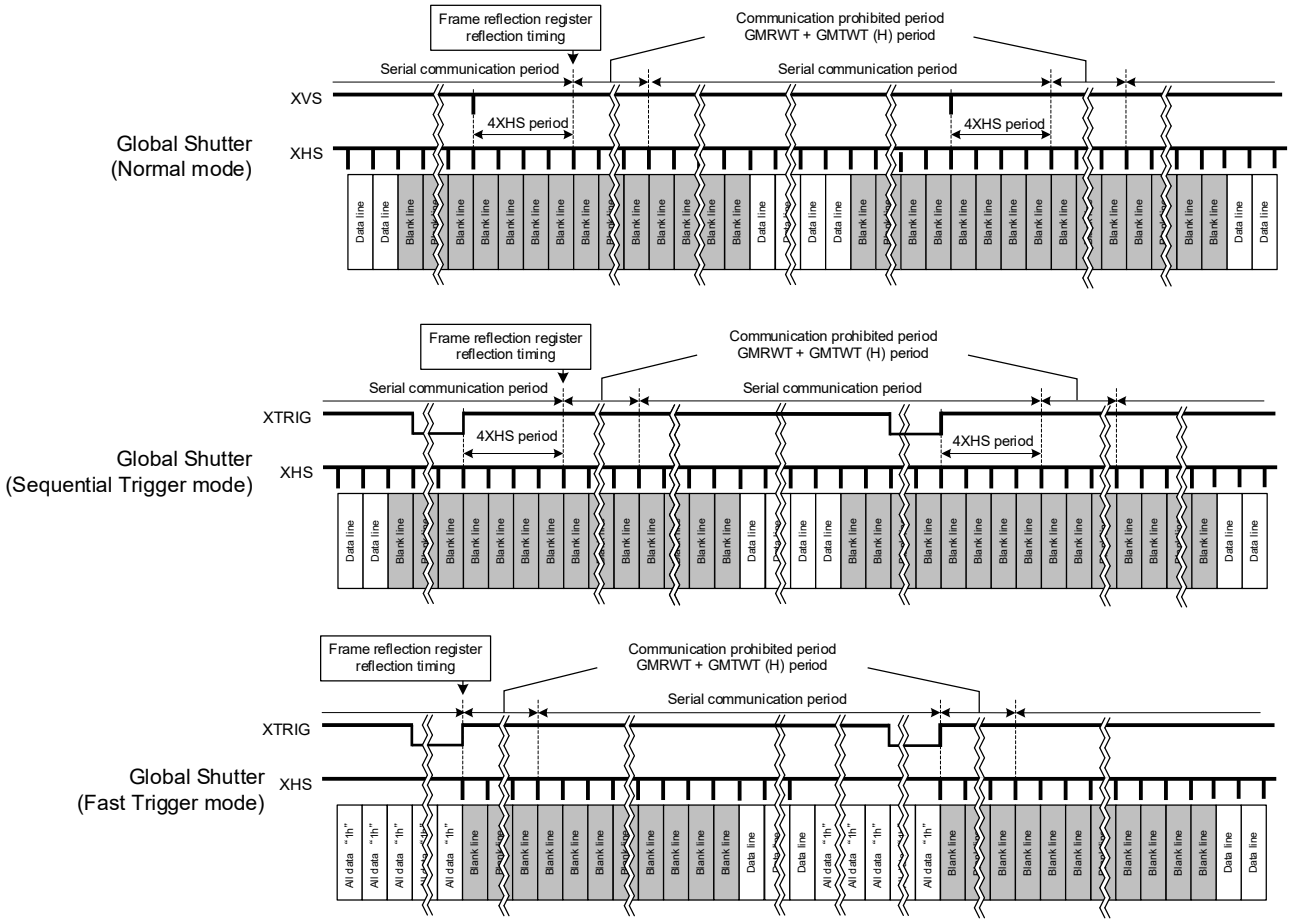
R / W bit	Data direction
0	Write (Master → Sensor)
1	Read (Sensor → Master)

I^2C pin description

Symbol	Pin No.	Description
SCL (common to SCK)	N6	Serial clock input
SDA (common to SDI)	H1	Serial data communication
SLAMODE0	K2	I^2C 1st Slave address select
SLAMODE1	H2	I^2C 1st Slave address select
SLAMODE2	L2	I^2C 1st Slave address select
XCE	N7	Fixed to High when using I^2C

16.5. Register Communication Timing (I²C)

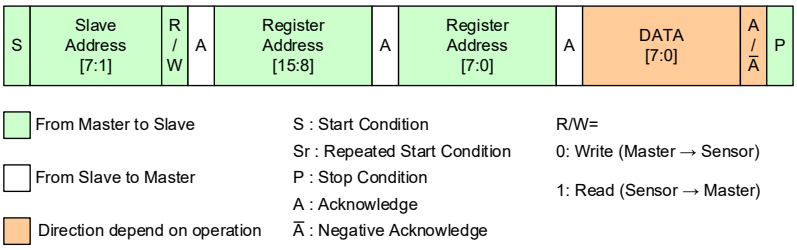
In I²C communication system, communication can be performed during the period excluding the communication prohibited period (GMRWT + GMTWT (H) period) shown below.
The registers whose reflection timing is “V” in the register map are reflected by the “Frame reflection register reflection timing” when communication is performed during the communication period shown in the figure below.
Registers whose reflection timing is “I” (Immediately) are reflected when the communication is performed.
Using REGHOLD function is recommended for register setting using I²C communication. For REGHOLD function, see section “Register Hold Setting” in chapter “Description of Various Functions”.
For GMRWT and GMTWT, see the register list of each readout mode in chapter “Readout Drive Modes”.



Communication Timing and Register Reflection Timing

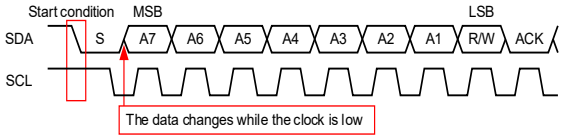
16.6. I²C Communication Protocol

I²C serial communication supports a 16-bit register address and 8-bit data message type.

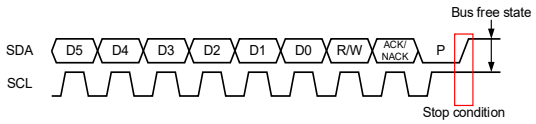


Communication protocol

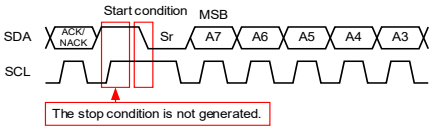
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) / Ā (Negative Acknowledge) is transferred. Data (SDA) is transferred at the clock (SCL) cycle. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start Condition is defined by SDA changing from High to Low while SCL is High. When the Stop Condition is not generated in the previous communication phase and Start Condition for the next communication is generated, that Start Condition is recognized as a Repeated Start Condition.



Start Condition

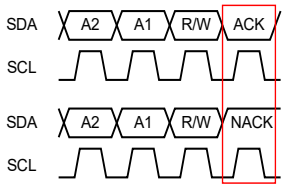


Stop Condition



Repeated Start Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge / Negative Acknowledge and release (does not drive) SDA. When Negative Acknowledge is generated, the Master must immediately generate the Stop Condition and end the communication.



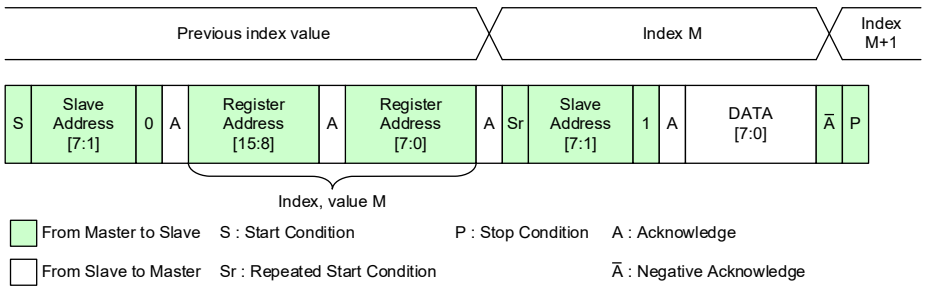
Acknowledge and Negative Acknowledge

16.7. I²C Serial Communication Read/Write Operation

This sensor supports the following four read operations and two write operations.

16.7.1. Single Read from Random Location

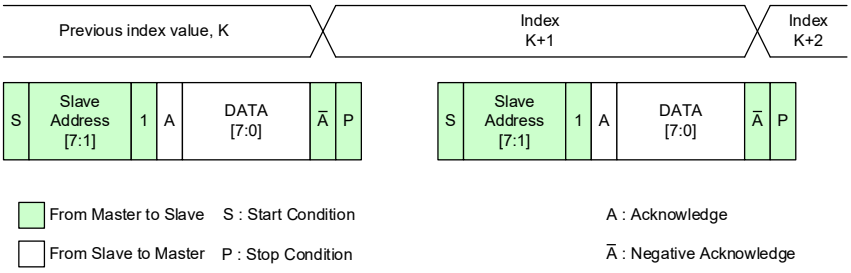
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the Start Condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop Condition to end the communication.



Single Read from Random Location

16.7.2. Single Read from Current Location

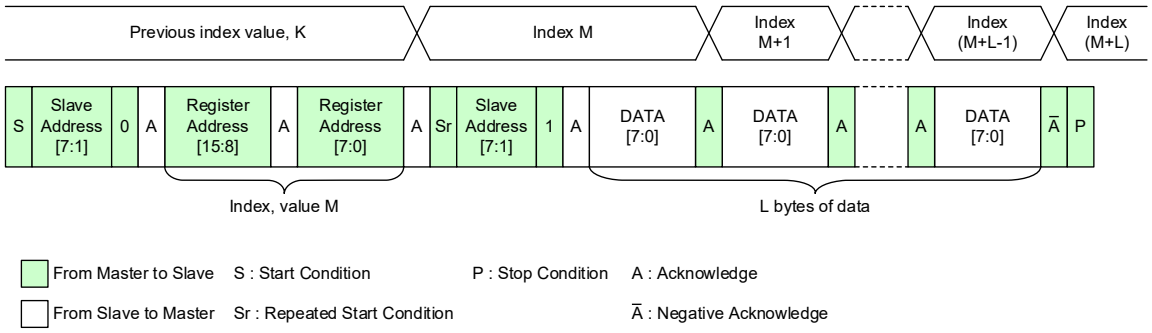
After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read/write is performed, the index is incremented by the subsequent Acknowledge/Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.



Single Read from Current Location

16.7.3. Sequential Read Starting from Random Location

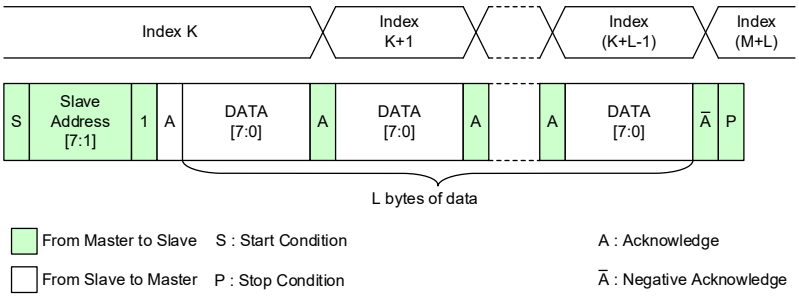
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Random Location

16.7.4. Sequential Read Starting from Current Location

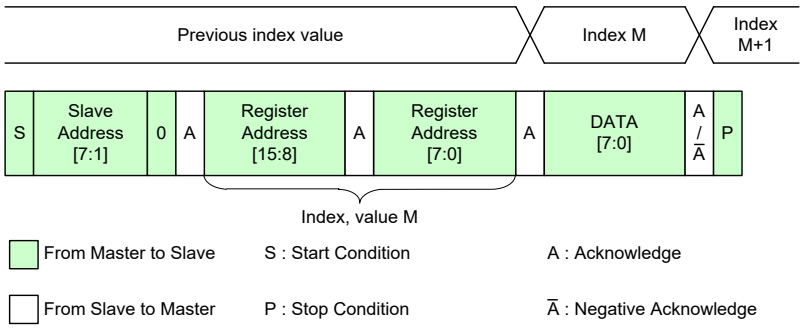
When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Current Location

16.7.5. Single Write to Random Location

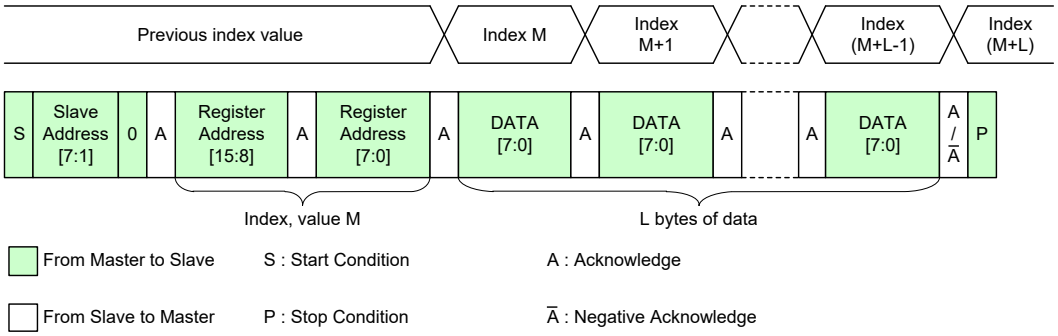
The Master sets the sensor index value to M by designating the sensor slave address with a write request, and designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop Condition to end the communication.



Single Write to Random Location

16.7.6. Sequential Write Starting from Random Location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop Condition to end the communication.



Sequential Write Starting from Random Location

17. Register Map

This sensor has a total of 6656 bytes of registers, composed of registers with address 00h to FFh that correspond to Chip ID = 02h to 0Dh, 10h to 1Ch, 1Fh. Use the initial values for empty address. Some registers must be change from the initial values, so the sensor control side should be capable of setting 6656 bytes.

There are three different register reflection timings.
About the Reflection timing column of the Register Map, registers noted as "I" are reflected immediately after writing to register, registers noted as "S" are set during standby mode and reflected after standby canceled, registers noted as "V" are reflected at “Fame reflection register reflection timing” on the figure described in the section of “Setting Registers Using Serial Communication”.

Do not perform communication to addresses and setting not listed in the Register Map. Doing so may result in operation errors. However, other registers that requires communication to address not listed may be added, so addresses 00h to FFh should be supported for Chip ID = 02h to 0Dh, 10h to 1Ch, 1Eh (In I^2C communication, address; 3000h to 3BFFh, 3E00h to 4AFFh, 4C00h to 4CFFh)

17.1. Chip ID = 02 (Write: Chip ID = 02h, Read: Chip ID = 82h, I²C: 30**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
00h	3000h	0	STANDBY [0]	Standby mode 0: Normal operation 1: Standby	1	01h	I
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
10h	3010h	0	XMSTA [0]	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop	1	01h	I
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
14h	3014h	0	INCKSEL_ST0 [7:0]	Set according to INCK frequency and drive mode.	0Ah	0Ah	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
15h	3015h	0	INCKSEL_ST1 [7:0]	Set according to INCK frequency and drive mode.	22h	22h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
16h	3016h	0	INCKSEL_ST2 [7:0]	Set according to INCK frequency and drive mode.	B1h	B1h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
18h	3018h	0	INCKSEL_ST3 [7:0]	Set according to INCK frequency and drive mode.	40h	40h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
19h	3019h	0	INCKSEL_ST4 [7:0]	Set according to INCK frequency and drive mode.	04h	04h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
1Bh	301Bh	0	INCKSEL_ST5 [7:0]	Set according to INCK frequency and drive mode.	3Ah	3Ah	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
34h	3034h	0	REGHOLD [0]	Register hold 0: Invalid 1: Valid	0	00h	I
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
3Ch	303Ch	0		Fixed to 0	0	00h	—
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3	HVMODE [1:0]	Drive mode setting of H/V direction 0h: All-pixel 1h: 1/2 Subsampling mode Other: Setting prohibited	0h		S
		4					
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
D0h	30D0h	0	VOPB_VBLK_HWIDTH [12:0]	LSB	09A8h	A8h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7		VOPB effective area and V Blank width setting			
D1h	30D1h	0				09h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
D2h	30D2h	0	FINFO_HWIDTH [12:0]	LSB	09A8h	A8h	S
		1					
		2					
		3					
		4					
		5					
		6		FINFO width setting			
		7					
D3h	30D3h	0				09h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
D4h	30D4h	0	VMAX [23:0]	LSB	0008AAh	AAh	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
D5h	30D5h	0		When sensor master mode vertical span setting. (Number of operation lines count from 1)		08h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
D6h	30D6h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
D8h	30D8h	0	HMAX [15:0]	LSB	0167h	67h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7		When sensor master mode and sensor slave mode, horizontal span setting. (Number of operation clocks count from 1)			
D9h	30D9h	0				01h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
DCh	30DCh	0 1	FREQ [1:0]	Set to data rate [SLVS] 0h: 594 Mbps 1h: 297 Mbps 2h: 891 Mbps 3h: 445.5 Mbps	2h	02h	S
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
E2h	30E2h	0 1 2 3 4 5 6 7	GMRWT [7:0]	Refer to the register list in each Readout mode	06h	06h	S
E3h	30E3h	0 1 2 3 4 5 6 7	GMTWT [7:0]	Refer to the register list in each Readout mode	28h	28h	S
E6h	30E6h	0 1 2 3 4 5 6 7	GSDLY [7:0]	Refer to the register list in each Readout mode	12h	12h	S

17.2. Chip ID = 03 (Write: Chip ID = 03h, Read: Chip ID = 83h, I²C: 31**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
00h	3100h	0	ROI_MODE [0]	Selection of ROI mode 0: ROI Mode 1: Overlap ROI Mode	0	00h	S
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
04h	3104h	0	FID0_ROIH1ON [0]	The horizontal setting of FID0 ROI area (1, y) (y = 1 to 8) 0: Disable 1: Enable	0	00h	V
		1	FID0_ROIV1ON [0]	The vertical setting of FID0 ROI area (x, 1) (x = 1 to 8) 0: Disable 1: Enable	0		I
		2	FID0_ROIH2ON [0]	The horizontal setting of FID0 ROI area (2, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		3	FID0_ROIV2ON [0]	The vertical setting of FID0 ROI area (x, 2) (x = 1 to 8) 0: Disable 1: Enable	0		I
		4	FID0_ROIH3ON [0]	The horizontal setting of FID0 ROI area (3, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		5	FID0_ROIV3ON [0]	The vertical setting of FID0 ROI area (x, 3) (x = 1 to 8) 0: Disable 1: Enable	0		I
		6	FID0_ROIH4ON [0]	The horizontal setting of FID0 ROI area (4, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		7	FID0_ROIV4ON [0]	The vertical setting of FID0 ROI area (x, 4) (x = 1 to 8) 0: Disable 1: Enable	0		I

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
05h	3105h	0	FID0_ROIH5ON [0]	The horizontal setting of FID0 ROI area (5, y) (y = 1 to 8) 0: Disable 1: Enable	0	00h	V
		1	FID0_ROIV5ON [0]	The vertical setting of FID0 ROI area (x, 5) (x = 1 to 8) 0: Disable 1: Enable	0		I
		2	FID0_ROIH6ON [0]	The horizontal setting of FID0 ROI area (6, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		3	FID0_ROIV6ON [0]	The vertical setting of FID0 ROI area (x, 6) (x = 1 to 8) 0: Disable 1: Enable	0		I
		4	FID0_ROIH7ON [0]	The horizontal setting of FID0 ROI area (7, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		5	FID0_ROIV7ON [0]	The vertical setting of FID0 ROI area (x, 7) (x = 1 to 8) 0: Disable 1: Enable	0		I
		6	FID0_ROIH8ON [0]	The horizontal setting of FID0 ROI area (8, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		7	FID0_ROIV8ON [0]	The vertical setting of FID0 ROI area (x, 8) (x = 1 to 8) 0: Disable 1: Enable	0		I

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
20h	3120h	0	FID0_ROIPH1 [12:0]	LSB Designation of horizontal cropping position for FID0 on area (1, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
21h	3121h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
22h	3122h	0	FID0_ROIPV1 [12:0]	LSB Designation of vertical cropping position for FID0 on area (x, 1) (x = 1 to 8) *Set the value of multiple of 8	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7					
23h	3123h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
24h	3124h	0	FID0_ROIWH1 [12:0]	LSB Designation of horizontal cropping size for FID0 on area (1, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
25h	3125h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
26h	3126h	0	FID0_ROIWV1 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping size for FID0 on area (x, 1) (x = 1 to 8) *Set the value of multiple of 8			
27h	3127h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
28h	3128h	0	FID0_ROIPH2 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping position for FID0 on area (2, y) (y = 1 to 8) *Set the value of multiple of 8			
29h	3129h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
2Ah	312Ah	0	FID0_ROIPV2 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping position for FID0 on area (x, 2) (x = 1 to 8) *Set the value of multiple of 8			
2Bh	312Bh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
2Ch	312Ch	0	FID0_ROIWH2 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping size for FID0 on area (2, y) (y = 1 to 8) *Set the value of multiple of 8			
2Dh	312Dh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
2Eh	312Eh	0	FID0_ROIWV2 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping size for FID0 on area (x, 2) (x = 1 to 8) *Set the value of multiple of 8			
2Fh	312Fh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
30h	3130h	0	FID0_ROIPH3 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping position for FID0 on area (3, y) (y = 1 to 8) *Set the value of multiple of 8			
31h	3131h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
32h	3132h	0	FID0_ROIPV3 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6		Designation of vertical cropping position for FID0 on area (x, 3) (x = 1 to 8) *Set the value of multiple of 8			
		7					
33h	3133h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
34h	3134h	0	FID0_ROIWH3 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5		Designation of horizontal cropping size for FID0 on area (3, y) (y = 1 to 8) *Set the value of multiple of 8			
		6					
		7					
35h	3135h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
36h	3136h	0	FID0_ROIWV3 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5		Designation of vertical cropping size for FID0 on area (x, 3) (x = 1 to 8) *Set the value of multiple of 8			
		6					
		7					
37h	3137h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
38h	3138h	0	FID0_ROIPH4 [12:0]	LSB Designation of horizontal cropping position for FID0 on area (4, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
39h	3139h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
3Ah	313Ah	0	FID0_ROIPV4 [12:0]	LSB Designation of vertical cropping position for FID0 on area (x, 4) (x = 1 to 8) *Set the value of multiple of 8	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7					
3Bh	313Bh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
3Ch	313Ch	0	FID0_ROIWH4 [12:0]	LSB Designation of horizontal cropping size for FID0 on area (4, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
3Dh	313Dh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
3Eh	313Eh	0	FID0_ROIWV4 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping size for FID0 on area (x, 4) (x = 1 to 8) *Set the value of multiple of 8			
3Fh	313Fh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
40h	3140h	0	FID0_ROIPH5 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping position for FID0 on area (5, y) (y = 1 to 8) *Set the value of multiple of 8			
41h	3141h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
42h	3142h	0	FID0_ROIPV5 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping position for FID0 on area (x, 5) (x = 1 to 8) *Set the value of multiple of 8			
43h	3143h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
44h	3144h	0	FID0_ROIWH5 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping size for FID0 on area (5, y) (y = 1 to 8) *Set the value of multiple of 8			
45h	3145h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
46h	3146h	0	FID0_ROIWV5 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping size for FID0 on area (x, 5) (x = 1 to 8) *Set the value of multiple of 8			
47h	3147h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
48h	3148h	0	FID0_ROIPH6 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping position for FID0 on area (6, y) (y = 1 to 8) *Set the value of multiple of 8			
49h	3149h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
4Ah	314Ah	0	FID0_ROIPV6 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6		Designation of vertical cropping position for FID0 on area (x, 6) (x = 1 to 8) *Set the value of multiple of 8			
		7					
4Bh	314Bh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
4Ch	314Ch	0	FID0_ROIWH6 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5		Designation of horizontal cropping size for FID0 on area (6, y) (y = 1 to 8) *Set the value of multiple of 8			
		6					
		7					
4Dh	314Dh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
4Eh	314Eh	0	FID0_ROIWV6 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5		Designation of vertical cropping size for FID0 on area (x, 6) (x = 1 to 8) *Set the value of multiple of 8			
		6					
		7					
4Fh	314Fh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
50h	3150h	0	FID0_ROIPH7 [12:0]	LSB Designation of horizontal cropping position for FID0 on area (7, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
51h	3151h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
52h	3152h	0	FID0_ROIPV7 [12:0]	LSB Designation of vertical cropping position for FID0 on area (x, 7) (x = 1 to 8) *Set the value of multiple of 8	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7					
53h	3153h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
54h	3154h	0	FID0_ROIWH7 [12:0]	LSB Designation of horizontal cropping size for FID0 on area (7, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
55h	3155h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
56h	3156h	0	FID0_ROIWV7 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping size for FID0 on area (x, 7) (x = 1 to 8) *Set the value of multiple of 8			
57h	3157h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
58h	3158h	0	FID0_ROIPH8 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping position for FID0 on area (8, y) (y = 1 to 8) *Set the value of multiple of 8			
59h	3159h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
5Ah	315Ah	0	FID0_ROIPV8 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping position for FID0 on area (x, 8) (x = 1 to 8) *Set the value of multiple of 8			
5Bh	315Bh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
5Ch	315Ch	0	FID0_ROIWH8 [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of horizontal cropping size for FID0 on area (8, y) (y = 1 to 8) *Set the value of multiple of 8			
5Dh	315Dh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
5Eh	315Eh	0	FID0_ROIWV8 [12:0]	LSB	0000h	00h	I
		1					
		2					
		3					
		4					
		5					
		6					
		7		Designation of vertical cropping size for FID0 on area (x, 8) (x = 1 to 8) *Set the value of multiple of 8			
5Fh	315Fh	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

17.3. Chip ID = 04 (Write: Chip ID = 04h, Read: Chip ID = 84h, I²C: 32**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
00h	3200h	0		Fixed to 1	1	05h	—
		1		Fixed to 0	0		—
		2		Fixed to 1	1		—
		3		Fixed to 0	0		—
		4	ADBIT [1:0]	AD conversion bits setting 0h: 10 bit 1h: 12 bit 2h: 8 bit 3h: Setting prohibited	0h		S
		5					
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
04h	3204h	0	VREVERSE [0]	Vertical (V) direction readout inversion control 0: Normal 1: Inverted	0	00h	V
		1	HREVERSE [0]	Horizontal (H) direction readout inversion control 0: Normal 1: Inverted	0		V
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
1Ch	321Ch	0	INCKSEL_N0 [7:0]	Set according to INCK frequency and drive mode.	80h	80h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
1Dh	321Dh	0	INCKSEL_N1 [7:0]	Set according to INCK frequency and drive mode.	05h	05h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
1Eh	321Eh	0	INCKSEL_N2 [7:0]	Set according to INCK frequency and drive mode.	E0h	E0h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
1Fh	321Fh	0	INCKSEL_N3 [7:0]	Set according to INCK frequency and drive mode.	00h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
24h	3224h	0	INCKSEL_D0 [7:0]	Set according to INCK frequency and drive mode.	80h	80h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
25h	3225h	0	INCKSEL_D1 [7:0]	Set according to INCK frequency and drive mode.	14h	14h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
26h	3226h	0	INCKSEL_D2 [7:0]	Set according to INCK frequency and drive mode.	C0h	C0h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
27h	3227h	0	INCKSEL_D3 [7:0]	Set according to INCK frequency and drive mode.	D0h	D0h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
3Ch	323Ch	0		Fixed to 1	1	19h	—
		1	LLBLANK [7:0]	LSB Refer to the register list in each Readout mode	0Ch		S
		2					
		3					
		4					
		5					
		6					
		7		MSB			
3Dh	323Dh	0		Fixed to 0	0	00h	—
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
3Eh	323Eh	0	VINT_EN [0]	Setting of Interrupt mode in Trigger Mode 0: V interrupt is disable 1: V interrupt is enable	1	33h	S
		1	VINT_EN_NOR [0]	Setting of Interrupt mode in Normal Mode 0: V interrupt is disable 1: V interrupt is enable	1		S
		2		Refer to the register list in each Readout mode	0Ch		S
		3					
		4					
		5					
		6					
		7					
40h	3240h	0	SHS [23:0]	LSB	000070h	70h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
41h	3241h	0				00h	
		1					
		2					
		3		Storage time adjustment Designated in line unit			
		4					
		5					
		6					
		7					
42h	3242h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			

17.4. Chip ID = 05 (Write: Chip ID = 05h, Read: Chip ID = 85h, I²C: 33**h)

Please refer to the other register map file for the register that has not been described.

17.5. Chip ID = 06 (Write: Chip ID = 06h, Read: Chip ID = 86h, I²C: 34**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
00h	3400h	0	TRIGMODE [2:0]	Global shutter mode setting 0h: Normal mode 1h: Sequential Trigger mode 2h: Fast Trigger mode Others: Setting prohibited	0h	00h	I [*1]
		1					
		2					
		3	TRIGTIMING [1:0]	Trigger mode setting 0h: Normal mode 1h: Trigger mode Others: Setting prohibited	0h		I [*1]
		4					
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
30h	3430h	0	ODBIT [1:0]	Number of output bit setting 0h: 10 bit 1h: 12 bit 2h: 8 bit 3h: Setting prohibited	0h	00h	S
		1					
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
35h	3435h	0	TOUT1SEL [1:0]	TOUT1 pin setting 0h: Low fixed 3h: Pulse output Others: Setting prohibited	0h	00h	S
		1					
		2	TOUT2SEL [1:0]	TOUT2 pin setting 0h: Low fixed 3h: Pulse output Others: Setting prohibited	0h		S
		3					
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
36h	3436h	0	TOUT0SEL [2:0]	TOUT0 pin setting 0h: Low fixed 1h: Exposure period monitoring Others: Setting prohibited	0h	00h	S
		1					
		2					
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

[*1] Refer to “Mode Transitions of Global Shutter Operation”

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
3Ah	343Ah	0	TRIG_TOUT1_SEL [3:0]	TOUT1 output setting 0h: Low fixed 1h: Pulse1 output Others: Setting prohibited	0h	00h	S
		1					
		2					
		3					
		4	TRIG_TOUT2_SEL [3:0]	TOUT2 output setting 0h: Low fixed 2h: Pulse2 output Others: Setting prohibited	0h		S
		5					
		6					
		7					
3Ch	343Ch	0		Fixed to 0	0	C0h	—
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4	SYNCSEL [1:0]	XHS, XVS pin setting 0h: Normal Output 3h: Hi-Z Others: Setting prohibited	0h		S
		5					
		6		Fixed to 1	1		—
		7		Fixed to 1	1		—
44h	3444h	0	STBSLVS [3:0]	Channel standby control of SLVS 1h: activate 8 ch 2h: activate 4 ch 3h: activate 2 ch Others: Setting prohibited	1h	01h	S
		1					
		2					
		3					
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
78h	3478h	0	PULSE1_EN_NOR [0]	Pulse1 output in normal mode 0: Disable 1: Enable	0	00h	S
		1	PULSE1_EN_TRIG [0]	Pulse1 output in trigger mode 0: Disable 1: Enable	0		S
		2	PULSE1_POL [0]	Pulse1 polarity selection 0: High active 1: Low active	0		S
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
79h	3479h	0	PULSE1_UP [23:0]	LSB	000000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
7Ah	347Ah	0		Pulse1 active period start timing setting Designated in line units from reference point (For details, see the “Pulse Output Function”)		00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
7Bh	347Bh	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
7Ch	347Ch	0	PULSE1_DN [23:0]	LSB	000000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
7Dh	347Dh	0		Pulse1 active period end timing setting Designated in line units from readout start (For details, see the “Pulse Output Function”)		00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
7Eh	347Eh	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
80h	3480h	0	PULSE2_EN_NOR [0]	Pulse2 output in normal mode 0: Disable 1: Enable	0	00h	S
		1	PULSE2_EN_TRIG [0]	Pulse2 output in trigger mode 0: Disable 1: Enable	0		S
		2	PULSE2_POL [0]	Pulse2 polarity selection 0: High active 1: Low active	0		S
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 1	0		S
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
81h	3481h	0	PULSE2_UP [23:0]	LSB	000000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
82h	3482h	0		Pulse2 active period end timing setting Designated in line units from reference point (For details, see the “Pulse Output Function”)		00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
83h	3483h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
84h	3484h	0	PULSE2_DN [23:0]	LSB	000000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
85h	3485	0		Pulse2 active period end timing setting Designated in line units from reference point (For details, see the “Pulse Output Function”)		00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
86h	3486h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			

17.6. Chip ID = 07 (Write: Chip ID = 07h, Read: Chip ID = 87h, I²C: 35**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
02h	3502h	0 1 2 3 4 5 6 7	GAIN_RTS [7:0]	Setting of Gain Reflection Timing at Normal mode. 08h: Gain reflect at the frame 09h: Gain reflect at the next frame (Same timing as SHS reflecting output.) Others: Setting prohibited	00h	00h	S
14h	3514h	0 1 2 3 4 5 6 7	GAIN [8:0]	LSB Gain setting 0 dB (0d) to 48 dB (480d) 0.1 dB Step (Refer to Address 02h about detail of Reflection Timing.)	000h	00h	V
15h	3515h	0		MSB		00h	
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
21h	3521h	0 1 2 3 4 5 6 7		Refer to the register list in each Readout mode	EDh	EDh	S
46h	3546h	0 1 2 3 4 5 6 7		Refer to the register list in each Readout mode	3Bh	3Bh	S

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
B4h	35B4h	0	BLKLEVEL [11:0]	LSB	03Ch	3Ch	V
		1					
		2					
		3					
		4		Black level offset value setting Recommended value. 00Fh: 8 bit 03Ch: 10 bit 0F0h: 12 bit			
		5					
		6					
		7					
B5h	35B5h	0				00h	
		1					
		2					
		3		MSB			
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

17.7. Chip ID = 08 (Write: Chip ID = 08h, Read: Chip ID = 88h, I²C: 36**h)

Please refer to the other register map file for the register that has not been described.

17.8. Chip ID = 09 (Write: Chip ID = 09h, Read: Chip ID = 89h, I²C: 37**h)

Please refer to the other register map file for the register that has not been described.

17.9. Chip ID = 0A (Write: Chip ID = 0Ah, Read: Chip ID = 8Ah, I²C: 38**h)

Please refer to the other register map file for the register that has not been described.

17.10. Chip ID = 0B (Write: Chip ID = 0Bh, Read: Chip ID = 8Bh, I²C: 39**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
04h	3904h	0	LANESEL [2:0]	Setting of SLVS output Channel 0h: 8 ch 2h: 4 ch 3h: 2 ch Others: Setting prohibited	0h	00h	S
		1					
		2					
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

17.11. Chip ID = 0C (Write: Chip ID = 0Ch, Read: Chip ID = 8Ch, I²C: 3A**h)

Please refer to the other register map file for the register that has not been described.

17.12. Chip ID = 0D (Write: Chip ID = 0Dh, Read: Chip ID = 8Dh, I²C: 3B**h)

Please refer to the other register map file for the register that has not been described.

17.13. Chip ID = 10 (Write: Chip ID = 10h, Read: Chip ID = 90h, I²C: 3E**h)

Please refer to the other register map file for the register that has not been described.

17.14. Chip ID = 11 (Write: Chip ID = 11h, Read: Chip ID = 91h, I²C: 3F**h)

Please refer to the other register map file for the register that has not been described.

17.15. Chip ID = 12 (Write: Chip ID = 12h, Read: Chip ID = 92h, I²C: 40**h)

Please refer to the other register map file for the register that has not been described.

17.16. Chip ID = 13 (Write: Chip ID = 13h, Read: Chip ID = 93h, I²C: 41**h)

Please refer to the other register map file for the register that has not been described.

17.17. Chip ID = 14 (Write: Chip ID = 14h, Read: Chip ID = 94h, I²C: 42**h)

Please refer to the other register map file for the register that has not been described.

17.18. Chip ID = 15 (Write: Chip ID = 15h, Read: Chip ID = 95h, I²C: 43**h)

Please refer to the other register map file for the register that has not been described.

17.19. Chip ID = 16 (Write: Chip ID = 16h, Read: Chip ID = 96h, I²C: 44**h)

Please refer to the other register map file for the register that has not been described.

17.20. Chip ID = 17 (Write: Chip ID = 17h, Read: Chip ID = 97h, I²C: 45**h)

Please refer to the other register map file for the register that has not been described.

17.21. Chip ID = 18 (Write: Chip ID = 18h, Read: Chip ID = 98h, I²C: 46**h)

Please refer to the other register map file for the register that has not been described.

17.22. Chip ID = 19 (Write: Chip ID = 19h, Read: Chip ID = 99h, I²C: 47**h)

Please refer to the other register map file for the register that has not been described.

17.23. Chip ID = 1A (Write: Chip ID = 1Ah, Read: Chip ID = 9Ah, I²C: 48**h)

Please refer to the other register map file for the register that has not been described.

17.24. Chip ID = 1B (Write: Chip ID = 1Bh, Read: Chip ID = 9Bh, I²C: 49**h)

Please refer to the other register map file for the register that has not been described.

17.25. Chip ID = 1C (Write: Chip ID = 1Ch, Read: Chip ID = 9Ch, I²C: 4A**h)

Please refer to the other register map file for the register that has not been described.

17.26. Chip ID = 1E (Write: Chip ID = 1Eh, Read: Chip ID = 9Eh, I²C: 4C**h)

Please refer to the other register map file for the register that has not been described.

18. Readout Drive Modes

The table below lists the operating modes available with this sensor. (Each value is the Max. frame rate of each number of ch.)

FREQ (CID = 02h, Address = DCh, [1:0]) = 0h

Drive mode	SLVS ch[*1]	Data rate [Mbps/ch]	A/D conversion	Frame rate [frame/s]	Number of recording pixels		Number of INCK in 1 H		
					H	V	INCK: 37.125 MHz	INCK: 74.25 MHz	INCK: 54 MHz
All pixel	8	594	8	92.3	2448	2048	181.5	363.0	264.0
	4	594		49.2			345.0	690.0	501.9
	2	594		25.8			662.0	1324.0	963.0
	8	594	10	74.9			225.0	450.0	327.3
	4	594		39.6			429.5	859.0	624.8
	2	594		20.7			825.5	1651.0	1200.8
	8	594	12	63.0			268.5	537.0	390.6
	4	594		33.2			513.5	1027.0	747.0
	2	594		17.3			989.0	1978.0	1438.6
Vertical / Horizontal 1/2 subsampling	8	594	8	220.3	1224	1024	145.0	290.0	211.0
	4	594		170.2			191.0	382.0	277.9
	2	594		93.9			354.0	708.0	515.0
	8	594	10	180.4			179.5	359.0	261.1
	4	594		138.3			237.0	474.0	344.8
	2	594		75.7			440.5	881.0	640.8
	8	594	12	162.8			200.0	400.0	291.0
	4	594		116.9			282.5	565.0	411.0
	2	594		63.8			527.0	1054.0	766.6
ROI	8	594	8	[*2]	[*3]	[*3]	181.5	363.0	264.0
	4	594		[*2]			345.0	690.0	501.9
	2	594		[*2]			662.0	1324.0	963.0
	8	594	10	[*2]			225.0	450.0	327.3
	4	594		[*2]			429.5	859.0	624.8
	2	594		[*2]			825.5	1651.0	1200.8
	8	594	12	[*2]			268.5	537.0	390.6
	4	594		[*2]			513.5	1027.0	747.0
	2	594		[*2]			989.0	1978.0	1438.6

[*1] The total data rate is the data rate multiplied by the number of channels.
Example) In All-pixel 92.3 [frame/s] mode: 594 [Mbps/ch] × 8 = 4.752 [Gbps]

[*2] See the section of “ROI mode”

[*3] Designated cropping area (ROI)

FREQ (CID = 02h, Address = DCh, [1:0]) = 1h

Drive mode	SLVS ch[*1]	Data rate [Mbps/ch]	A/D conversion	Frame rate [frame/s]	Number of recording pixels		Number of INCK in 1 H		
					H	V	INCK: 37.125 MHz	INCK: 74.25 MHz	INCK: 54 MHz
All pixel	8	297	8	48.3	2448	2048	351.0	702.0	510.6
	4	297		25.4			672.5	1345.0	978.2
	2	297		13.0			1315.5	2631.0	1913.5
	8	297	10	38.9			437.0	874.0	635.7
	4	297		20.4			839.0	1678.0	1220.4
	2	297		10.4			1642.5	3285.0	2389.1
	8	297	12	32.6			523.0	1046.0	760.8
	4	297		17.0			1005.0	2010.0	1461.9
	2	297		8.7			1969.0	3938.0	2864.0
Vertical / Horizontal 1/2 subsampling	8	297	8	165.3	1224	1024	197.0	394.0	286.6
	4	297		91.2			364.5	729.0	530.2
	2	297		48.1			699.5	1399.0	1017.5
	8	297	10	134.3			244.5	489.0	355.7
	4	297		73.6			454.0	908.0	660.4
	2	297		38.7			872.5	1745.0	1269.1
	8	297	12	113.1			292.0	584.0	424.8
	4	297		61.9			543.0	1086.0	789.9
	2	297		32.4			1045.0	2090.0	1520.0
ROI	8	297	8	[*2]	[*3]	[*3]	351.0	702.0	510.6
	4	297		[*2]			672.5	1345.0	978.2
	2	297		[*2]			1315.5	2631.0	1913.5
	8	297	10	[*2]			437.0	874.0	635.7
	4	297		[*2]			839.0	1678.0	1220.4
	2	297		[*2]			1642.5	3285.0	2389.1
	8	297	12	[*2]			523.0	1046.0	760.8
	4	297		[*2]			1005.0	2010.0	1461.9
	2	297		[*2]			1969.0	3938.0	2864.0

[*1] The total data rate is the data rate multiplied by the number of channels.
Example) In All-pixel 48.3 [frame/s] mode: 297 [Mbps/ch] × 8 = 2.376 [Gbps]

[*2] See the section of “ROI mode”

[*3] Designated cropping area (ROI)

FREQ (CID = 02h, Address = DCh, [1:0]) = 2h

Drive mode	SLVS ch[*1]	Data rate [Mbps/ch]	A/D conversion	Frame rate [frame/s]	Number of recording pixels		Number of INCK in 1 H		
					H	V	INCK: 37.125 MHz	INCK: 74.25 MHz	INCK: 54 MHz
All pixel	8	891	8	114.8	2448	2048	145.0	290.0	211.0
	4	891		72.0			234.0	468.0	340.4
	2	891		38.2			445.5	891.0	648.0
	8	891	10	93.4			179.5	359.0	261.1
	4	891		58.4			290.0	580.0	421.9
	2	891		30.8			554.5	1109.0	806.6
	8	891	12	84.0			200.0	400.0	291.0
	4	891		49.2			345.0	690.0	501.9
	2	891		25.8			662.0	1324.0	963.0
Vertical / Horizontal 1/2 subsampling	8	891	8	220.3	1224	1024	145.0	290.0	211.0
	4	891		220.3			145.0	290.0	211.0
	2	891		136.8			240.0	480.0	349.1
	8	891	10	180.4			179.5	359.0	261.1
	4	891		180.4			179.5	359.0	261.1
	2	891		111.2			297.5	595.0	432.8
	8	891	12	162.8			200.0	400.0	291.0
	4	891		162.8			200.0	400.0	291.0
	2	891		93.9			354.0	708.0	515.0
ROI	8	891	8	[*2]	[*3]	[*3]	145.0	290.0	211.0
	4	891		[*2]			234.0	468.0	340.4
	2	891		[*2]			445.5	891.0	648.0
	8	891	10	[*2]			179.5	359.0	261.1
	4	891		[*2]			290.0	580.0	421.9
	2	891		[*2]			554.5	1109.0	806.6
	8	891	12	[*2]			200.0	400.0	291.0
	4	891		[*2]			345.0	690.0	501.9
	2	891		[*2]			662.0	1324.0	963.0

[*1] The total data rate is the data rate multiplied by the number of channels.
Example) In All-pixel 114.8 [frame/s] mode: 891 [Mbps/ch] × 8 = 7.128 [Gbps]

[*2] See the section of “ROI mode”

[*3] Designated cropping area (ROI)

FREQ (CID = 02h, Address = DCh, [1:0]) = 3h

Drive mode	SLVS ch[*1]	Data rate [Mbps/ch]	A/D conversion	Frame rate [frame/s]	Number of recording pixels		Number of INCK in 1 H		
					H	V	INCK: 37.125 MHz	INCK: 74.25 MHz	INCK: 54 MHz
All pixel	8	445.5	8	71.0	2448	2048	237.5	475.0	345.5
	4	445.5		37.7			452.0	904.0	657.5
	2	445.5		19.4			881.0	1762.0	1281.5
	8	445.5	10	57.4			295.0	590.0	429.1
	4	445.5		30.3			563.0	1126.0	819.0
	2	445.5		15.6			1099.0	2198.0	1598.6
	8	445.5	12	48.3			351.0	702.0	510.6
	4	445.5		25.4			672.5	1345.0	978.2
	2	445.5		13.0			1315.5	2631.0	1913.5
Vertical / Horizontal 1/2 subsampling	8	445.5	8	220.3	1224	1024	145.0	290.0	211.0
	4	445.5		133.2			246.5	493.0	358.6
	2	445.5		71.0			470.5	941.0	684.4
	8	445.5	10	180.4			179.5	359.0	261.1
	4	445.5		108.3			306.0	612.0	445.1
	2	445.5		57.4			585.5	1171.0	851.7
	8	445.5	12	162.8			200.0	400.0	291.0
	4	445.5		91.2			364.5	729.0	530.2
	2	445.5		48.1			699.5	1399.0	1017.5
ROI	8	445.5	8	[*2]	[*3]	[*3]	237.5	475.0	345.5
	4	445.5		[*2]			452.0	904.0	657.5
	2	445.5		[*2]			881.0	1762.0	1281.5
	8	445.5	10	[*2]			295.0	590.0	429.1
	4	445.5		[*2]			563.0	1126.0	819.0
	2	445.5		[*2]			1099.0	2198.0	1598.6
	8	445.5	12	[*2]			351.0	702.0	510.6
	4	445.5		[*2]			672.5	1345.0	978.2
	2	445.5		[*2]			1315.5	2631.0	1913.5

[*1] The total data rate is the data rate multiplied by the number of channels.
Example) In All-pixel 71.0 [frame/s] mode: 445.5 [Mbps/ch] × 8 = 3.564 [Gbps]

[*2] See the section of “ROI mode”

[*3] Designated cropping area (ROI)

18.1. Restriction on Image Data Output

If the shutter releases on outputting the image data in this product, blank or Idle Code is inserted in the imade data because of shutter stabilization wait time. Shutter stabilization wait time depends on the readout mode.
The insertion timing of shutter stabilization wait time changes depending on the shutter release timing.
During the shutter stabilization wait time, the sync codes (SLVS) is not output.. Refer to the sync codes from the sensor and perform synchronization.

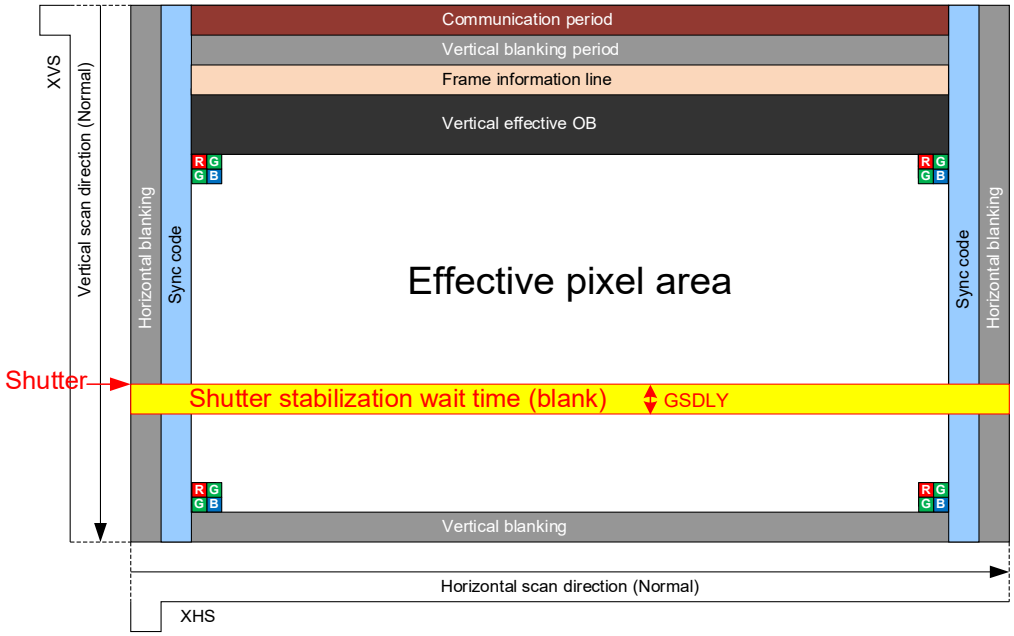


Image Drawing of Sutter stabilization wait time inserted (SLVS output)

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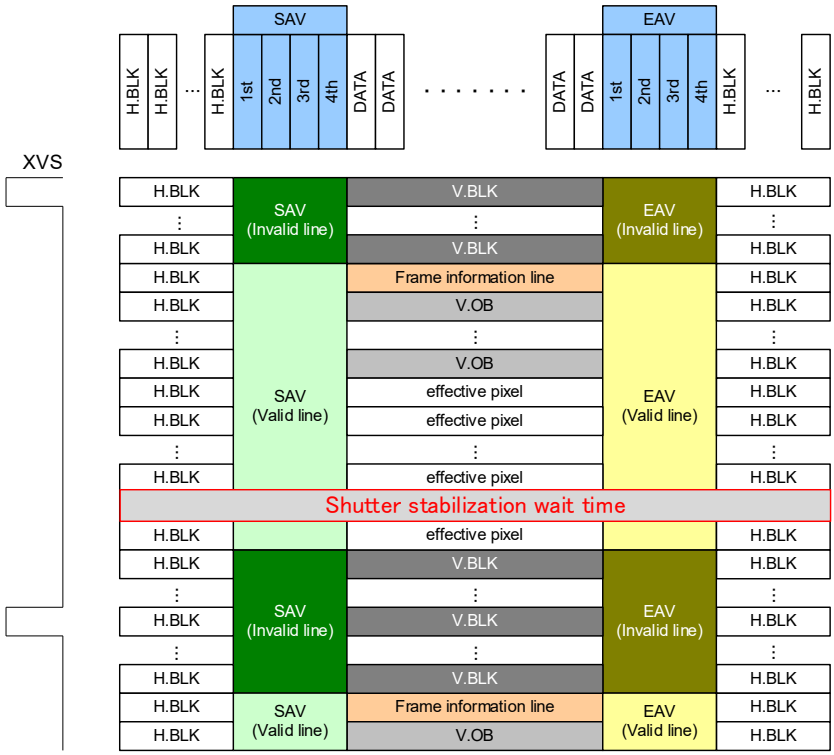
18.2. Image Data Output Format

18.2.1. SLVS Output Format

Sync code

The sync code is added immediately before and after “dummy signal + OB signal + effective pixel data” and then output. The sync code is output in order of 1st, 2nd, 3rd and 4th. The fixed value is output for 1st to 3rd. (BLK: Blanking period)



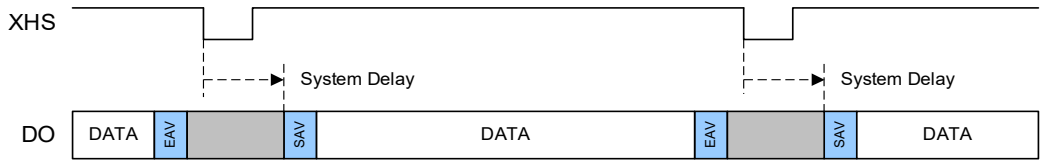
Sync Code Output Timing

List of Sync Code

Sync code	1st code			2nd code			3rd code			4th code		
	8 bit	10 bit	12 bit	8 bit	10 bit	12 bit	8 bit	10 bit	12 bit	8 bit	10 bit	12 bit
SAV (Valid line)	FFh	3FFh	FFFh	00h	000h	000h	00h	000h	000h	80h	200h	800h
EAV (Valid line)	FFh	3FFh	FFFh	00h	000h	000h	00h	000h	000h	9Dh	274h	9D0h
SAV (Invalid line)	FFh	3FFh	FFFh	00h	000h	000h	00h	000h	000h	ABh	2ACh	AB0h
EAV (Invalid line)	FFh	3FFh	FFFh	00h	000h	000h	00h	000h	000h	B6h	2D8h	B60h

Sync Code Output Timing

The sensor output signal passes through the internal circuits and is output with a latency time (system delay) relative to the horizontal sync signal. This system delay value is undefined for each line, so refer to the sync codes output from the sensor and perform synchronization.



18.3. Image Data Output Format on each Readout mode

18.3.1. All-pixel scan

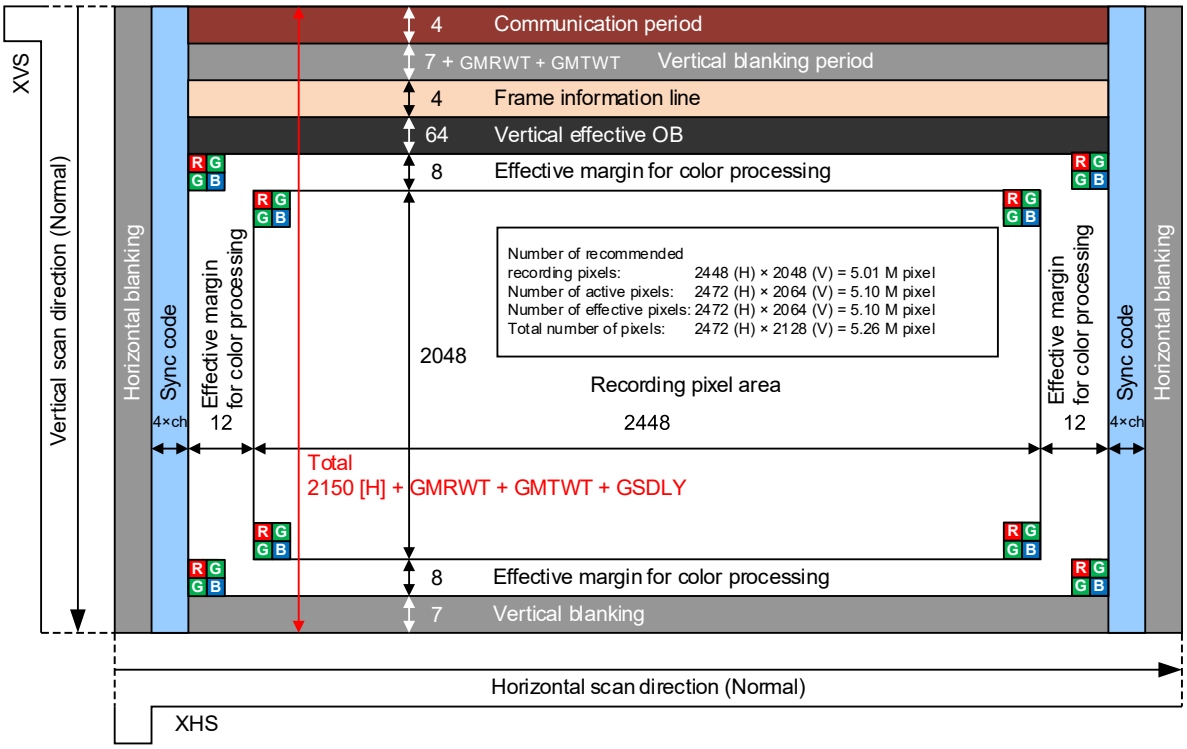
Register List of All-pixel scan mode

Please refer to the other register map file for the register that has not been described.

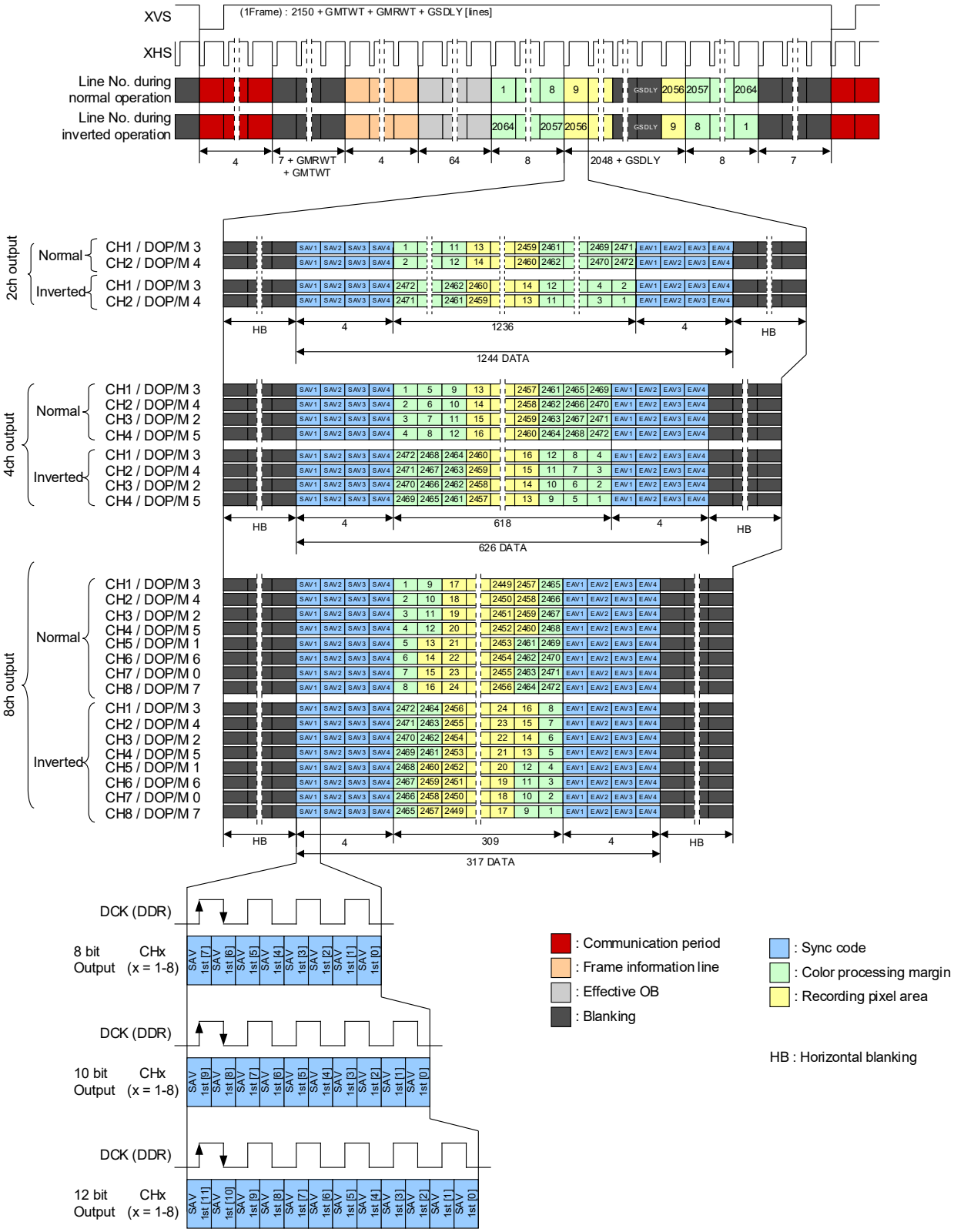
Address	bit	Register name	Initial Value	Setting value									Remarks
				AD = 8 bit			AD = 10 bit			AD = 12 bit			
				8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	
				92.3 [frame/s]	49.2 [frame/s]	25.8 [frame/s]	74.9 [frame/s]	39.6 [frame/s]	20.7 [frame/s]	63.0 [frame/s]	33.2 [frame/s]	17.3 [frame/s]	FREQ = 0h
				48.3 [frame/s]	25.4 [frame/s]	13.0 [frame/s]	38.9 [frame/s]	20.4 [frame/s]	10.4 [frame/s]	32.6 [frame/s]	17.0 [frame/s]	8.7 [frame/s]	FREQ = 1h
				114.8 [frame/s]	72.0 [frame/s]	38.2 [frame/s]	93.4 [frame/s]	58.4 [frame/s]	30.8 [frame/s]	84.0 [frame/s]	49.2 [frame/s]	25.8 [frame/s]	FREQ = 2h
				71.0 [frame/s]	37.7 [frame/s]	19.4 [frame/s]	57.4 [frame/s]	30.3 [frame/s]	15.6 [frame/s]	48.3 [frame/s]	25.4 [frame/s]	13.0 [frame/s]	FREQ = 3h
				594 Mbps/ch									FREQ = 0h
				297 Mbps/ch									FREQ = 1h
				891 Mbps/ch									FREQ = 2h
				445.5 Mbps/ch									FREQ = 3h
Chip ID = 02h													
14h	[7:0]	INCKSEL_ST0	0Ah	INCK = 74.25 MHz: 0Ah INCK = 54 MHz: F0h INCK = 37.125 MHz: 05h									
15h	[7:0]	INCKSEL_ST1	22h	INCK = 74.25 MHz: 22h INCK = 54 MHz: D2h INCK = 37.125 MHz: 91h									
16h	[7:0]	INCKSEL_ST2	B1h	INCK = 74.25 MHz: B1h INCK = 54 MHz: 80h INCK = 37.125 MHz: 50h									
18h	[7:0]	INCKSEL_ST3	40h	INCK = 74.25 MHz: 40h INCK = 54 MHz: 18h INCK = 37.125 MHz: 20h									
19h	[7:0]	INCKSEL_ST4	04h	INCK = 74.25 MHz: 04h INCK = 54 MHz: 03h INCK = 37.125 MHz: 02h									
1Bh	[7:0]	INCKSEL_ST5	3Ah	INCK = 74.25 MHz: 3Ah INCK = 54 MHz: 2Ah INCK = 37.125 MHz: 1Dh									
3Ch	[4:3]	HVMODE	0h	0h									All-pixel
D0h	[7:0]	VOPB_VBLK_HWIDTH	09A8h	09A8h									
D1h	[4:0]												
D2h	[7:0]	FINFO_HWIDTH	09A8h	09A8h									
D3h	[4:0]												
D4h	[7:0]	VMAX	0008AAh	8A6h	88Ah	87Ah	89Ah	884h	876h	892h	87Ch	874h	FREQ = 0h
D5h	[7:0]			88Ah	87Ah	872h	884h	876h	870h	87Ch	874h	86Eh	FREQ = 1h
D6h	[7:0]			8B6h	89Ah	882h	8A6h	890h	87Ch	8A0h	88Ah	87Ah	FREQ = 2h
				898h	882h	876h	88Eh	87Ch	874h	88Ah	87Ah	872h	FREQ = 3h
D8h	[7:0]	HMAX	0167h	16Bh	2B2h	52Ch	1C2h	35Bh	673h	219h	403h	7BAh	FREQ = 0h
				2BEh	541h	A47h	36Ah	68Eh	CD5h	416h	7DAh	F62h	FREQ = 1h
D9h	[7:0]			122h	1D4h	37Bh	167h	244h	455h	190h	2B2h	52Ch	FREQ = 2h
				1DBh	388h	6E2h	24Eh	466h	896h	2BEh	541h	A47h	FREQ = 3h
DCh	[1:0]	FREQ	2h	0h / 1h / 2h / 3h									
E2h	[7:0]	GMRWT	06h	06h	04h	02h	06h	04h	02h	04h	02h	02h	FREQ = 0h
				04h	02h	02h	04h	02h	02h	02h	02h	02h	FREQ = 1h
				08h	06h	04h	06h	04h	02h	06h	04h	02h	FREQ = 2h
				06h	04h	02h	04h	02h	02h	04h	02h	02h	FREQ = 3h
E3h	[7:0]	GMTWT	28h	28h	16h	0Ch	20h	12h	0Ah	1Ch	0Eh	08h	FREQ = 0h
				16h	0Ch	06h	12h	0Ah	06h	0Eh	08h	04h	FREQ = 1h
				32h	20h	10h	28h	1Ah	0Eh	24h	16h	0Ch	FREQ = 2h
				1Eh	10h	0Ah	18h	0Eh	08h	16h	0Ch	06h	FREQ = 3h

Address	bit	Register name	Initial Value	Setting value									Remarks
				AD = 8 bit			AD = 10 bit			AD = 12 bit			
				8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	
				92.3 [frame/s]	49.2 [frame/s]	25.8 [frame/s]	74.9 [frame/s]	39.6 [frame/s]	20.7 [frame/s]	63.0 [frame/s]	33.2 [frame/s]	17.3 [frame/s]	FREQ = 0h
				48.3 [frame/s]	25.4 [frame/s]	13.0 [frame/s]	38.9 [frame/s]	20.4 [frame/s]	10.4 [frame/s]	32.6 [frame/s]	17.0 [frame/s]	8.7 [frame/s]	FREQ = 1h
				114.8 [frame/s]	72.0 [frame/s]	38.2 [frame/s]	93.4 [frame/s]	58.4 [frame/s]	30.8 [frame/s]	84.0 [frame/s]	49.2 [frame/s]	25.8 [frame/s]	FREQ = 2h
				71.0 [frame/s]	37.7 [frame/s]	19.4 [frame/s]	57.4 [frame/s]	30.3 [frame/s]	15.6 [frame/s]	48.3 [frame/s]	25.4 [frame/s]	13.0 [frame/s]	FREQ = 3h
				594 Mbps/ch									FREQ = 0h
				297 Mbps/ch									FREQ = 1h
				891 Mbps/ch									FREQ = 2h
				445.5 Mbps/ch									FREQ = 3h
E6h	[7:0]	GSDLY	12h	12h	0Ah	06h	0Eh	08h	04h	0Ch	06h	04h	FREQ = 0h
				0Ah	06h	04h	08h	04h	02h	06h	04h	02h	FREQ = 1h
				16h	0Eh	08h	12h	0Ch	06h	10h	0Ah	06h	FREQ = 2h
				0Eh	08h	04h	0Ch	06h	04h	0Ah	06h	04h	FREQ = 3h
Chip ID = 04h													
00h	[5:4]	ADBIT	0h	2h			0h			1h			0: 10 bit 1: 12 bit 2: 8 bit
1Ch	[7:0]	INCKSEL_N0	80h	INCK = 74.25 MHz: 80h INCK = 54 MHz: 80h INCK = 37.125 MHz: 40h									
1Dh	[7:0]	INCKSEL_N1	05h	05h									
1Eh	[7:0]	INCKSEL_N2	E0h	INCK = 74.25 MHz: E0h INCK = 54 MHz: 34h INCK = 37.125 MHz: E0h									
1Fh	[7:0]	INCKSEL_N3	00h	INCK = 74.25 MHz: 00h INCK = 54 MHz: 01h INCK = 37.125 MHz: 00h									
24h	[7:0]	INCKSEL_D0	80h	INCK = 74.25 MHz: 80h INCK = 54 MHz: 80h INCK = 37.125 MHz: 40h									
25h	[7:0]	INCKSEL_D1	14h	14h									
26h	[7:0]	INCKSEL_D2	C0h	INCK = 74.25 MHz: 80h INCK = 54 MHz: B0h INCK = 37.125 MHz: 80h									FREQ = 0h FREQ = 1h
				INCK = 74.25 MHz: C0h INCK = 54 MHz: 08h INCK = 37.125 MHz: C0h									FREQ = 2h FREQ = 3h
27h	[7:0]	INCKSEL_D3	D0h	90h									FREQ = 0h
				A0h									FREQ = 1h
				INCK = 74.25 MHz: D0h INCK = 54 MHz: D1h INCK = 37.125 MHz: D0h									FREQ = 2h
				INCK = 74.25 MHz: E0h INCK = 54 MHz: E1h INCK = 37.125 MHz: E0h									FREQ = 3h
3Ch	[7:1]	LLBLANK	0Ch	0Ch									
3Dh	[0]												
Chip ID = 06h													
30h	[1:0]	ODBIT	0h	2h			0h			1h			0: 10 bit 1: 12 bit 2: 8 bit
44h	[3:0]	STBSLVS	1h	1h	N/A	N/A	1h	N/A	N/A	1h	N/A	N/A	8 ch SLVS
				N/A	2h	N/A	N/A	2h	N/A	N/A	2h	N/A	4 ch SLVS
				N/A	N/A	3h	N/A	N/A	3h	N/A	N/A	3h	2 ch SLVS

Address	bit	Register name	Initial Value	Setting value									Remarks
				AD = 8 bit			AD = 10 bit			AD = 12 bit			
				8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	
				92.3 [frame/s]	49.2 [frame/s]	25.8 [frame/s]	74.9 [frame/s]	39.6 [frame/s]	20.7 [frame/s]	63.0 [frame/s]	33.2 [frame/s]	17.3 [frame/s]	FREQ = 0h
				48.3 [frame/s]	25.4 [frame/s]	13.0 [frame/s]	38.9 [frame/s]	20.4 [frame/s]	10.4 [frame/s]	32.6 [frame/s]	17.0 [frame/s]	8.7 [frame/s]	FREQ = 1h
				114.8 [frame/s]	72.0 [frame/s]	38.2 [frame/s]	93.4 [frame/s]	58.4 [frame/s]	30.8 [frame/s]	84.0 [frame/s]	49.2 [frame/s]	25.8 [frame/s]	FREQ = 2h
				71.0 [frame/s]	37.7 [frame/s]	19.4 [frame/s]	57.4 [frame/s]	30.3 [frame/s]	15.6 [frame/s]	48.3 [frame/s]	25.4 [frame/s]	13.0 [frame/s]	FREQ = 3h
				594 Mbps/ch									FREQ = 0h
				297 Mbps/ch									FREQ = 1h
				891 Mbps/ch									FREQ = 2h
				445.5 Mbps/ch									FREQ = 3h
Chip ID = 07h													
21h	[7:0]		EDh	EDh									
46h	[7:0]		3Bh	3Bh									
B4h	[7:0]	BLKLEVEL	03Ch	00Fh			03Ch			0F0h			Recommended value
B5h	[3:0]												
Chip ID = 0Bh													
04h	[2:0]	LANESEL	0h	0h	N/A	N/A	0h	N/A	N/A	0h	N/A	N/A	8 ch SLVS
				N/A	2h	N/A	N/A	2h	N/A	N/A	2h	N/A	4 ch SLVS
				N/A	N/A	3h	N/A	N/A	3h	N/A	N/A	3h	2 ch SLVS



Pixel Array Image Drawing in All-pixel scan Mode
(SLVS output Shutter stabilization wait time is not included)



Drive Timing Chart for Serial Output in All-pixel Scan Mode (SLVS output)

18.3.2. ROI mode

This Sensor has ROI function that signals are cut out and read out in multi arbitrary positions.
Cropping position can set maximum 64 areas that specified by horizontal 8 points and vertical 8 points, regarding effective pixel start position as origin (0, 0) in all pixel scan mode. Cropping is available from All-pixel scan mode and horizontal period are fixed to the value for this mode.
These cropped areas by horizontal cropping setting (ROI (1, y) to ROI (8, y)) are output with left justified and that extends the horizontal blanking period. In vertical cropping area (ROI (x, 1) to ROI (x, 8)), the number of image data is also output from cropping start line and the frame rate can be adjusted by changing the number of input XVS lines in slave mode or changing register VMAX in master mode.
One invalid frame is generated when the ROI area changing size or cropping address.
ROI image is shown in the figure below.
In case of Vertical / Horizontal 1/2 subsampling mode, this sensor doesn't support ROI mode.
The horizontal output width of Frame Information can be set by FINFO_HWIDTH register.
The horizontal output width of Vertical OB and Vertical blanking can be set by VOPB_VBLK_HWIDTH register.
This section is written in case of all-pixel scan mode for example on this document.

When SLVS output

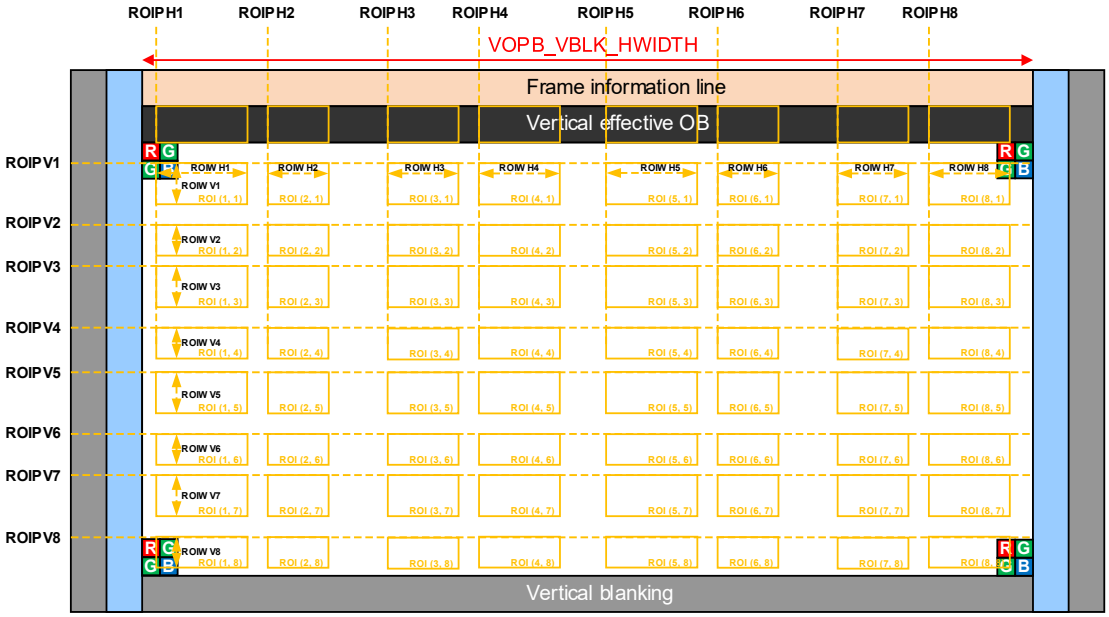
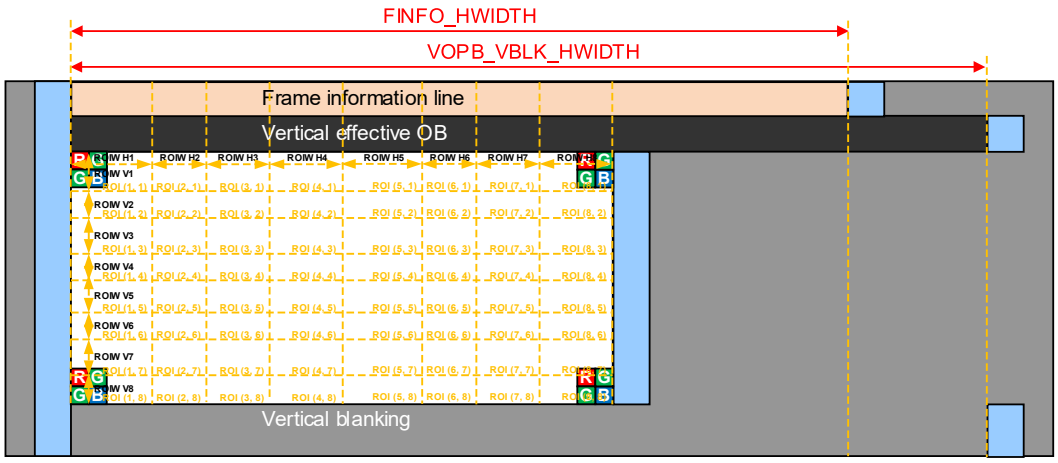


Image Drawing of Designated Areas in ROI Mode (SLVS output)



Details of Image Drawing (SLVS output)

Register List of ROI mode

Please set All-pixel scan mode to the settings other than the following.

Address	bit	Register name	Initial Value	Setting value									Remarks
				AD = 8 bit			AD = 10 bit			AD = 12 bit			
				8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	*7 [frame/s]	*8 [frame/s]	*9 [frame/s]	
				594 Mbps/ch									FREQ = 0h
				297 Mbps/ch									FREQ = 1h
				891 Mbps/ch									FREQ = 2h
				445.5 Mbps/ch									FREQ = 3h
Chip ID = 02h													
14h	[7:0]	INCKSEL_ST0	0Ah	INCK = 74.25 MHz: 0Ah INCK = 54 MHz: F0h INCK = 37.125 MHz: 05h									
15h	[7:0]	INCKSEL_ST1	22h	INCK = 74.25 MHz: 22h INCK = 54 MHz: D2h INCK = 37.125 MHz: 91h									
16h	[7:0]	INCKSEL_ST2	B1h	INCK = 74.25 MHz: B1h INCK = 54 MHz: 80h INCK = 37.125 MHz: 50h									
18h	[7:0]	INCKSEL_ST3	40h	INCK = 74.25 MHz: 40h INCK = 54 MHz: 18h INCK = 37.125 MHz: 20h									
19h	[7:0]	INCKSEL_ST4	04h	INCK = 74.25 MHz: 04h INCK = 54 MHz: 03h INCK = 37.125 MHz: 02h									
1Bh	[7:0]	INCKSEL_ST5	3Ah	INCK = 74.25 MHz: 3Ah INCK = 54 MHz: 2Ah INCK = 37.125 MHz: 1Dh									
3Ch	[4:3]	HVMODE	0h	0h									All-pixel
D0h	[7:0]	VOPB_VBLK_HWIDTH	09A8h	VOPB effective area and V Blank width setting *Set the value of multiple of 8									
D1h	[4:0]												
D2h	[7:0]	FINFO_HWIDTH	09A8h	FINFO width setting *Set the value of multiple of 16									
D3h	[4:0]												
D4h	[7:0]	VMAX	0008AAh	*1	*2	*3	*4	*5	*6	*7	*8	*9	
D5h	[7:0]												
D6h	[7:0]												
D8h	[7:0]	HMAX	0167h	16Bh	2B2h	52Ch	1C2h	35Bh	673h	219h	403h	7BAh	FREQ = 0h
				2BEh	541h	A47h	36Ah	68Eh	CD5h	416h	7DAh	F62h	FREQ = 1h
D9h	[7:0]			122h	1D4h	37Bh	167h	244h	455h	190h	2B2h	52Ch	FREQ = 2h
				1DBh	388h	6E2h	24Eh	466h	896h	2BEh	541h	A47h	FREQ = 3h
DCh	[1:0]	FREQ	2h	0h / 1h / 2h / 3h									
E2h	[7:0]	GMRWT	06h	06h	04h	02h	06h	04h	02h	04h	02h	02h	FREQ = 0h
				04h	02h	02h	04h	02h	02h	02h	02h	02h	FREQ = 1h
				08h	06h	04h	06h	04h	02h	06h	04h	02h	FREQ = 2h
				06h	04h	02h	04h	02h	02h	04h	02h	02h	FREQ = 3h
E3h	[7:0]	GMTWT	28h	28h	16h	0Ch	20h	12h	0Ah	1Ch	0Eh	08h	FREQ = 0h
				16h	0Ch	06h	12h	0Ah	06h	0Eh	08h	04h	FREQ = 1h
				32h	20h	10h	28h	1Ah	0Eh	24h	16h	0Ch	FREQ = 2h
				1Eh	10h	0Ah	18h	0Eh	08h	16h	0Ch	06h	FREQ = 3h
E6h	[7:0]	GSDLY	12h	12h	0Ah	06h	0Eh	08h	04h	0Ch	06h	04h	FREQ = 0h
				0Ah	06h	04h	08h	04h	02h	06h	04h	02h	FREQ = 1h
				16h	0Eh	08h	12h	0Ch	06h	10h	0Ah	06h	FREQ = 2h
				0Eh	08h	04h	0Ch	06h	04h	0Ah	06h	04h	FREQ = 3h

Address	bit	Register name	Initial Value	Setting value									Remarks
				AD = 8 bit			AD = 10 bit			AD = 12 bit			
				8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	*7 [frame/s]	*8 [frame/s]	*9 [frame/s]	
				594 Mbps/ch									FREQ = 0h
				297 Mbps/ch									FREQ = 1h
				891 Mbps/ch									FREQ = 2h
				445.5 Mbps/ch									FREQ = 3h
Chip ID = 03h													
04h	[0]	FID0_ROIH1ON	0	The horizontal setting of FID0 ROI area (1, y) (y = 1 to 8) 0: Disable 1: Enable									
	[1]	FID0_ROIV1ON	0	The vertical setting of FID0 ROI area (x, 1) (x = 1 to 8) 0: Disable 1: Enable									
	[2]	FID0_ROIH2ON	0	The horizontal setting of FID0 ROI area (2, y) (y = 1 to 8) 0: Disable 1: Enable									
	[3]	FID0_ROIV2ON	0	The vertical setting of FID0 ROI area (x, 2) (x = 1 to 8) 0: Disable 1: Enable									
	[4]	FID0_ROIH3ON	0	The horizontal setting of FID0 ROI area (3, y) (y = 1 to 8) 0: Disable 1: Enable									
	[5]	FID0_ROIV3ON	0	The vertical setting of FID0 ROI area (x, 3) (x = 1 to 8) 0: Disable 1: Enable									
	[6]	FID0_ROIH4ON	0	The horizontal setting of FID0 ROI area (4, y) (y = 1 to 8) 0: Disable 1: Enable									
	[7]	FID0_ROIV4ON	0	The vertical setting of FID0 ROI area (x, 4) (x = 1 to 8) 0: Disable 1: Enable									
05h	[0]	FID0_ROIH5ON	0	The horizontal setting of FID0 ROI area (5, y) (y = 1 to 8) 0: Disable 1: Enable									
	[1]	FID0_ROIV5ON	0	The vertical setting of FID0 ROI area (x, 5) (x = 1 to 8) 0: Disable 1: Enable									
	[2]	FID0_ROIH6ON	0	The horizontal setting of FID0 ROI area (6, y) (y = 1 to 8) 0: Disable 1: Enable									
	[3]	FID0_ROIV6ON	0	The vertical setting of FID0 ROI area (x, 6) (x = 1 to 8) 0: Disable 1: Enable									
	[4]	FID0_ROIH7ON	0	The horizontal setting of FID0 ROI area (7, y) (y = 1 to 8) 0: Disable 1: Enable									
	[5]	FID0_ROIV7ON	0	The vertical setting of FID0 ROI area (x, 7) (x = 1 to 8) 0: Disable 1: Enable									
	[6]	FID0_ROIH8ON	0	The horizontal setting of FID0 ROI area (8, y) (y = 1 to 8) 0: Disable 1: Enable									
	[7]	FID0_ROIV8ON	0	The vertical setting of FID0 ROI area (x, 8) (x = 1 to 8) 0: Disable 1: Enable									
20h 21h	[7:0] [4:0]	FID0_ROIPH1	0000h	Designation of horizontal cropping position for FID0 on area (1, y) (y = 1 to 8) *Set the value of multiple of 8									
22h 23h	[7:0] [4:0]	FID0_ROIPV1	0000h	Designation of vertical cropping position for FID0 on area (x, 1) (x = 1 to 8) *Set the value of multiple of 8									
24h 25h	[7:0] [4:0]	FID0_ROIWH1	0000h	Designation of horizontal cropping size for FID0 on area (1, y) (y = 1 to 8) *Set the value of multiple of 8									
26h 27h	[7:0] [4:0]	FID0_ROIWV1	0000h	Designation of vertical cropping size for FID0 on area (x, 1) (x = 1 to 8) *Set the value of multiple of 8									
28h 29h	[7:0] [4:0]	FID0_ROIPH2	0000h	Designation of horizontal cropping position for FID0 on area (2, y) (y = 1 to 8) *Set the value of multiple of 8									
2Ah 2Bh	[7:0] [4:0]	FID0_ROIPV2	0000h	Designation of vertical cropping position for FID0 on area (x, 2) (x = 1 to 8) *Set the value of multiple of 8									
2Ch 2Dh	[7:0] [4:0]	FID0_ROIWH2	0000h	Designation of horizontal cropping size for FID0 on area (2, y) (y = 1 to 8) *Set the value of multiple of 8									
2Eh 2Fh	[7:0] [4:0]	FID0_ROIWV2	0000h	Designation of vertical cropping size for FID0 on area (x, 2) (x = 1 to 8) *Set the value of multiple of 8									
30h 31h	[7:0] [4:0]	FID0_ROIPH3	0000h	Designation of horizontal cropping position for FID0 on area (3, y) (y = 1 to 8) *Set the value of multiple of 8									
32h 33h	[7:0] [4:0]	FID0_ROIPV3	0000h	Designation of vertical cropping position for FID0 on area (x, 3) (x = 1 to 8) *Set the value of multiple of 8									
34h 35h	[7:0] [4:0]	FID0_ROIWH3	0000h	Designation of horizontal cropping size for FID0 on area (3, y) (y = 1 to 8) *Set the value of multiple of 8									
36h 37h	[7:0] [4:0]	FID0_ROIWV3	0000h	Designation of vertical cropping size for FID0 on area (x, 3) (x = 1 to 8) *Set the value of multiple of 8									

Address	bit	Register name	Initial Value	Setting value									Remarks
				AD = 8 bit			AD = 10 bit			AD = 12 bit			
				8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	*7 [frame/s]	*8 [frame/s]	*9 [frame/s]	
				594 Mbps/ch									FREQ = 0h
				297 Mbps/ch									FREQ = 1h
				891 Mbps/ch									FREQ = 2h
				445.5 Mbps/ch									FREQ = 3h
38h	[7:0]	FID0_ROIPH4	0000h	Designation of horizontal cropping position for FID0 on area (4, y) (y = 1 to 8) *Set the value of multiple of 8									
39h	[4:0]												
3Ah	[7:0]	FID0_ROIPV4	0000h	Designation of vertical cropping position for FID0 on area (x, 4) (x = 1 to 8) *Set the value of multiple of 8									
3Bh	[4:0]												
3Ch	[7:0]	FID0_ROIWH4	0000h	Designation of horizontal cropping size for FID0 on area (4, y) (y = 1 to 8) *Set the value of multiple of 8									
3Dh	[4:0]												
3Eh	[7:0]	FID0_ROIWV4	0000h	Designation of vertical cropping size for FID0 on area (x, 4) (x = 1 to 8) *Set the value of multiple of 8									
3Fh	[4:0]												
40h	[7:0]	FID0_ROIPH5	0000h	Designation of horizontal cropping position for FID0 on area (5, y) (y = 1 to 8) *Set the value of multiple of 8									
41h	[4:0]												
42h	[7:0]	FID0_ROIPV5	0000h	Designation of vertical cropping position for FID0 on area (x, 5) (x = 1 to 8) *Set the value of multiple of 8									
43h	[4:0]												
44h	[7:0]	FID0_ROIWH5	0000h	Designation of horizontal cropping size for FID0 on area (5, y) (y = 1 to 8) *Set the value of multiple of 8									
45h	[4:0]												
46h	[7:0]	FID0_ROIWV5	0000h	Designation of vertical cropping size for FID0 on area (x, 5) (x = 1 to 8) *Set the value of multiple of 8									
47h	[4:0]												
48h	[7:0]	FID0_ROIPH6	0000h	Designation of horizontal cropping position for FID0 on area (6, y) (y = 1 to 8) *Set the value of multiple of 8									
49h	[4:0]												
4Ah	[7:0]	FID0_ROIPV6	0000h	Designation of vertical cropping position for FID0 on area (x, 6) (x = 1 to 8) *Set the value of multiple of 8									
4Bh	[4:0]												
4Ch	[7:0]	FID0_ROIWH6	0000h	Designation of horizontal cropping size for FID0 on area (6, y) (y = 1 to 8) *Set the value of multiple of 8									
4Dh	[4:0]												
4Eh	[7:0]	FID0_ROIWV6	0000h	Designation of vertical cropping size for FID0 on area (x, 6) (x = 1 to 8) *Set the value of multiple of 8									
4Fh	[4:0]												
50h	[7:0]	FID0_ROIPH7	0000h	Designation of horizontal cropping position for FID0 on area (7, y) (y = 1 to 8) *Set the value of multiple of 8									
51h	[4:0]												
52h	[7:0]	FID0_ROIPV7	0000h	Designation of vertical cropping position for FID0 on area (x, 7) (x = 1 to 8) *Set the value of multiple of 8									
53h	[4:0]												
54h	[7:0]	FID0_ROIWH7	0000h	Designation of horizontal cropping size for FID0 on area (7, y) (y = 1 to 8) *Set the value of multiple of 8									
55h	[4:0]												
56h	[7:0]	FID0_ROIWV7	0000h	Designation of vertical cropping size for FID0 on area (x, 7) (x = 1 to 8) *Set the value of multiple of 8									
57h	[4:0]												
58h	[7:0]	FID0_ROIPH8	0000h	Designation of horizontal cropping position for FID0 on area (8, y) (y = 1 to 8) *Set the value of multiple of 8									
59h	[4:0]												
5Ah	[7:0]	FID0_ROIPV8	0000h	Designation of vertical cropping position for FID0 on area (x, 8) (x = 1 to 8) *Set the value of multiple of 8									
5Bh	[4:0]												
5Ch	[7:0]	FID0_ROIWH8	0000h	Designation of horizontal cropping size for FID0 on area (8, y) (y = 1 to 8) *Set the value of multiple of 8									
5Dh	[4:0]												
5Eh	[7:0]	FID0_ROIWV8	0000h	Designation of vertical cropping size for FID0 on area (x, 8) (x = 1 to 8) *Set the value of multiple of 8									
5Fh	[4:0]												
Chip ID = 04h													
00h	[5:4]	ADBIT	0h	2h			0h			1h			0: 10 bit 1: 12 bit 2: 8 bit
1Ch	[7:0]	INCKSEL_N0	80h	INCK = 74.25 MHz: 80h INCK = 54 MHz: 80h INCK = 37.125 MHz: 40h									
1Dh	[7:0]	INCKSEL_N1	05h	05h									
1Eh	[7:0]	INCKSEL_N2	E0h	INCK = 74.25 MHz: E0h INCK = 54 MHz: 34h INCK = 37.125 MHz: E0h									
1Fh	[7:0]	INCKSEL_N3	00h	INCK = 74.25 MHz: 00h INCK = 54 MHz: 01h INCK = 37.125 MHz: 00h									

Address	bit	Register name	Initial Value	Setting value									Remarks
				AD = 8 bit			AD = 10 bit			AD = 12 bit			
				8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	*7 [frame/s]	*8 [frame/s]	*9 [frame/s]	
				594 Mbps/ch									FREQ = 0h
				297 Mbps/ch									FREQ = 1h
				891 Mbps/ch									FREQ = 2h
				445.5 Mbps/ch									FREQ = 3h
24h	[7:0]	INCKSEL_D0	80h	INCK = 74.25 MHz: 80h INCK = 54 MHz: 80h INCK = 37.125 MHz: 40h									
25h	[7:0]	INCKSEL_D1	14h	14h									
26h	[7:0]	INCKSEL_D2	C0h	INCK = 74.25 MHz: 80h INCK = 54 MHz: B0h INCK = 37.125 MHz: 80h									FREQ = 0h FREQ = 1h
				INCK = 74.25 MHz: C0h INCK = 54 MHz: 08h INCK = 37.125 MHz: C0h									FREQ = 2h FREQ = 3h
27h	[7:0]	INCKSEL_D3	D0h	90h									FREQ = 0h
				A0h									FREQ = 1h
				INCK = 74.25 MHz: D0h INCK = 54 MHz: D1h INCK = 37.125 MHz: D0h									FREQ = 2h
				INCK = 74.25 MHz: E0h INCK = 54 MHz: E1h INCK = 37.125 MHz: E0h									FREQ = 3h
3Ch	[7:1]	LLBLANK	0Ch	0Ch									
3Dh	[0]												
Chip ID = 06h													
30h	[1:0]	ODBIT	0h	2h			0h			1h			0: 10 bit 1: 12 bit 2: 8 bit
44h	[3:0]	STBSLVS	1h	1h	N/A	N/A	1h	N/A	N/A	1h	N/A	N/A	8 ch SLVS
				N/A	2h	N/A	N/A	2h	N/A	N/A	2h	N/A	4 ch SLVS
				N/A	N/A	3h	N/A	N/A	3h	N/A	N/A	3h	2 ch SLVS
Chip ID = 07h													
21h	[7:0]		EDh	EDh									
46h	[7:0]		3Bh	3Bh									
B4h	[7:0]	BLKLEVEL	03Ch	00Fh			03Ch			0F0h			Recommended value
B5h	[3:0]												
Chip ID = 0Bh													
04h	[2:0]	LANESEL	0h	0h	N/A	N/A	0h	N/A	N/A	0h	N/A	N/A	8 ch SLVS
				N/A	2h	N/A	N/A	2h	N/A	N/A	2h	N/A	4 ch SLVS
				N/A	N/A	3h	N/A	N/A	3h	N/A	N/A	3h	2 ch SLVS

Restrictions on ROI mode

The register settings should satisfy following conditions:

* Do not designate area like be overlap.
ROIPH1 + ROIWH1 ≤ ROIPH2
ROIPH2 + ROIWH2 ≤ ROIPH3
ROIPH3 + ROIWH3 ≤ ROIPH4
…
ROIPH8 + ROIWH8 ≤ 2472d

ROIPV1 + ROIWV1 ≤ ROIPV2
ROIPV2 + ROIWV2 ≤ ROIPV3
ROIPV3 + ROIWV3 ≤ ROIPV4
…
ROIPV8 + ROIWV8 ≤ 2064d

* Set the ROIPHx and ROIWHx (x = 1 to 8) registers in multiple of 8.
* Set the ROIPVx and ROIWVx (x = 1 to 8) registers in multiple of 8.
* Set the VOPB_VBLK_HWIDTH register in multiple of 8.
* Set the FINFO_HWIDTH register in multiple of 16.

* The range of horizontal output width is as below.
10 / 12 bit mode
608d ≤ ROIWH1 + ROIWH2 + ROIWH3 + …. + ROIWH8 ≤ 2472d

8 bit mode
1200d ≤ ROIWH1 + ROIWH2 + ROIWH3 + …. + ROIWH8 ≤ 2472d

* The range of vertical output width is as below.
8 / 10 / 12 bit mode
8d ≤ ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 ≤ 2064d

* The range of output width for Vertical OB and Vertical blanking is as below.
16d ≤ VOPB_VBLK_HWIDTH ≤ 2472d

* The range of output width for Frame information is as below.
10 / 12 bit mode
608d ≤ FINFO_HWIDTH ≤ 2472d

8 bit mode
1200d ≤ FINFO_HWIDTH ≤ 2472d

Frame rate on ROI mode

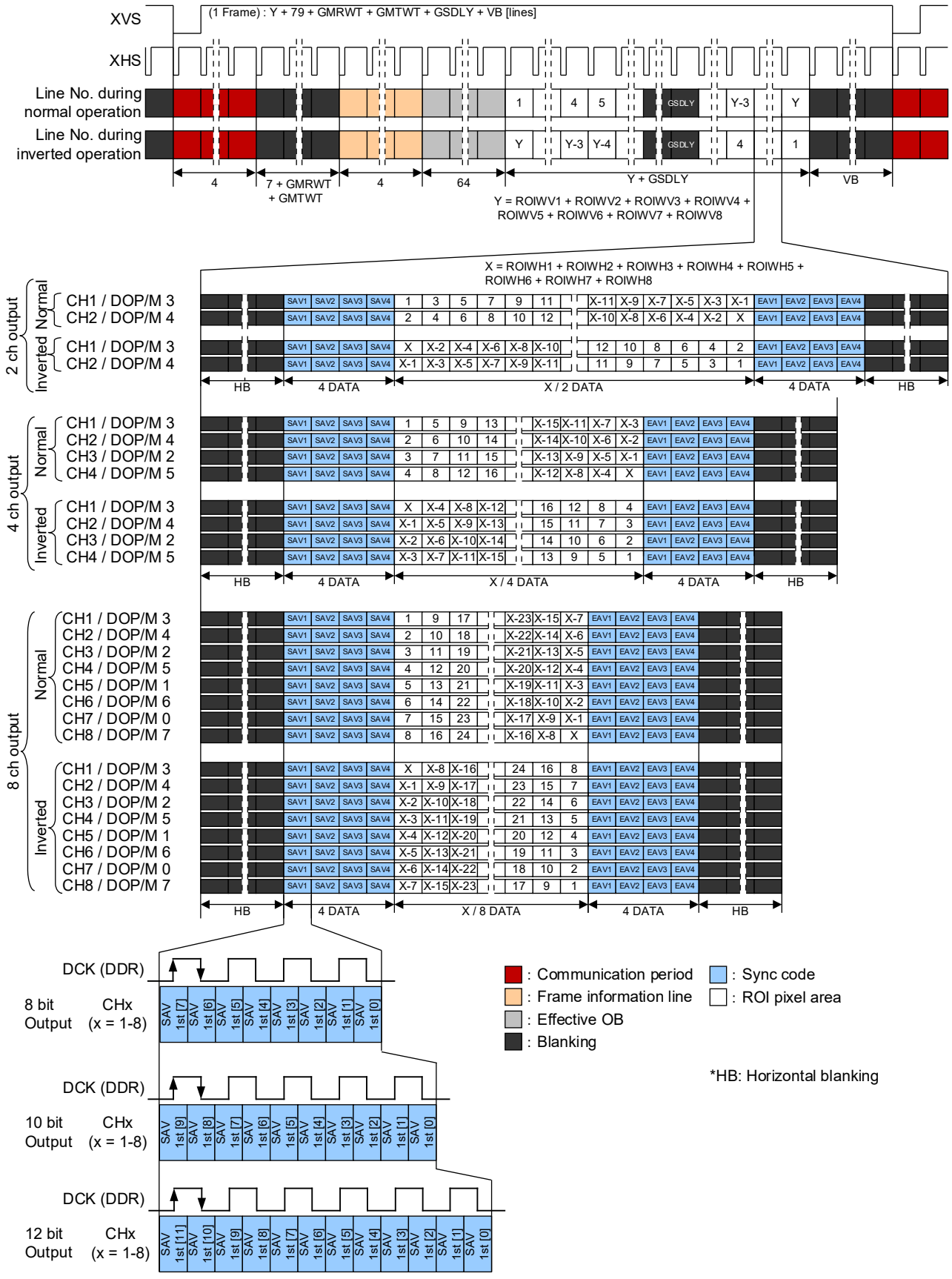
Frame rate [frame/s] = 1 / ((“Number of lines per frame” or VMAX) × (1 H period))

* Number of lines per frame or VMAX
  V_{TR} = ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 + GMRWT + GMTWT + GSDLY + 86
  For GMRWT, GMTWT and GSDLY, refer to the register list of each readout mode.
* 1 H period: Change according to the data rate settings and the number of SLVS channels.
  Calculate by number of INCK in 1 H and the period of INCK.

The example of ROI setting is shown below.
ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 = 640
ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 = 8 (minimum value)

Frame rate List of each setting

Register settings No. in register list	1 H period [μs]				Frame rate [frame/s]							
					Total number of ROI: 640 [line]				Total number of ROI: 8 [line]			
	FREQ 0h	FREQ 1h	FREQ 2h	FREQ 3h	FREQ = 0h	FREQ = 1h	FREQ = 2h	FREQ = 3h	FREQ = 0h	FREQ = 1h	FREQ = 2h	FREQ = 3h
*1	4.89	9.46	3.91	6.40	258.91	138.80	317.66	201.43	1294.59	813.60	1471.46	1085.52
*2	9.30	18.12	6.31	12.18	141.21	74.00	203.92	108.93	827.75	484.24	1086.67	673.23
*3	17.84	35.44	12.00	23.74	75.17	38.24	110.52	56.79	491.93	266.23	683.06	383.08
*4	6.07	11.78	4.84	7.95	212.08	112.37	261.80	164.29	1130.13	685.11	1309.01	939.16
*5	11.57	22.60	7.82	15.17	114.33	59.63	166.68	88.15	697.07	402.26	941.30	568.46
*6	22.24	44.25	14.94	29.61	60.61	30.71	89.50	45.64	408.84	217.33	577.17	312.78
*7	7.24	14.09	5.39	9.46	179.56	94.89	236.76	138.80	1001.94	611.93	1221.21	813.60
*8	13.84	27.08	9.30	18.12	96.65	49.91	141.21	74.00	623.25	342.03	827.75	484.24
*9	26.64	53.04	17.84	35.44	50.72	25.68	75.17	38.24	347.57	184.85	491.93	266.23



Drive Timing Chart for Serial Output in ROI Mode (SLVS output)

18.3.3. Overlap ROI mode

This Sensor has ROI function that signals are cut out and read out in multi arbitrary positions.
Cropping position can set maximum 8 areas, regarding effective pixel start position as origin (0, 0) in all pixel scan mode. Cropping is available from All-pixel scan mode and horizontal period are fixed to the value for this mode.
These cropped areas by horizontal cropping setting (ROI (1, y) to ROI (8, y)) are output with left justified and that extends the horizontal blanking period. In vertical cropping area (ROI (x, 1) to ROI (x, 8)), the number of image data is also output from cropping start line and the frame rate can be adjusted by changing the number of input XVS lines in slave mode or changing register VMAX in master mode.
One invalid frame is generated when the ROI area changing size or cropping address.
ROI image is shown in the figure below.
In case of Vertical / Horizontal 1/2 subsampling mode, this sensor doesn't support ROI mode.
The horizontal output width of Frame Information can be set by FINFO_HWIDTH register.
The horizontal output width of Vertical OB and Vertical blanking can be set by VOPB_VBLK_HWIDTH register.
This section is written in case of all-pixel scan mode for example on this document.

When SLVS output

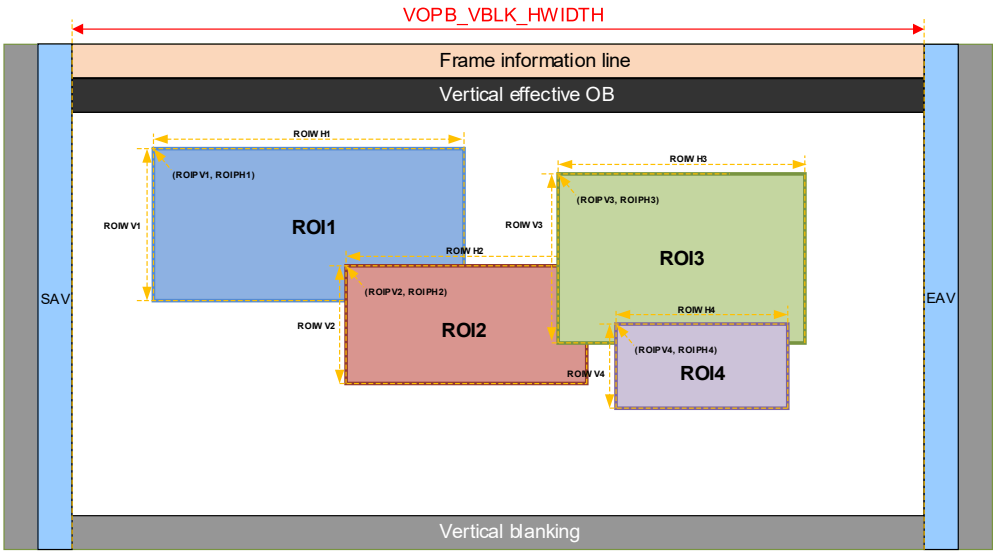
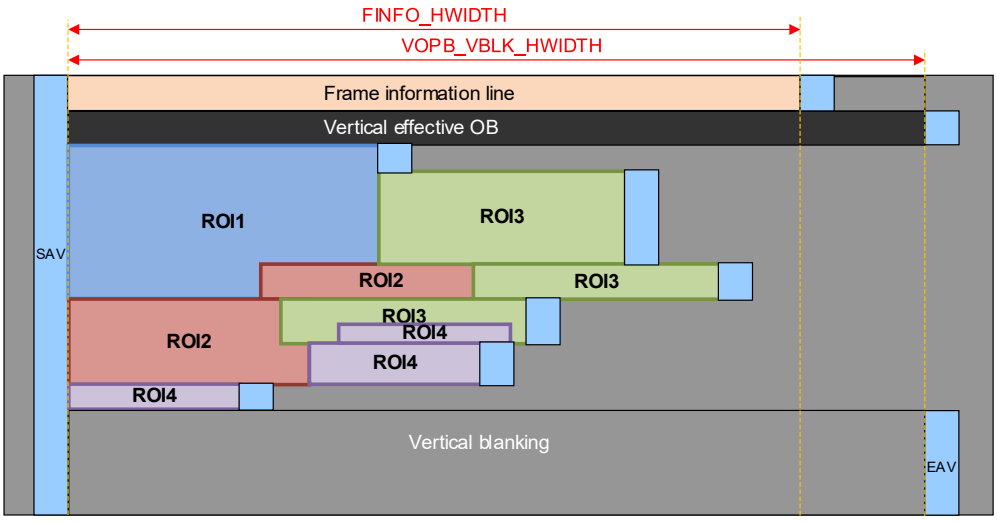


Image Drawing of Designated Areas in Overlap ROI Mode (SLVS output)



Details of Image Drawing (SLVS output)

Register List of Overlap ROI mode

Please set ROI mode to the settings other than the following.

Address	bit	Register name	Initial Value	Setting value									Remarks
				AD = 8 bit			AD = 10 bit			AD = 12 bit			
				8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	*7 [frame/s]	*8 [frame/s]	*9 [frame/s]	
				594 Mbps/ch									FREQ = 0h
				297 Mbps/ch									FREQ = 1h
				891 Mbps/ch									FREQ = 2h
				445.5 Mbps/ch									FREQ = 3h
Chip ID = 02h													
D0h	[7:0]	VOPB_VBLK_HWIDTH	09A8h	VOPB effective area and V Blank width setting *Set the value of multiple of 8									
D1h	[4:0]												
D2h	[7:0]	FINFO_HWIDTH	09A8h	FINFO width setting *Set the value of multiple of 16									
D3h	[4:0]												
Chip ID = 03h													
00h	[0]	ROI_MODE	0	1									

Restrictions on Overlap ROI mode

The register settings should satisfy following conditions:

ROIPH1 + ROIWH1 ≤ 2472d
ROIPH2 + ROIWH2 ≤ 2472d
ROIPH3 + ROIWH3 ≤ 2472d
…
ROIPH8 + ROIWH8 ≤ 2472d

ROIPV1 + ROIWV1 ≤ 2064d
ROIPV2 + ROIWV2 ≤ 2064d
ROIPV3 + ROIWV3 ≤ 2064d
…
ROIPV8 + ROIWV8 ≤ 2064d

* Set the ROIPHx and ROIWHx (x = 1 to 8) registers in multiple of 8.
* Set the ROIPVx and ROIWVx (x = 1 to 8) registers in multiple of 8.
* Set the VOPB_VBLK_HWIDTH register in multiple of 8.
* Set the FINFO_HWIDTH register in multiple of 16.

* The range of horizontal output width is as below.
 10 / 12 bit mode
  ROIWH1 ≥ 8d, ROIWH2 ≥ 8d, ROIWH3 ≥ 8d, …. ROIWH8 ≥ 8d
  “Minimum horizontal output width after ROI operation” ≥ 608d
  “Maximum horizontal output width after ROI operation” ≤ 2472d

 8 bit mode
  ROIWH1 ≥ 8d, ROIWH2 ≥ 8d, ROIWH3 ≥ 8d, …. ROIWH8 ≥ 8d
  “Minimum horizontal output width after ROI operation” ≥ 1200d
  “Maximum horizontal output width after ROI operation” ≤ 2472d

* The range of vertical output width is as below.
 8 / 10 / 12 bit mode
  ROIWV1 ≥ 8d, ROIWV2 ≥ 8d, ROIWV3 ≥ 8d, … ROIWV8 ≥ 8d
  “Minimum vertical output width after ROI operation” ≥ 8d
  “Maximum vertical output width after ROI operation” ≤ 2064d

* The range of output width for Vertical OB and Vertical blanking is as below.
  16d ≤ VOPB_VBLK_HWIDTH ≤ 2472d

* The range of output width for Frame information is as below.
 10 / 12 bit mode
  608d ≤ FINFO_HWIDTH ≤ 2472d

 8 bit mode
  1200d ≤ FINFO_HWIDTH ≤ 2472d

Frame rate on Overlap ROI mode

Frame rate [frame/s] = 1 / ((“Number of lines per frame” or VMAX) × (1 H period))
When the vertical output width is 640 or 8 lines, refer to ROI mode.

18.3.4. Vertical / Horizontal 1/2 Subsampling mode

By setting Vertical / Horizontal 1/2 Subsampling mode, the frame rate becomes faster than All-pixel mode.
The first pixel read out in this mode is Gb.

When SLVS output

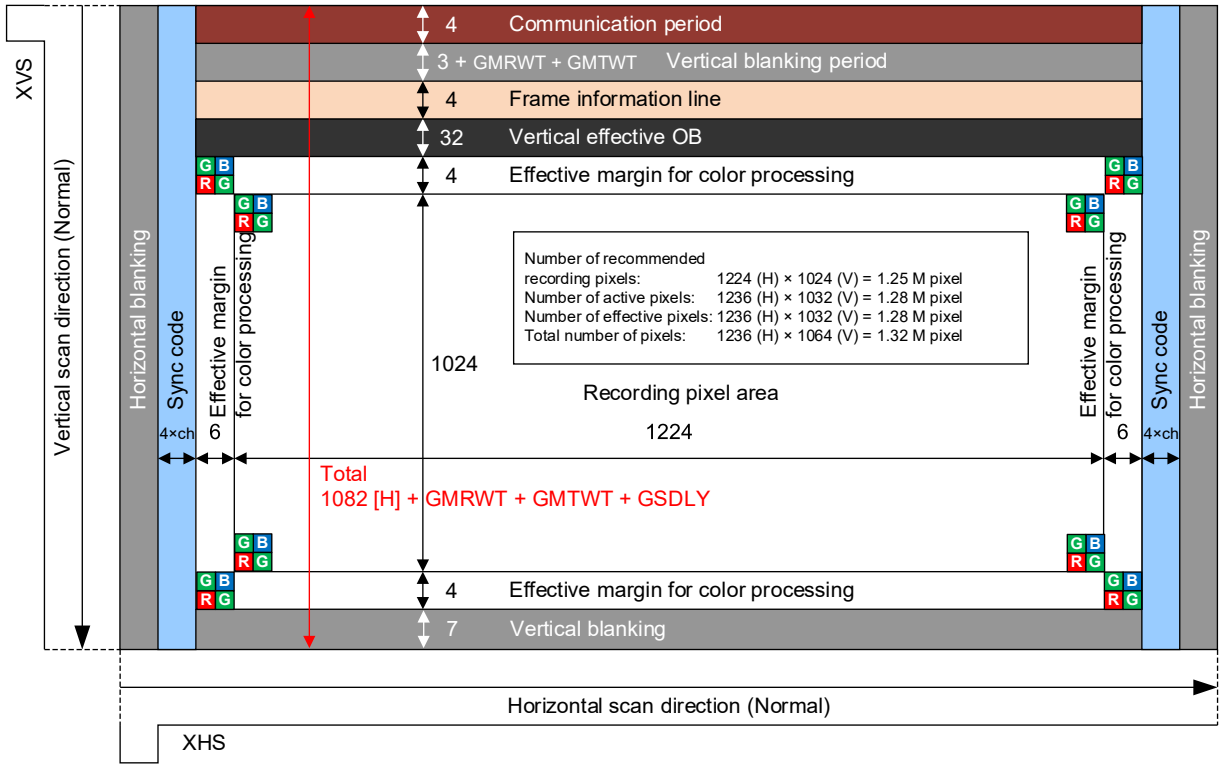
Register List of Vertical / Horizontal 1/2 subsampling mode

Please set All-pixel scan mode to the settings other than the following.

Address	bit	Register name	Initial Value	Setting value									Remarks
				AD = 8 bit			AD = 10 bit			AD = 12 bit			
				8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	
				220.3 [frame/s]	170.2 [frame/s]	93.9 [frame/s]	180.4 [frame/s]	138.3 [frame/s]	75.7 [frame/s]	162.8 [frame/s]	116.9 [frame/s]	63.8 [frame/s]	FREQ = 0h
				165.3 [frame/s]	91.2 [frame/s]	48.1 [frame/s]	134.3 [frame/s]	73.6 [frame/s]	38.7 [frame/s]	113.1 [frame/s]	61.9 [frame/s]	32.4 [frame/s]	FREQ = 1h
				220.3 [frame/s]	220.3 [frame/s]	136.8 [frame/s]	180.4 [frame/s]	180.4 [frame/s]	111.2 [frame/s]	162.8 [frame/s]	162.8 [frame/s]	93.9 [frame/s]	FREQ = 2h
				220.3 [frame/s]	133.2 [frame/s]	71.0 [frame/s]	180.4 [frame/s]	108.3 [frame/s]	57.4 [frame/s]	162.8 [frame/s]	91.2 [frame/s]	48.1 [frame/s]	FREQ = 3h
				594 Mbps/ch									FREQ = 0h
				297 Mbps/ch									FREQ = 1h
				891 Mbps/ch									FREQ = 2h
				445.5 Mbps/ch									FREQ = 3h
Chip ID = 02h													
14h	[7:0]	INCKSEL_ST0	0Ah	INCK = 74.25 MHz: 0Ah INCK = 54 MHz: F0h INCK = 37.125 MHz: 05h									
15h	[7:0]	INCKSEL_ST1	22h	INCK = 74.25 MHz: 22h INCK = 54 MHz: D2h INCK = 37.125 MHz: 91h									
16h	[7:0]	INCKSEL_ST2	B1h	INCK = 74.25 MHz: B1h INCK = 54 MHz: 80h INCK = 37.125 MHz: 50h									
18h	[7:0]	INCKSEL_ST3	40h	INCK = 74.25 MHz: 40h INCK = 54 MHz: 18h INCK = 37.125 MHz: 20h									
19h	[7:0]	INCKSEL_ST4	04h	INCK = 74.25 MHz: 04h INCK = 54 MHz: 03h INCK = 37.125 MHz: 02h									
1Bh	[7:0]	INCKSEL_ST5	3Ah	INCK = 74.25 MHz: 3Ah INCK = 54 MHz: 2Ah INCK = 37.125 MHz: 1Dh									
3Ch	[4:3]	HVMODE	0h	1h									1/2 Subsampling
D0h D1h	[7:0] [4:0]	VOPB_VBLK_HWIDTH	09A8h	04D4h									
D2h D3h	[7:0] [4:0]	FINFO_HWIDTH	09A8h	04D4h									
D4h	[7:0]	VMAX	0008AAh	48Ah	476h	45Ch	47Ah	46Ch	458h	474h	464h	450h	FREQ = 0h
D5h	[7:0]			474h	45Ch	44Eh	46Ah	456h	44Ah	464h	450h	448h	FREQ = 1h
D6h	[7:0]			48Ah	48Ah	46Ah	47Ah	47Ah	462h	474h	474h	45Ch	FREQ = 2h
				48Ah	46Ah	456h	47Ah	460h	450h	474h	45Ch	44Eh	FREQ = 3h
D8h	[7:0]	HMAX	0167h	122h	17Eh	2C4h	167h	1DAh	371h	190h	235h	41Eh	FREQ = 0h
				18Ah	2D9h	577h	1E9h	38Ch	6D1h	248h	43Eh	82Ah	FREQ = 1h
D9h	[7:0]			122h	122h	1E0h	167h	167h	253h	190h	190h	2C4h	FREQ = 2h
				122h	1EDh	3ADh	167h	264h	493h	190h	2D9h	577h	FREQ = 3h
DCh	[1:0]	FREQ	2h	0h / 1h / 2h / 3h									
E2h	[7:0]	GMRWT	06h	08h	06h	04h	06h	06h	04h	06h	04h	02h	FREQ = 0h
				06h	04h	02h	04h	04h	02h	04h	02h	02h	FREQ = 1h
				08h	08h	04h	06h	06h	04h	06h	06h	04h	FREQ = 2h
				08h	04h	04h	06h	04h	02h	06h	04h	02h	FREQ = 3h
E3h	[7:0]	GMTWT	28h	32h	26h	14h	28h	1Eh	12h	24h	1Ah	0Eh	FREQ = 0h
				24h	14h	0Ch	1Eh	10h	0Ah	1Ah	0Eh	08h	FREQ = 1h
				32h	32h	1Eh	28h	28h	18h	24h	24h	14h	FREQ = 2h
				32h	1Eh	10h	28h	18h	0Eh	24h	14h	0Ch	FREQ = 3h

Address	bit	Register name	Initial Value	Setting value									Remarks
				AD = 8 bit			AD = 10 bit			AD = 12 bit			
				8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	
				220.3 [frame/s]	170.2 [frame/s]	93.9 [frame/s]	180.4 [frame/s]	138.3 [frame/s]	75.7 [frame/s]	162.8 [frame/s]	116.9 [frame/s]	63.8 [frame/s]	FREQ = 0h
				165.3 [frame/s]	91.2 [frame/s]	48.1 [frame/s]	134.3 [frame/s]	73.6 [frame/s]	38.7 [frame/s]	113.1 [frame/s]	61.9 [frame/s]	32.4 [frame/s]	FREQ = 1h
				220.3 [frame/s]	220.3 [frame/s]	136.8 [frame/s]	180.4 [frame/s]	180.4 [frame/s]	111.2 [frame/s]	162.8 [frame/s]	162.8 [frame/s]	93.9 [frame/s]	FREQ = 2h
				220.3 [frame/s]	133.2 [frame/s]	71.0 [frame/s]	180.4 [frame/s]	108.3 [frame/s]	57.4 [frame/s]	162.8 [frame/s]	91.2 [frame/s]	48.1 [frame/s]	FREQ = 3h
				594 Mbps/ch									FREQ = 0h
				297 Mbps/ch									FREQ = 1h
				891 Mbps/ch									FREQ = 2h
				445.5 Mbps/ch									FREQ = 3h
E6h	[7:0]	GSDLY	12h	16h	10h	0Ah	12h	0Eh	08h	10h	0Ch	06h	FREQ = 0h
				10h	0Ah	06h	0Eh	08h	04h	0Ch	06h	04h	FREQ = 1h
				16h	16h	0Eh	12h	12h	0Ch	10h	10h	0Ah	FREQ = 2h
				16h	0Eh	08h	12h	0Ah	06h	10h	0Ah	06h	FREQ = 3h
Chip ID = 04h													
1Ch	[7:0]	INCKSEL_N0	80h	INCK = 74.25 MHz: 80h INCK = 54 MHz: 80h INCK = 37.125 MHz: 40h									
1Dh	[7:0]	INCKSEL_N1	05h	05h									
1Eh	[7:0]	INCKSEL_N2	E0h	INCK = 74.25 MHz: E0h INCK = 54 MHz: 34h INCK = 37.125 MHz: E0h									
1Fh	[7:0]	INCKSEL_N3	00h	INCK = 74.25 MHz: 00h INCK = 54 MHz: 01h INCK = 37.125 MHz: 00h									
24h	[7:0]	INCKSEL_D0	80h	INCK = 74.25 MHz: 80h INCK = 54 MHz: 80h INCK = 37.125 MHz: 40h									
25h	[7:0]	INCKSEL_D1	14h	14h									
26h	[7:0]	INCKSEL_D2	C0h	INCK = 74.25 MHz: 80h INCK = 54 MHz: B0h INCK = 37.125 MHz: 80h									FREQ = 0h FREQ = 1h
				INCK = 74.25 MHz: C0h INCK = 54 MHz: 08h INCK = 37.125 MHz: C0h									FREQ = 2h FREQ = 3h
27h	[7:0]	INCKSEL_D3	D0h	90h									FREQ = 0h
				A0h									FREQ = 1h
				INCK = 74.25 MHz: D0h INCK = 54 MHz: D1h INCK = 37.125 MHz: D0h									FREQ = 2h
				INCK = 74.25 MHz: E0h INCK = 54 MHz: E1h INCK = 37.125 MHz: E0h									FREQ = 3h
3Ch	[7:1]	LLBLANK	0Ch	08h									
3Dh	[0]												
3Eh	[7:2]		0Ch	08h									
Chip ID = 06h													
44h	[3:0]	STBSLVS	1h	1h	N/A	N/A	1h	N/A	N/A	1h	N/A	N/A	8 ch SLVS
				N/A	2h	N/A	N/A	2h	N/A	N/A	2h	N/A	4 ch SLVS
				N/A	N/A	3h	N/A	N/A	3h	N/A	N/A	3h	2 ch SLVS

Address	bit	Register name	Initial Value	Setting value									Remarks
				AD = 8 bit			AD = 10 bit			AD = 12 bit			
				8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	8 ch	4 ch	2 ch	
				220.3 [frame/s]	170.2 [frame/s]	93.9 [frame/s]	180.4 [frame/s]	138.3 [frame/s]	75.7 [frame/s]	162.8 [frame/s]	116.9 [frame/s]	63.8 [frame/s]	FREQ = 0h
				165.3 [frame/s]	91.2 [frame/s]	48.1 [frame/s]	134.3 [frame/s]	73.6 [frame/s]	38.7 [frame/s]	113.1 [frame/s]	61.9 [frame/s]	32.4 [frame/s]	FREQ = 1h
				220.3 [frame/s]	220.3 [frame/s]	136.8 [frame/s]	180.4 [frame/s]	180.4 [frame/s]	111.2 [frame/s]	162.8 [frame/s]	162.8 [frame/s]	93.9 [frame/s]	FREQ = 2h
				220.3 [frame/s]	133.2 [frame/s]	71.0 [frame/s]	180.4 [frame/s]	108.3 [frame/s]	57.4 [frame/s]	162.8 [frame/s]	91.2 [frame/s]	48.1 [frame/s]	FREQ = 3h
				594 Mbps/ch									FREQ = 0h
				297 Mbps/ch									FREQ = 1h
				891 Mbps/ch									FREQ = 2h
				445.5 Mbps/ch									FREQ = 3h
Chip ID = 07h													
21h	[7:0]		EDh	79h									
46h	[7:0]		3Bh	1Eh									
B4h	[7:0]	BLKLEVEL	03Ch	00Fh			03Ch			0F0h			Recommended value
B5h	[3:0]												
Chip ID = 0Bh													
04h	[2:0]	LANESEL	0h	0h	N/A	N/A	0h	N/A	N/A	0h	N/A	N/A	8 ch SLVS
				N/A	2h	N/A	N/A	2h	N/A	N/A	2h	N/A	4 ch SLVS
				N/A	N/A	3h	N/A	N/A	3h	N/A	N/A	3h	2 ch SLVS



Pixel Array Image Drawing in Vertical / Horizontal 1/2 subsampling mode
(SLVS output Shutter stabilization wait time is not included)

19. Description of Various Function

19.1. Standby mode

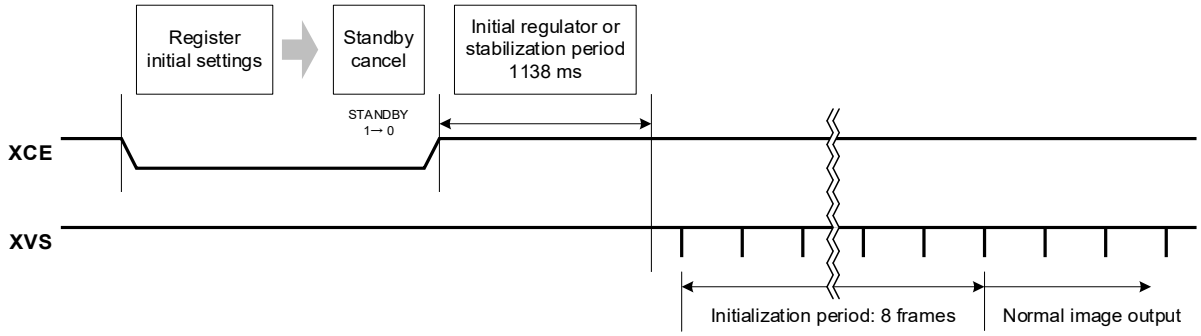
This sensor stops its operation and goes into standby mode which reduces the power consumption by writing “1” to the standby control register STANDBY. Standby mode is also established after power-on or other system reset operation.

Register List of Standby setting

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address ( ): I^2C	bit			
STANDBY [0]	02h	00h (3000h)	[0]	1	1: Standby 0: Operating	Register communication is executed even in standby mode.

The serial communication registers hold the previous values. However, the address registers transmitted in standby mode are overwritten. The serial communication block operates even in standby mode, so standby mode can be canceled by setting the STANDBY register to “0”. Some time is required for sensor internal circuit stabilization after standby mode is canceled. For details on the sequence of setting and cancel of standby mode, see the section of “Sensor Setting Flow”.

After standby mode is canceled, a normal image is output from the 9 frames after internal regulator stabilization (1138 ms or more).



Sequence from Standby Cancel to Stable Image Output

19.2. Slave Mode and Master Mode

The sensor can be switched between slave mode and master mode.
The switching is made by the XMASTER pin. Establish the XMASTER pin status before canceling the system reset. (Do not switch this pin status during operation.)

Slave Mode (XMASTER = 1h)

Input a vertical sync signal to XVS and input a horizontal sync signal to XHS. For sync signal interval, input data lines to output for vertical sync signal and 1 H period designated in each operating mode for horizontal sync signal. See the section of "Readout Drive Modes" for the number of output data line and 1 H period.
In this sensor, the low-power consumption function is always ON, so be sure to set HMAX [15:0] even in slave mode. The setting value of HMAX [15:0] can be calculated using the following.

HMAX [15:0] = “Number of INCK in 1H” × 74.25 / INCK Frequency

Master Mode (XMASTER = 0h)

Set “XMSTA = 0” in order to start the operation. In addition, set the count number of sync signal in vertical direction by the VMAX [23:0] register and the clock number in horizontal direction by the HMAX [15:0] register. See the description of operation mode for details of the section of “Readout Drive Modes”.
In master mode, it is possible to output horizontal / vertical sync signals from XHS pin / XVS pin by setting register: SYNCSEL [1:0].

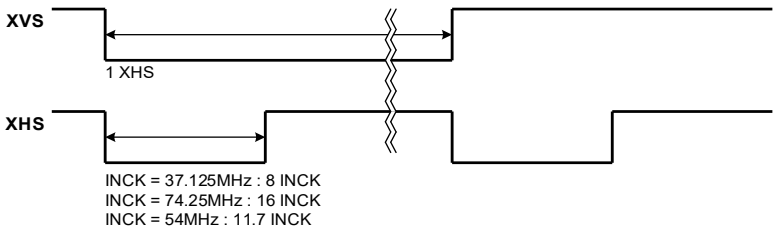
Pin Processing

Pin name	Pin processing	Operation mode	Remarks
XMASTER pin	Low fixed	Master mode	High: OV_{DD} Low: GND
	High fixed	Slave mode	

Register List of Slave Mode and Master Mode

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address ( ): I^2C	Bit			
XMSTA [0]	02h	10h (3010h)	[0]	1	1: Master operation ready (Initial value) 0: Master operation start	The master operation starts by setting 0.
VMAX [23:0]		D4h (30D4h)	[7:0]	0008AAh	See the item of each drive mode	Line number per frame designated (Master mode and Slave mode common setting.)
		D5h (30D5h)	[7:0]			
		D6h (30D6h)	[7:0]			
HMAX [15:0]		D8h (30D8h)	[7:0]	0167h	See the item of each drive mode	Clock number per line designated (Master mode and Slave mode common setting.)
		D9h (30D9h)	[7:0]			
SYNCSEL [1:0]	06h	3Ch (343Ch)	[5:4]	0h	0h: Normal Output 3h: Hi-Z	XHS, XVS pin setting in Master mode

XVS / XHS Output in Master Mode



The XVS and XHS are output in timing that set “XMSTA = 0” after standby is released. The XVS and XHS are output asynchronous with other input or output signals. In addition, the output signals are output with an undefined latency time (system delay) relative to the XHS. Therefore, refer to the sync codes output from the sensor and perform synchronization.

19.3. Gain Adjustment Function

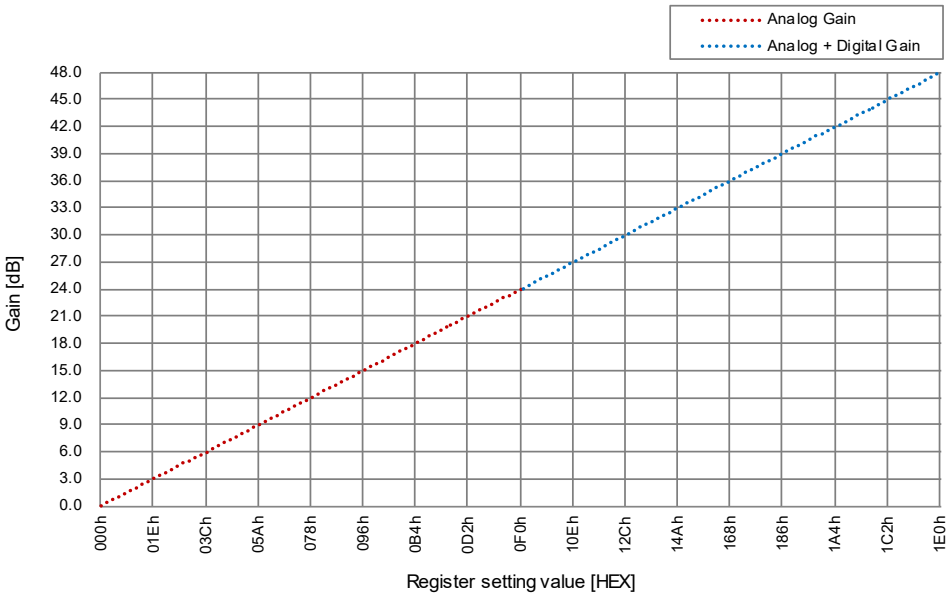
PGC

The Programmable Gain Control (PGC) of this device consists of the analog block and digital block.
The total of analog gain and digital gain can be set up to 48 dB by the GAIN [8:0] register setting.

The value which is ten times the gain is set to register. (0.1 dB step)

Example)
When set to 6 dB:

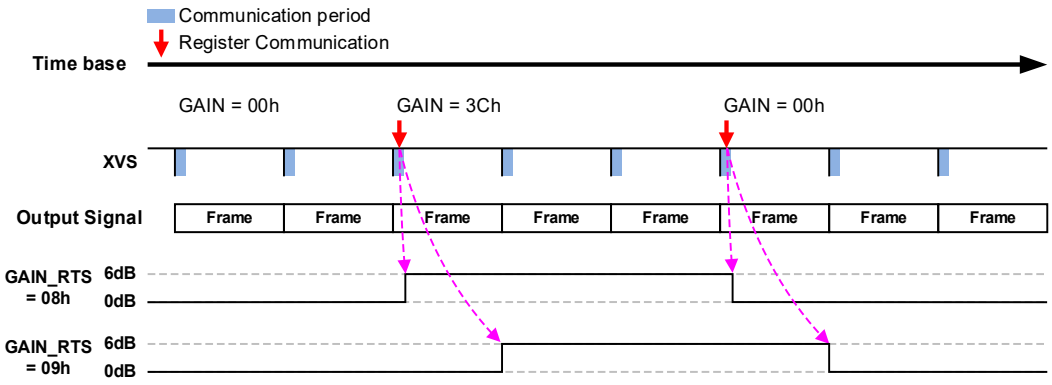
6 × 10 = 60d, GAIN = 03Ch



Register List of Gain setting

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address ( ): I²C	bit		Setting range	
GAIN_RTS [7:0]	07h	02h (3502h)	[7:0]	00h	08h or 09h	08h: Gain reflect at the frame 09h: Gain reflect at the next frame
GAIN [8:0]		14h (3514h)	[7:0]	000h	000h to 1E0h (0d to 480d)	Setting value: Gain [dB] × 10
		15h (3515h)	[0]			

Gain Reflection Timing is changed by the set value of the GAIN_RTS [7:0] register as shown below.



Gain Reflection Timing

19.4. Black Level Adjustment Function

The black level offset (offset variable range: 000h to FFFh) can be added relative to the data in which the digital gain modulation was performed by the BLKLEVEL [11:0] register. When the BLKLEVEL [11:0] setting is increased by 1 LSB, the black level is increased by 1 LSB.

* Use with values shown below is recommended.
  8 bit output: 00Fh (15d)
  10 bit output: 03Ch (60d)
  12 bit output: 0F0h (240d)

Register List of Black level adjustment

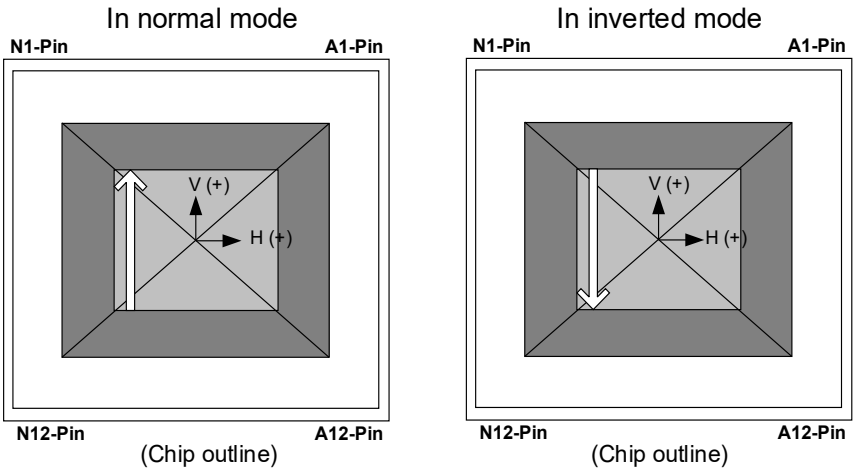
Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I^2C	bit		
BLKLEVEL [11:0]	07h	B4h (35B4h)	[7:0]	03Ch	000h to FFFh
		B5h (35B5h)	[3:0]		

19.5. Horizontal / Vertical Normal Operation and Inverted Operation

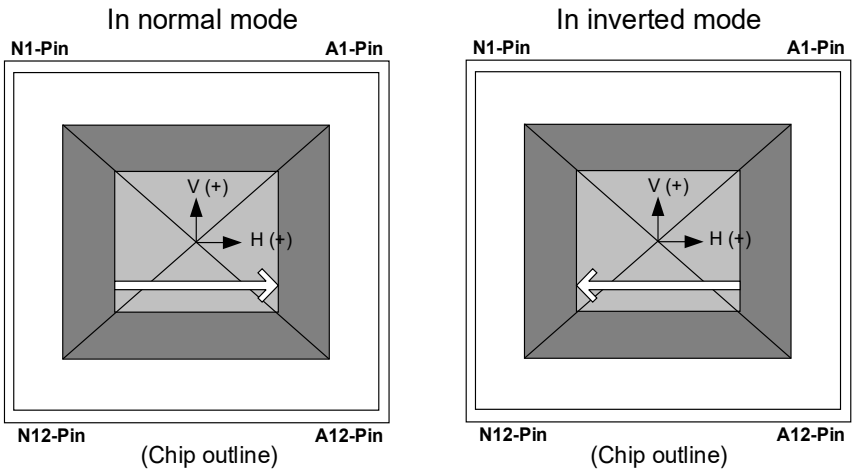
The sensor readout direction (normal / inverted) in vertical direction can be switched by the VREVERSE register setting and sensor readout direction (normal / inverted) in horizontal direction can be switched by the HREVERSE register setting. See the section of “Readout Drive Modes” for the order of readout lines in normal and inverted modes.
One invalid frame is generated when reading immediately after the readout vertical direction change in order to switch the normal operation and inversion between frames.

Register List of Readout Drive Direction setting

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
VREVERSE [0]	04h	04h (3204h)	[0]	0	0: Normal (Initial value) 1: Inverted
HREVERSE [0]			[1]	0	0: Normal (Initial value) 1: Inverted



Normal and Inverted Drive Outline in Vertical Direction (TOP VIEW)



Normal and Inverted Drive Outline in Horizontal Direction (TOP VIEW)

19.6. Shutter and Exposure Time Settings

This sensor has a global shutter function that integrates to all line collectively by using memory in each pixel. This sensor has a variable electronic shutter function that can control the exposure time in line units for adjust the exposure time. This sensor transferred signal to memory in pixel after the exposure (memory transfer), then this sensor performs output in which readout operation is performed sequentially for each line in sync with the XHS signal. This sensor has trigger mode that can be controlled exposure start timing and memory transfer timing by trigger.

Note) For exposure time control, an image which reflects the setting is output from the frame after the setting changes.

In this item, the shutter operation and storage time are shown as in the figure below with the time sequence on the horizontal axis and the vertical address on the vertical axis. For simplification, shutter and readout operation are noted in line units.

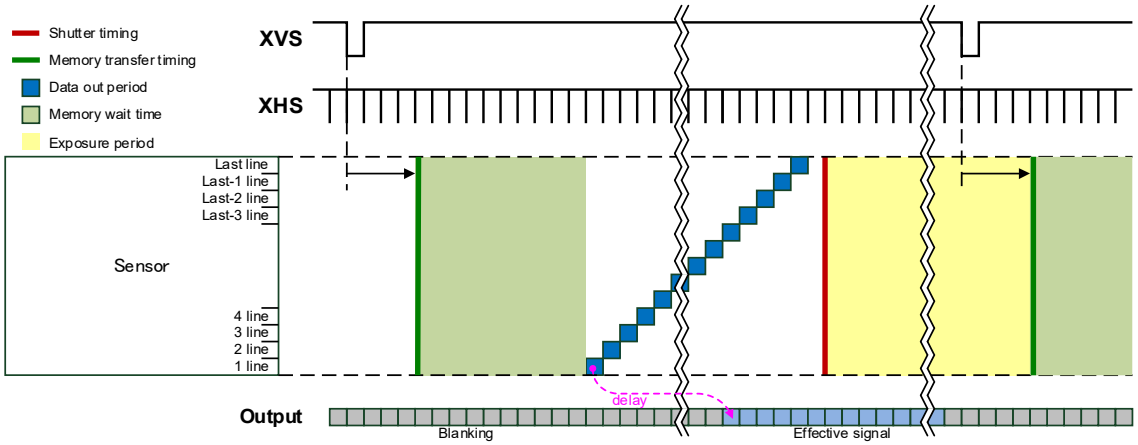


Image Drawing of Global Shutter (Normal mode) Operation

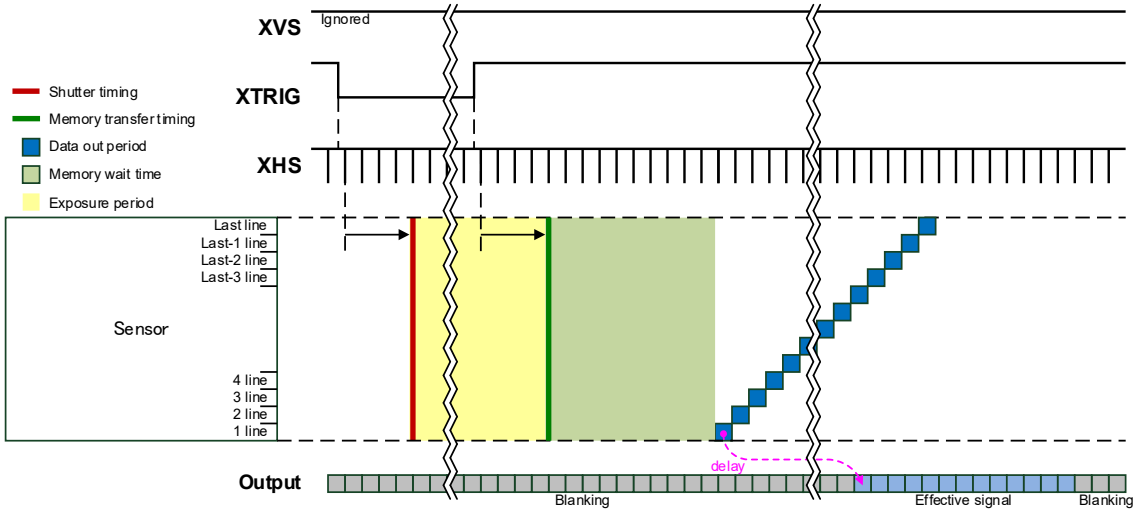


Image Drawing of Global Shutter (Sequential Trigger mode) Operation

19.6.1. Global Shutter (Normal Mode) Operation

The exposure time can be controlled by varying the electronic shutter timing. In the electronic shutter settings, the exposure time is controlled by the SHS [23:0] register. For setting value of SHS [23:0], see the table “List of Exposure Setting”. When the sensor is operating in slave mode, the number of lines per frame is determined by the XVS interval (number of lines), using the input XHS interval as the line unit. When the sensor is operating in master mode, the number of lines per frame is determined by the VMAX [23:0] register. The number of lines per frame differs according to the readout mode.
When XVS is input at intervals shorter than the recommended setting value of VMAX [23:0] in each readout mode, interrupt operation is performed.

Calculation Formula of Exposure Time

Exposure time [µs] = (1 H period [µs]) × (Number of lines per frame - SHS) + 2.47 [µs][*1]
[*1]: Exposure time error (t_{OFFSET})

Register List of Shutter setting

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
VMAX [23:0]	02h	D4h (30D4h)	[7:0]	0008AAh	Set the number of lines per frame (only in master mode)
		D5h (30D5h)	[7:0]		
		D6h (30D6h)	[7:0]		
GMRWT [7:0]		E2h (30E2h)	[7:0]	06h	For setting, refer to the register list of each readout mode
GMTWT [7:0]		E3h (30E3h)	[7:0]	28h	For setting, refer to the register list of each readout mode
GSDLY [7:0]		E6h (30E6h)	[7:0]	12h	For setting, refer to the register list of each readout mode
VINT_EN_NOR [0]	04h	3Eh (323Eh)	[1]	1	Setting of Interrupt mode in Normal Mode 0: V interrupt is disable 1: V interrupt is enable
SHS [23:0]		40h (3240h)	[7:0]	000070h	Sets the shutter sweep time. (memory wait time (GMTWT value) +4) to (Number of lines per frame - 1)
		41h (3241h)	[7:0]		
		42h (3242h)	[7:0]		

When set VMAX [23:0] to a number of V lines or more than that noted for each operating mode, the imaging characteristics are not guaranteed.

List of Exposure Setting

Drive mode	memory transfer stabilization wait time [H]	Number of lines per frame [DEC]	SHS Setting value [DEC]	Exposure Setting value [H]	AD 12 bit, FREQ 0, 8 ch output (Maximum frame rate)	
					Frame rate [frame/s]	Actual exposure [ms][*3]
All-pixel	36 (GMTWT[*1])	2208 (VMAX)	2207	1	84.0	0.008
			2206	2		0.013
			…	…		…
			41	2167		11.677
			40	2168		11.682
1/2 subsampling	36 (GMTWT[*1])	1140 (VMAX)	1139	1	162.8	0.008
			1138	2		0.013
			…	…		…
			41	1099		5.923
			40	1100		5.928
ROI Overlap ROI	All-pixel (GMTWT[*1])	V_{TR}[*2]	V_{TR}-1	1	[*2]	0.008
			V_{TR}-2	2		0.013
			…	…		…
			41	V_{TR}-41		[*4]
			40	V_{TR}-40		

[*1] For GMTWT, refer to the register list of each readout mode.
[*2] V_{TR} and the frame rate, refer to the section “ROI mode” in “Readout Drive Modes”.
[*3] INCK frequency is input by typical value, and t_{OFFSET} (2.47 [μs]) is included.
[*4] Conform to the calculation formula of exposure time. (Number of lines per frame = V_{TR})

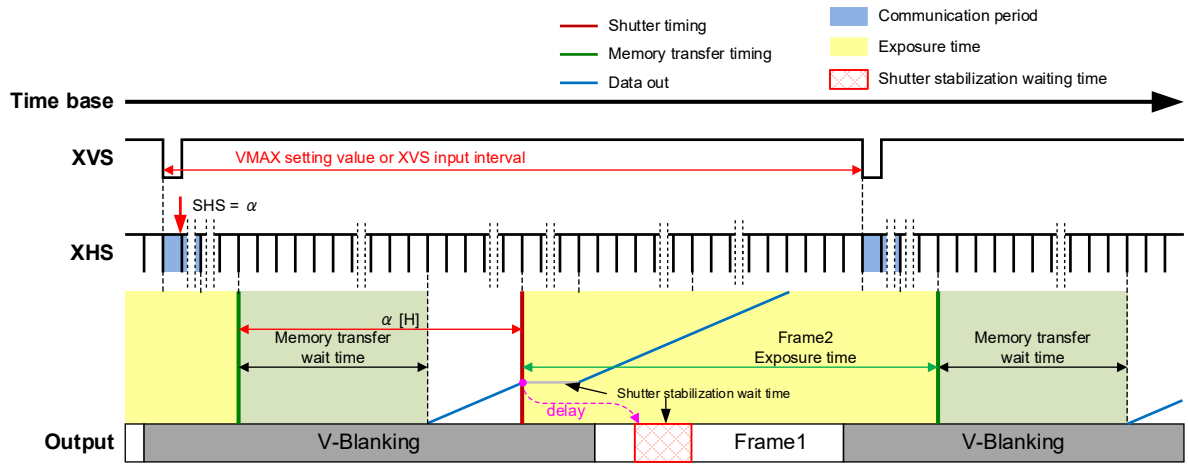


Image Drawing of Global Shutter (Normal Mode)

Interrupt Operation

In case of “VINT_EN_NOR = 1”, the image drawing when the interrupt operation is generated is shown below. When the next XVS is input during read of the frame (Frame 1 in the figure below), Frame 1 becomes an invalid frame. XVS input timing of interrupt generating corresponds to recommended setting value of VMAX [23:0] in each readout mode.
In case of "VINT_EN_NOR = 0", XVS input at intervals shorter than the recommended setting value of VMAX [23:0] is invalid.

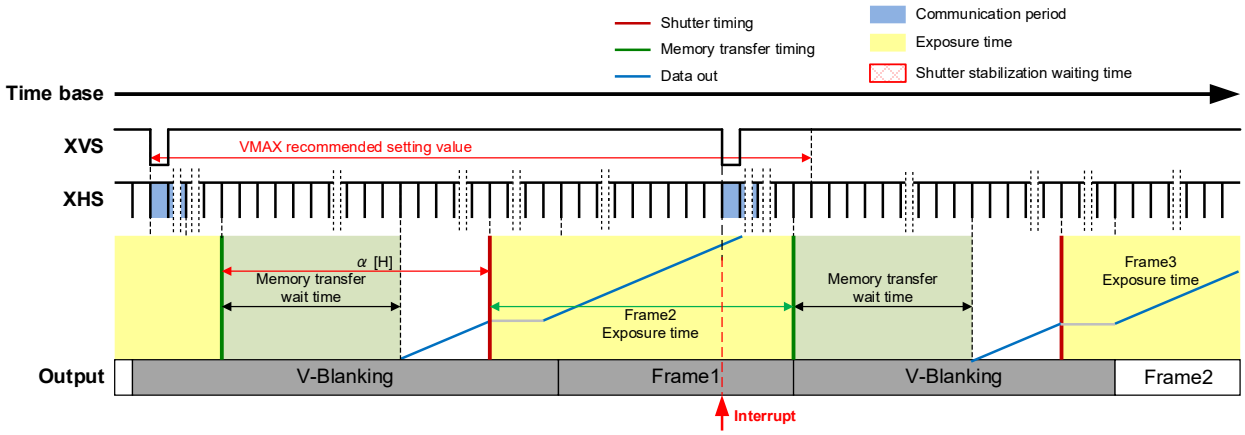


Image Drawing of Interrupt Operation in Global Shutter (Normal Mode)

19.6.2. Global Shutter (Sequential Trigger Mode) Operation

The exposure time can be controlled by varying the pulse width that is input to XTRIG1 pin. The pulse width designated in XHS unit [H]. For the transition from normal mode to Sequential trigger mode, set 1 to the register TRIGMODE [2:0]. The XVS input signal is ignored during Sequential trigger mode operating. In case of inputting trigger continuously, there are period which prohibit the trigger rise input (t_{TGPD}) and fall input (t_{TGES}) based on the previous trigger rise.
When the trigger rise is input before the rise input prohibited period (t_{TGPD}), interrupt operation starts.
This function is slave mode only. The number of lines per frame differs according to the operating mode.
XTRIG2 pin is set Open (Hi-Z) or fixed to High after power-on sequence.

Calculation Formula of Exposure Time

Exposure time [µs] = (1 H period [µs]) × (XTRIG low level pulse width [H][*2]) + 2.47 [µs][*1]
[*1]: Exposure time error (t_{OFFSET})
[*2]: Low level pulse width is counted by XHS pulse.

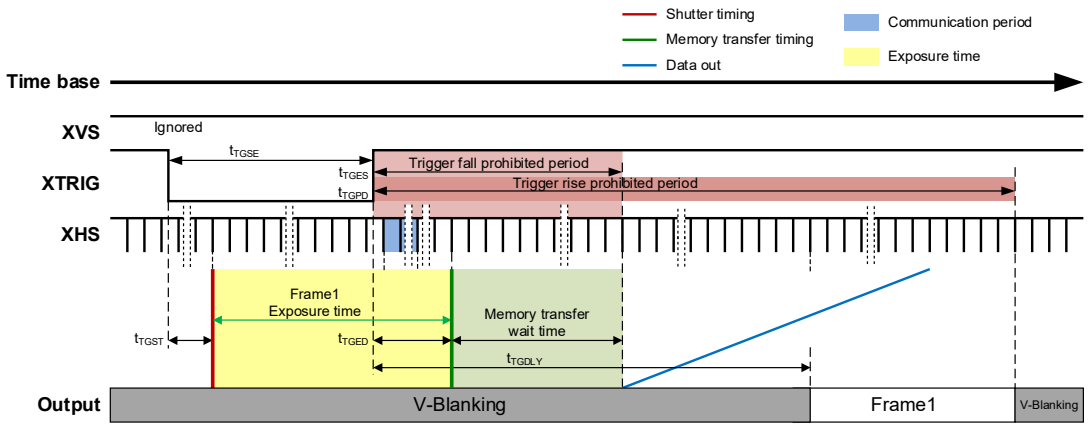
Register List of shutter setting

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
XMSTA	02h	10h (3010h)	[0]	1	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop
VINT_EN [0]	04h	3Eh (323Eh)	[0]	1	Setting of Interrupt mode in Trigger Mode 0: V interrupt is disable 1: V interrupt is enable
TRIGMODE [2:0]	06h	00h (3400h)	[2:0]	0h	Global shutter mode setting 0h: Normal mode 1h: Sequential Trigger mode 2h: Fast Trigger mode
TRIGTIMING [1:0]	06h	00h (3400h)	[4:3]	0h	Trigger mode setting 0h: Normal mode 1h: Trigger mode Others: Setting prohibited

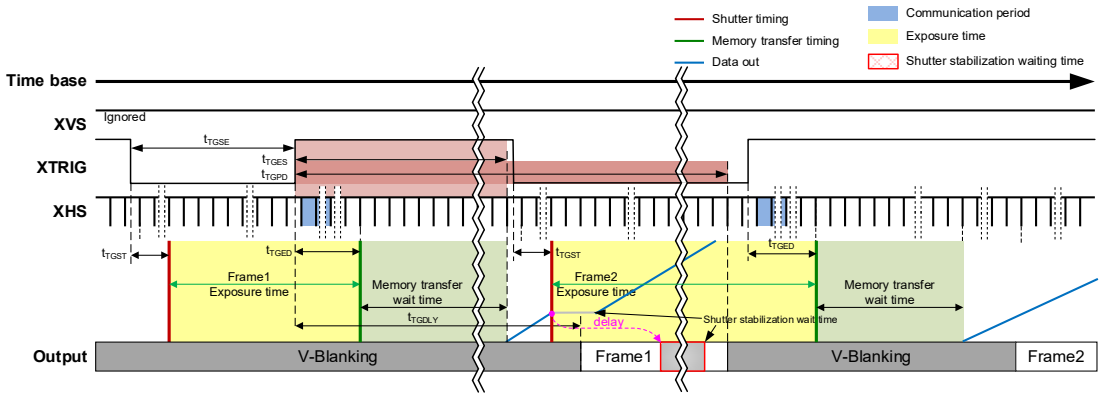
Parameter List of Global Shutter (Sequential Trigger Mode)

Item	Symbol	Min.	Typ.	Max.	Unit
Integration start delay (All-pixel / ROI / 1/2 Subsampling)	t_{TGST}	4 + GMRWT[*1]	—	5 + GMRWT[*1]	H
Integration end delay (All-pixel / ROI / 1/2 Subsampling)	t_{TGED}	4 + GMRWT[*1] + t_{OFFSET}	—	5 + GMRWT[*1] + t_{OFFSET}	H
Pulse width	t_{TGSE}	1	—	—	H
Next trigger fall prohibited period (All-pixel, ROI, 1/2 Subsampling)	t_{TGES}	5 + GMRWT[*1] + GMTWT[*1]	—	—	H
Next trigger rise prohibited period (All-pixel, 1/2 Subsampling)	t_{TGPD}	VMAX	—	—	H
Next trigger rise prohibited period (ROI)		V_{TR}[*2]	—	—	
Data output delay (All-pixel / ROI)	t_{TGDLY}	—	15 + GMRWT[*1] + GMTWT[*1]	—	H
Data output delay (1/2 Subsampling)			11 + GMRWT[*1] + GMTWT[*1]		

[*1] For GMRWT, GMTWT refer to the register list of each readout mode.
[*2] V_{TR} (See the section “ROI mode” in “Readout Drive Modes”)



Single shutter Image Drawing of Global Shutter (Sequential Trigger Mode)



Multi shutter image Drawing of Global Shutter (Sequential Trigger Mode)

Interrupt Operation

In case of “VINT_EN = 1”, the image drawing when the interrupt operation is generated is shown below. When the trigger is raised again and the next frame is output during read of the frame for which read was started by a trigger rise (Frame 1 in the figure below), Frame 1 becomes an invalid frame. Trigger timing of interrupt generating corresponds to t_{TGPD} in Parameter List of Global Shutter (Trigger Mode)
In case of “VINT_EN = 0”, both of the rising edge and the falling edge of the trigger signal are ignored in t_{TGPD} (Prohibit period).

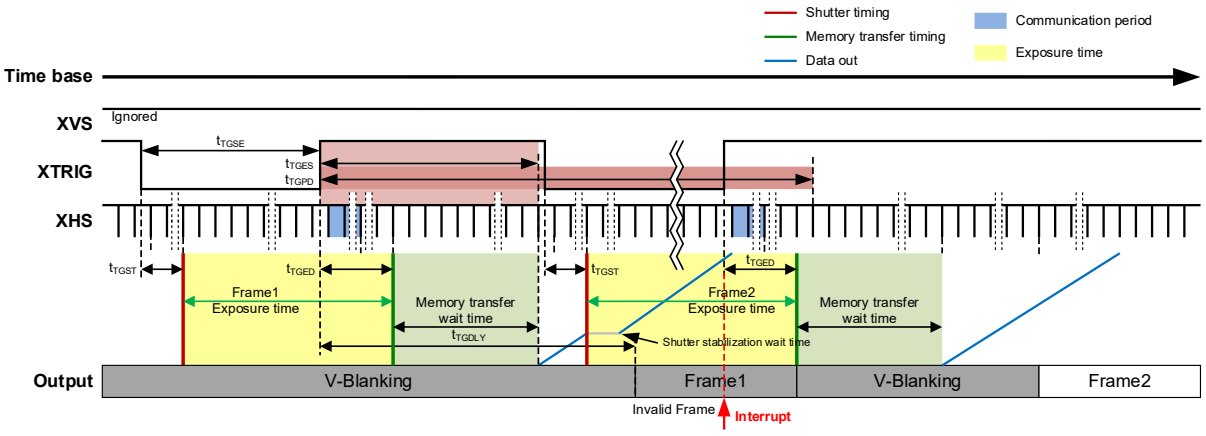


Image Drawing of Interrupt Operation in Global Shutter (Sequential Trigger Mode)

19.6.3. Global Shutter (Fast Trigger Mode) Operation

Fast trigger mode is the trigger mode that starts exposure at fall of XTRIG1 immediately.
In the Fast trigger mode, set the register TRIGMODE [2:0] to 2h at standby state, and then release standby. In the Fast trigger mode, the image size can not be changed during the operation.
This mode supports Master mode only.
XTRIG2 pin is set Open (Hi-Z) or fixed to High after power-on sequence.

Calculation Formula of Exposure Time

Exposure time [µs] = (XTRIG low level pulse width [µs]) + (GMRWT [H] × 1 H period [µs]) + 2.53 [µs][*1]
[*1]: Exposure time error (t_{OFFSET})

Register List of shutter setting

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I^2C	bit		
XMSTA [0]	02h	10h (3010h)	[0]	1	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop
TRIGMODE [2:0]	06h	00h (3400h)	[2:0]	0h	Global shutter mode setting 0h: Normal mode 1h: Sequential Trigger mode 2h: Fast Trigger mode
TRIGTIMING [1:0]	06h	00h (3400h)	[4:3]	0h	Trigger mode setting 0h: Normal mode 1h: Trigger mode Others: Setting prohibited

Parameter List of Global Shutter (Fast Trigger Mode)

Item	Symbol	Min.	Typ.	Max.	Unit
Integration start delay (All-pixel / ROI / 1/2 Subsampling)	t_{TGST}	—	—	0.1	µs
Integration end delay (All-pixel / ROI / 1/2 Subsampling)	t_{TGED}	—	—	0.1 + GMRWT[*1] + t_{OFFSET}	µs
Pulse width	t_{TGSE}	0.05	—	—	µs
Next trigger rise / fall prohibited period (All-pixel, 1/2 Subsampling)	t_{TGPD}	VMAX	—	—	H
Next trigger rise / fall prohibited period (ROI)		V_{TR}[*2]	—	—	
Data output delay (All-pixel / ROI)	t_{TGDLY}	—	11 + GMRWT[*1] + GMTWT[*1]	—	H
Data output delay (1/2 Subsampling)			7 + GMRWT[*1] + GMTWT[*1]		

[*1] For GMRWT, GMTWT refer to the register list of each readout mode.
[*2] V_{TR} (see the section “ROI mode” in “Readout Drive Modes”).

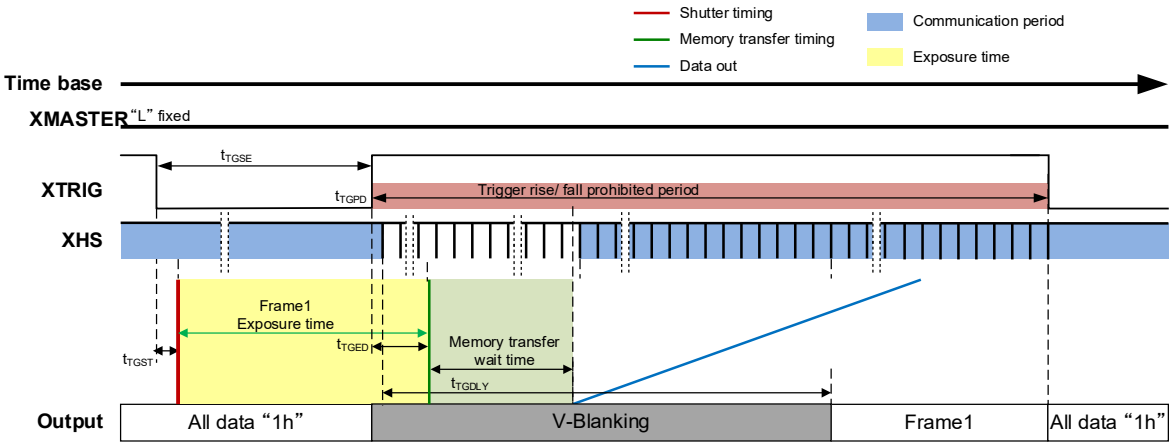


Image Drawing of Global Shutter (Fast Trigger Mode) (4-wire)

19.6.4. Mode Transitions of Global Shutter Operation

The sensor can be switched between normal mode and trigger mode in global shutter operation by setting the register TRIGMODE [2:0]. The sensor will transition to normal mode or trigger mode “GMRWT [7:0] (H) + GMTWT [7:0] (H)” after the register TRIGMODE [2:0] is set.
(The XVS and XTRIG input during transition are prohibited.)
In case of Fast Trigger mode, the mode transition must be done via sensor standby.

Transition from Normal Mode to Sequential Trigger Mode

The sensor will transition from normal mode to Sequential trigger mode after setting “TRIGMODE [2:0] = 1h”. The XVS input is ignored after transition to trigger mode. Trigger input is prohibited for a “GMRWT [7:0] (H) + GMTWT [7:0] (H)” period after the register TRIGMODE [2:0] is set. When TRIGMODE [2:0] is set during data read, read operation is stopped and that frame becomes an invalid frame.

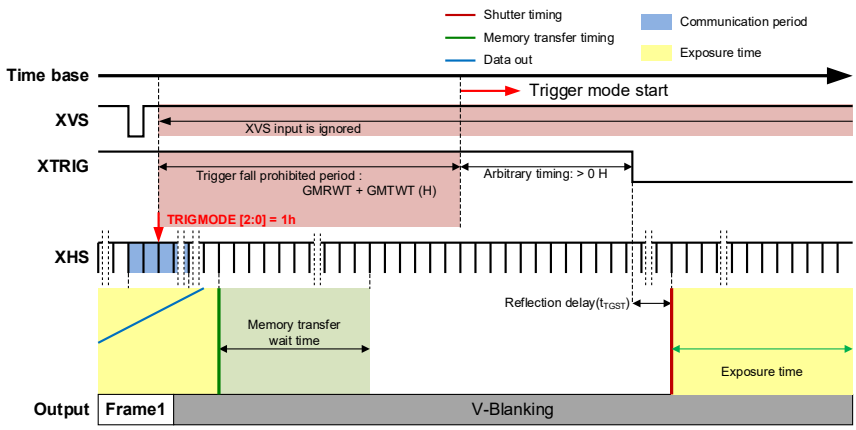


Image Drawing of Transition from Normal Mode to Sequential Trigger Mode

Transition from Sequential Trigger Mode to Normal Mode

The sensor will transition from trigger mode to normal mode after setting “TRIGMODE [2:0] = 0h”. Start XVS input after transition to normal mode. Set TRIGMODE [2:0] after Next trigger rise prohibited period (t_{TGPD}) has passed. When TRIGMODE [2:0] is set before t_{TGPD}, read operation is stopped and that frame becomes an invalid frame.

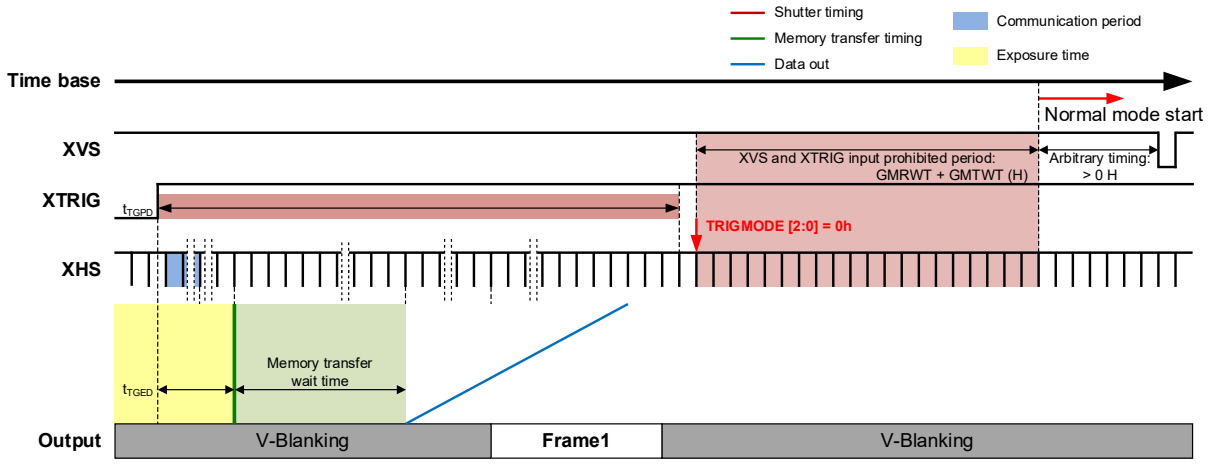


Image Drawing of Transition from Sequential Trigger Mode to Normal Mode

19.6.5. Pulse Output Function

This sensor has a pulse output function that indicates each state of shutter operation.

TOUT0 pin: The monitor output for Exposure period
TOUT1 pin: Programmable pulse
TOUT2 pin: Programmable pulse

(1) Exposure period control signal

This function is to output the actual exposure period control signal from the TOUT0 pin by setting the following registers.
This function can also be used in Fast trigger mode.

Register List of Pulse Output Function

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
TOUT0SEL [2:0]	06h	36h (3436h)	[2:0]	0h	TOUT0 pin setting 0h: Low fixed 1h: The monitor output for Exposure period

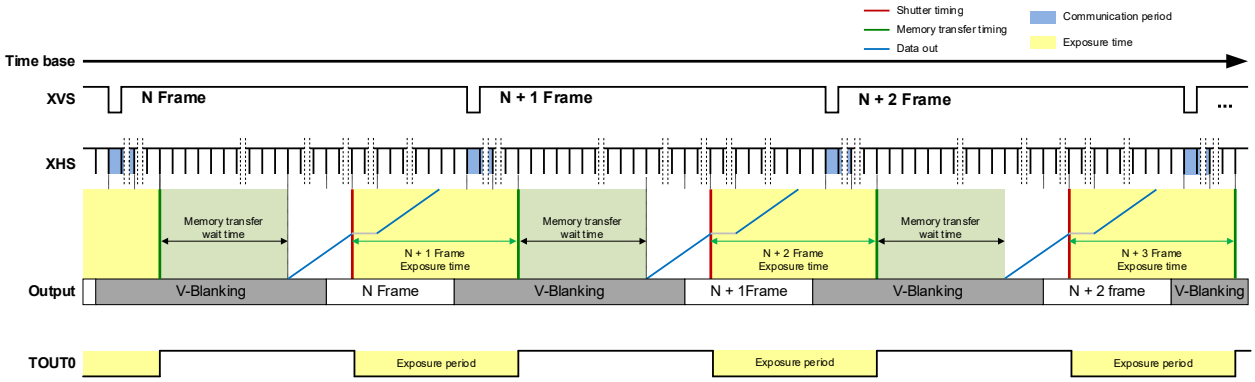


Image Drawing of the monitor output for Exposure period in Global Shutter (Normal Mode)

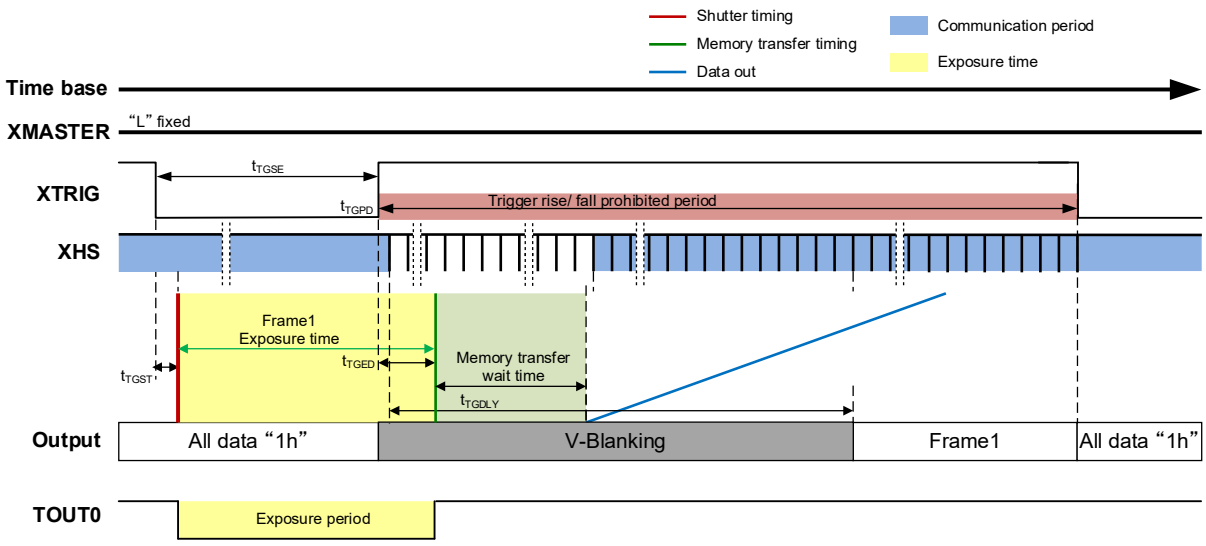


Image Drawing of the monitor output for Exposure period in Global Shutter (Fast Trigger Mode)

(2) Programmable Pulse signal

This function outputs programmable pulses from the TOUT1 and TOUT2 pins. The rise timing and fall timing of programmable pulse are set by registers, so user can generate the flexible pulses. For the reference point (The timing when register value set to 0) to be set, see the table “List of Reference point". The programmable pulse is output asynchronously with other signals on the basis of the sensor internal timing shown in the table “List of Reference point".
This function doesn't support Fast Trigger mode.

Register List of Pulse Output Function

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
TOUT1SEL [1:0]	06h	35h (3435h)	[1:0]	0h	TOUT1 pin setting 0h: Low fixed 3h: Pulse output
TOUT2SEL [1:0]			[3:2]	0h	TOUT2 pin setting 0h: Low fixed 3h: Pulse output
TRIG_TOUT1_SEL [3:0]		3Ah (343Ah)	[3:0]	0h	TOUT1 pin output selection 0h: Low fixed 1h: Pulse1 output
TRIG_TOUT2_SEL [3:0]			[7:4]	0h	TOUT2 pin output selection 0h: Low fixed 2h: Pulse2 output
PULSE1_EN_NOR [0]		78h (3478h)	[0]	0	Pulse1 enable in normal mode 0: disable 1: enable
PULSE1_EN_TRIG [0]			[1]	0	Pulse1 enable in trigger mode 0: disable 1: enable
PULSE1_POL [0]			[2]	0	Pulse1 polarity selection 0: High active 1: Low active
PULSE1_UP [23:0]		79h (3479h)	[7:0]	000000h	Pulse1 active period start timing setting Designated in line units from reference point
		7Ah (347Ah)	[7:0]		
		7Bh (347Bh)	[7:0]		
PULSE1_DN [23:0]		7Ch (347Ch)	[7:0]	000000h	Pulse1 active period end timing setting Designated in line units from reference point
		7Dh (347Dh)	[7:0]		
		7Eh (347Eh)	[7:0]		
PULSE2_EN_NOR [0]		80h (3480h)	[0]	0	Pulse2 enable in normal mode 0: disable 1: enable
PULSE2_EN_TRIG [0]			[1]	0	Pulse2 enable in trigger mode 0: disable 1: enable
PULSE2_POL [0]			[2]	0	Pulse2 polarity selection 0: High active 1: Low active
			[5]	0	Fixed to 1
PULSE2_UP [23:0]		81h (3481h)	[7:0]	000000h	Pulse2 active period start timing setting Designated in line units from reference point
		82h (3482h)	[7:0]		
		83h (3483h)	[7:0]		
PULSE2_DN [23:0]		84h (3484h)	[7:0]	000000h	Pulse2 active period end timing setting Designated in line units from reference point
		85h (3485h)	[7:0]		
		86h (3486h)	[7:0]		

List of Reference Point

	Normal mode	Trigger mode
Reference point of Pulse1	XVS fall edge in N frame	Fall edge of input trigger
Reference point of Pulse2	XVS fall edge in N +1 frame	Rise edge of input trigger

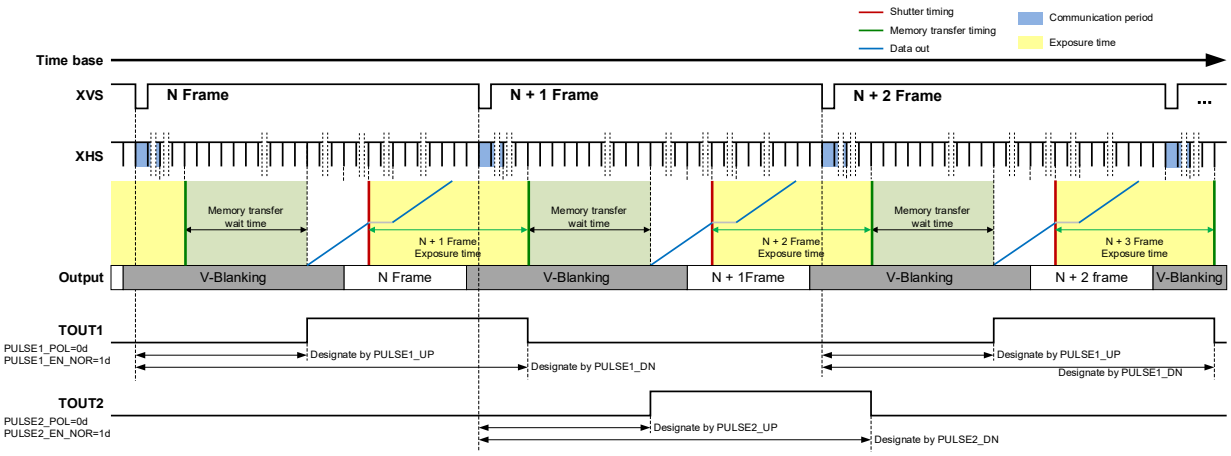


Image Drawing of Pulse Output Function in Global Shutter (Normal Mode)

In normal mode, TOUT1 and TOUT2 are output alternately each time inputting XVS.

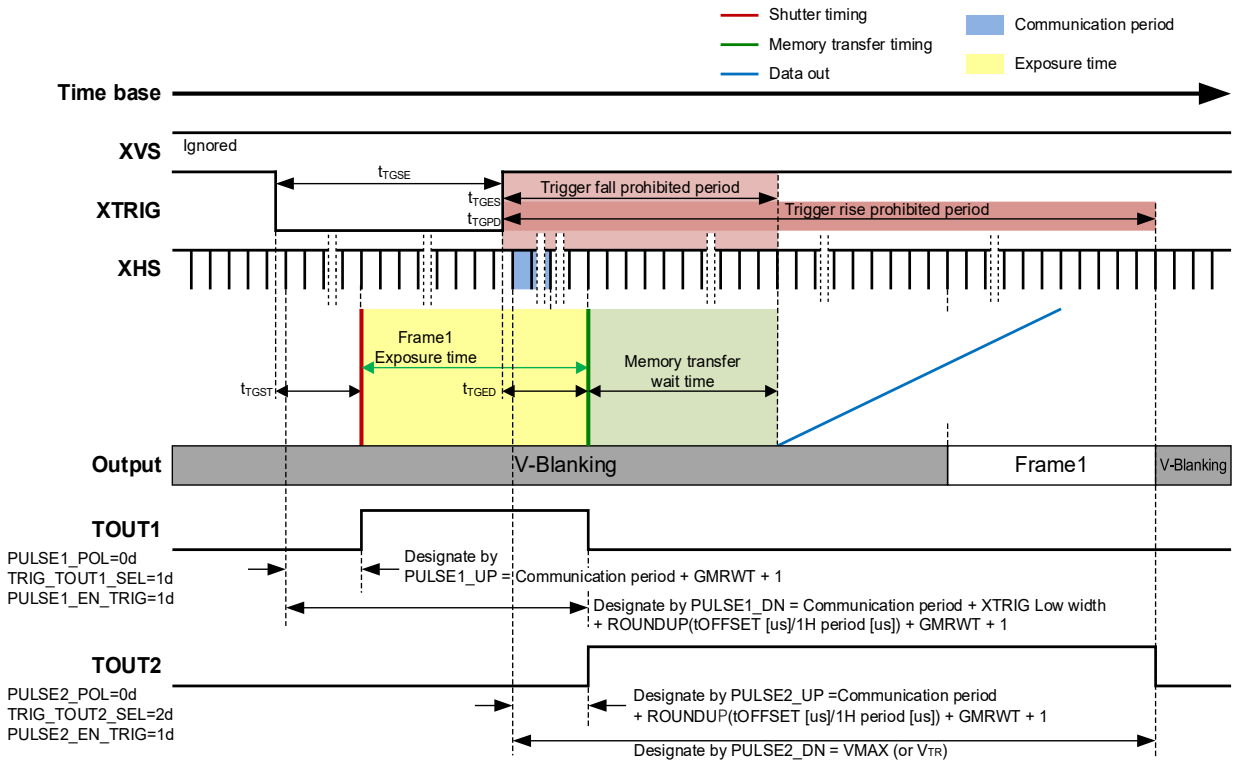


Image Drawing of Pulse Output Function in Global Shutter (Sequential Trigger Mode)

19.7. Signal Output

19.7.1. Output Pin Settings

This sensor supports SLVS (2 ch / 4 ch / 8 ch switching) output.
When changing the number of SLVS channels, set it via standby

Register List of Output Settings

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I^2C	bit		
STBSLVS [3:0]	06h	44h (3444h)	[3:0]	1h	The un-using SLVS channel go into standby
LANESEL [2:0]	0Bh	04h (3904h)	[2:0]	0h	SLVS Output channel selection (See the list of output pins below)

SLVS Output Pins

Output pins	SLVS output		
	2 ch	4 ch	8 ch
DOP0 / DOM0	Hi-Z	Hi-Z	Ch 7
DOP1 / DOM1	Hi-Z	Hi-Z	Ch 5
DOP2 / DOM2	Hi-Z	Ch 3	Ch 3
DOP3 / DOM3	Ch 1	Ch 1	Ch 1
DOP4 / DOM4	Ch 2	Ch 2	Ch 2
DOP5 / DOM5	Hi-Z	Ch 4	Ch 4
DOP6 / DOM6	Hi-Z	Hi-Z	Ch 6
DOP7 / DOM7	Hi-Z	Hi-Z	Ch 8
DCKP / DCKM	DCK	DCK	DCK

19.7.2. Output Format
When SLVS output

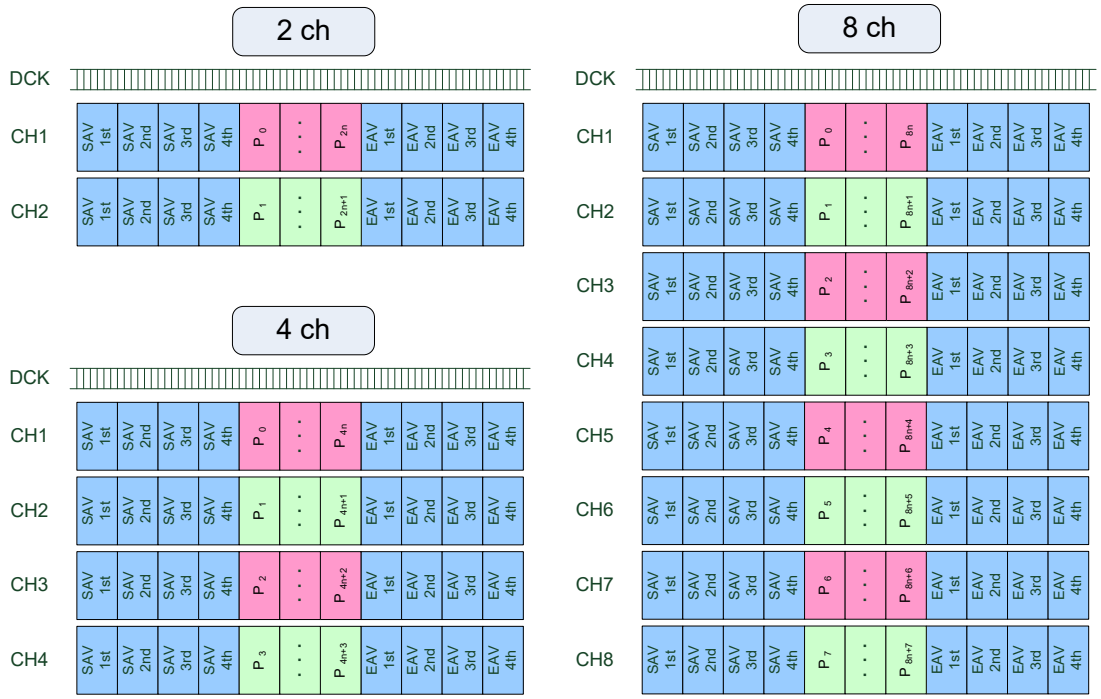
SLVS 2 ch / 4 ch / 8 ch output format is shown in the figure below.

When setting 2 ch, after four data of SAV is output in the order of CH1 to CH2 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH1 to CH2 respectively.

When setting 4 ch, after four data of SAV is output in the order of CH1 to CH4 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH1 to CH4 respectively.

When setting 8 ch, after four data of SAV is output in the order of CH1 to CH8 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH1 to CH8 respectively.

Data is sent MSB first. For details, see drive timing in each mode in the section of "Readout Drive Modes".



Output Format of SLVS 2 ch / 4 ch / 8 ch

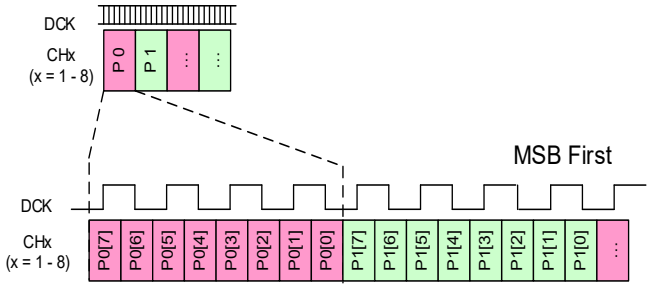
19.7.3. Output Pin Bit Width Selection

The output pin width can be selected from 8-bit, 10-bit or 12-bit output using register ADBIT, ODBIT. Sync code is output according to bit width setting of these register.

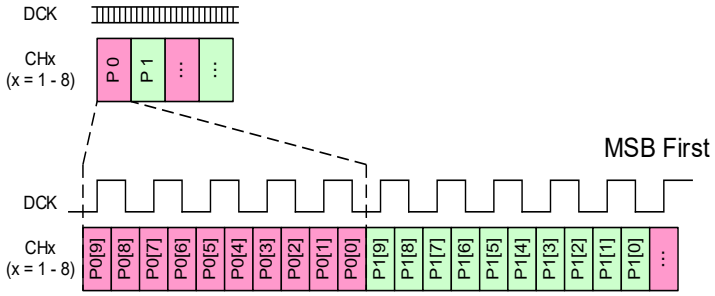
Register List of Bit Width Selection

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address ( ) : I²C	bit			
ADBIT [1:0]	04h	00h (3200h)	[5:4]	0h	0h: 10 bit 1h: 12 bit 2h: 8 bit	Set same value to both ADBIT and ODBIT
ODBIT [1:0]	06h	30h (3430h)	[1:0]	0h	0h: 10 bit 1h: 12 bit 2h: 8 bit	

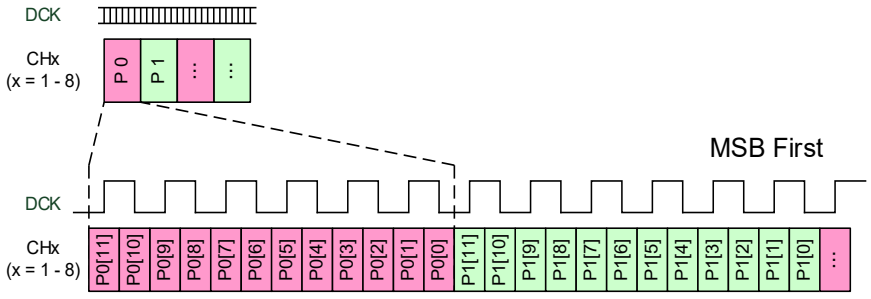
When SLVS output



Example of Data format in SLVS 8-bit output



Example of Data format in SLVS 10-bit output



Example of Data format in SLVS 12-bit output

19.7.4. Output Signal Range

The sensor output has either a 8-bit or 10-bit or 12-bit gradation, but SLVS output is not performed over the full range, and the maximum output value is “FFh – 1” (8-bit output), “3FFh - 1” (10-bit output) and “FFFh - 1” (12-bit output). The minimum value is 001h. The output range for each output gradation is shown in the table below. The maximum level and the minimum level are output only in the sync codes. For sync codes, see subsection “SLVS Output Format” in chapter “Readout Drive Modes”.

Output Gradation and Output Range

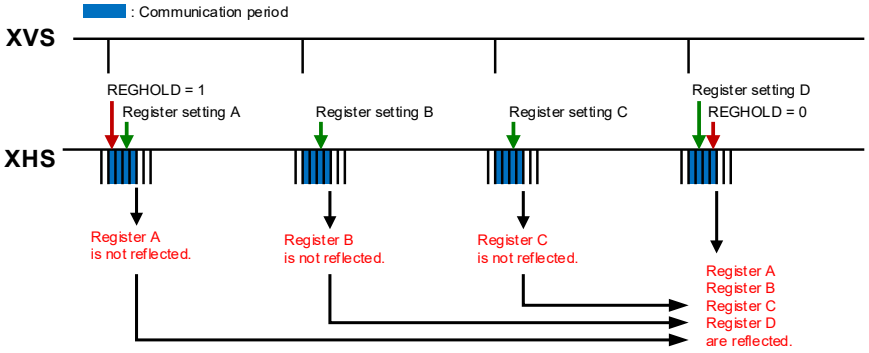
Output gradation	Output value	
	SLVS	
	Min.	Max.
8 bit	01h	FEh
10 bit	001h	3FEh
12 bit	001h	FFEh

19.8. Register Hold Setting

Register setting can be transmitted with divided to several frames and it can be reflected globally at a certain frame by the register REGHOLD. Setting REGHOLD = 1 at the start of register communication period prevents the registers that are set thereafter from reflecting at the frame reflection timing. The registers that are set when setting REGHOLD = 1 are reflected globally by setting REGHOLD = 0 at the end of communication period of the desired frame to reflect the register.

Register List of Register Hold

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I^2C	bit		
REGHOLD [0]	02h	34h (3034h)	[0]	0	0: Invalid 1: Valid (Register hold)



Register Hold Setting

19.9. Mode Transition

The Mode transition between operations is shown below. These examples shown in case that setting is completed within one communication timing.

List of Mode Transition

Transition			State
Operation mode			
Normal mode (Sensor Slave mode)	→	Sequential Trigger mode	Via the standby state is unnecessary Invalid frame: 1
Sequential Trigger mode	→	Normal mode (Sensor Slave mode)	
Normal mode (Sensor Master mode)	→	Fast Trigger mode	Via the standby state is necessary
Fast Trigger mode	→	Normal mode (Sensor Master mode)	
Readout mode (Normal mode or Sequential Trigger mode)			
All-pixel	→	ROI	Via the standby state is unnecessary Invalid frame: 0
ROI	→	All-pixel	
ROI	→	ROI	
Readout mode (Fast Trigger mode)			
All-pixel	→	ROI	Via the standby state is necessary
ROI	→	All-pixel	
ROI	→	ROI	
- Transition between modes other than the above - Change the input frequency of INCK[*1] - Change the register setting noted “S” in the reflection timing column of the Register Map			Via the standby state is necessary

[*1] When changing input INCK frequency, care should be taken not to be input pulses whose width are shorter than the High / Low level width in front and behind of the INCK pulse at the frequency change. If the pulses above generate at the frequency change, change INCK frequency during system reset in the state of XCLR = Low, and then perform system clear in the state of XCLR = High following the item of "Power on sequence" in the section of "Power on / off sequence". Execute initial setting again because the register settings become default state after system clear.

19.10. Other Function

This sensor has the function as below. About detail, refer to each application note.

- Multi Frame Set Output mode (2 / 4 frame)
- Multi Exposure Trigger mode
- Multi Frame ROI (Multi Exposure + ROI) mode
- Low Power Consumption (Low power consumption function is always ON)
- Thermometer
- Gradation Compression
- Dual Trigger
- Self Trigger
- Short Interval Shutter function
- Pattern Generator (Refer to Support Package)

19.11. Extension Function

Use these function after enough checks and evaluation.

- Black Level Auto Adjust Off
- Short Exposure Mode

20. Power-on and Power-off Sequence

20.1. Power-on sequence

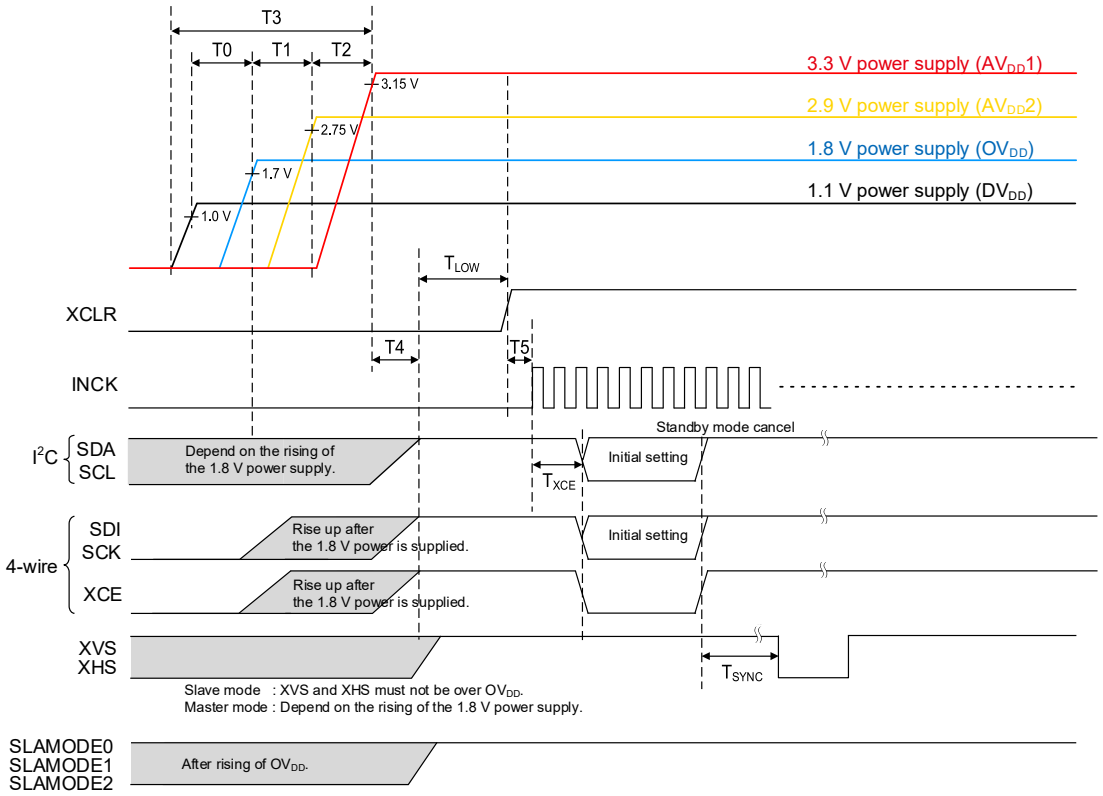
Follow the sequence below to turn on the power supplies.

(1) Turn on the power supplies so that the power supplies rise in order of 1.1 V power supply (DV_{DD}) →1.8 V power supply (OV_{DD}) → 2.9 V power supply ($AV_{DD}2$) → 3.3 V power supply ($AV_{DD}1$). In addition, all power supplies should finish rising within 200 ms. Set each digital input pin (INCK, XCE, SCK, SDI, XCLR, XMASTER, XTRIG1, XTRIG2, SLAMODE0, SLAMODE1, SLAMODE2, XVS, and XHS) to 0 V or high impedance.

(2) The register values are undefined immediately after power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.)
In addition, hold XCE to High level during this period. Rise XCE after 1.8 V power supply (OV_{DD}), so hold XCE at High level until INCK is input.

(3) Start the input of INCK after turning the level of XCLR into the high.

(4) Make the sensor setting by register communication after stabilizing the master clock (INCK).

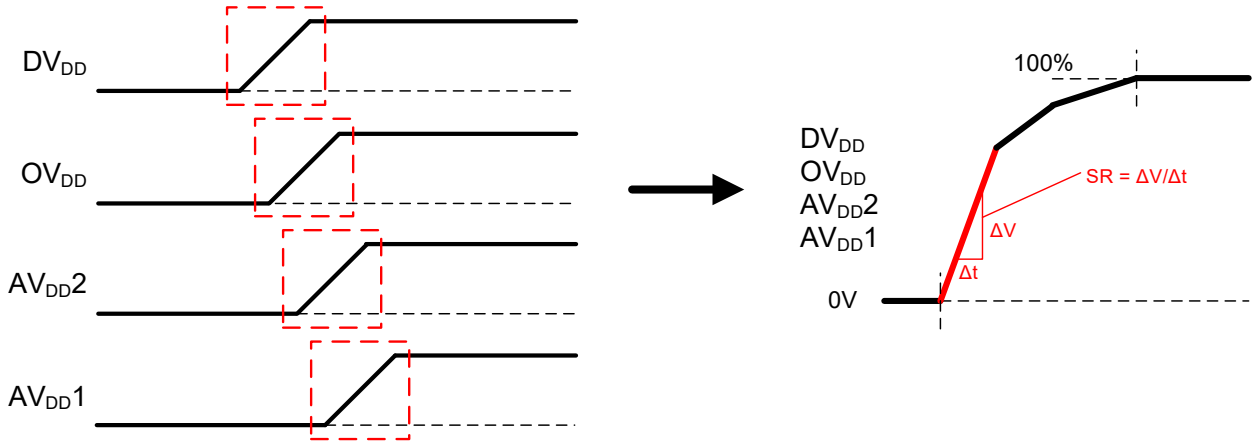


Power-on Sequence

Item	Symbol	Min.	Max.	Unit
1.1 V power supply rising to 1.8 V power supply rising	T0	0	–	ms
1.8 V power supply rising to 2.9 V power supply rising	T1	0	–	ms
2.9 V power supply rising to 3.3 V power supply rising	T2	0	–	ms
Rising time of all power supply	T3	–	200	ms
All power supply rising to XCE High	T4	0	–	ms
XCE High to Clear OFF	T_{LOW}	0.5	–	µs
Clear OFF to INCK rising	T5	1	–	µs
INCK rising to Communication start	T_{XCE}	20	–	µs
Standby OFF (communication) to External input XHS, XVS (slave mode only)	T_{SYNC}	1138	–	ms

20.2. Slew Rate Limitation of Power-on Sequence

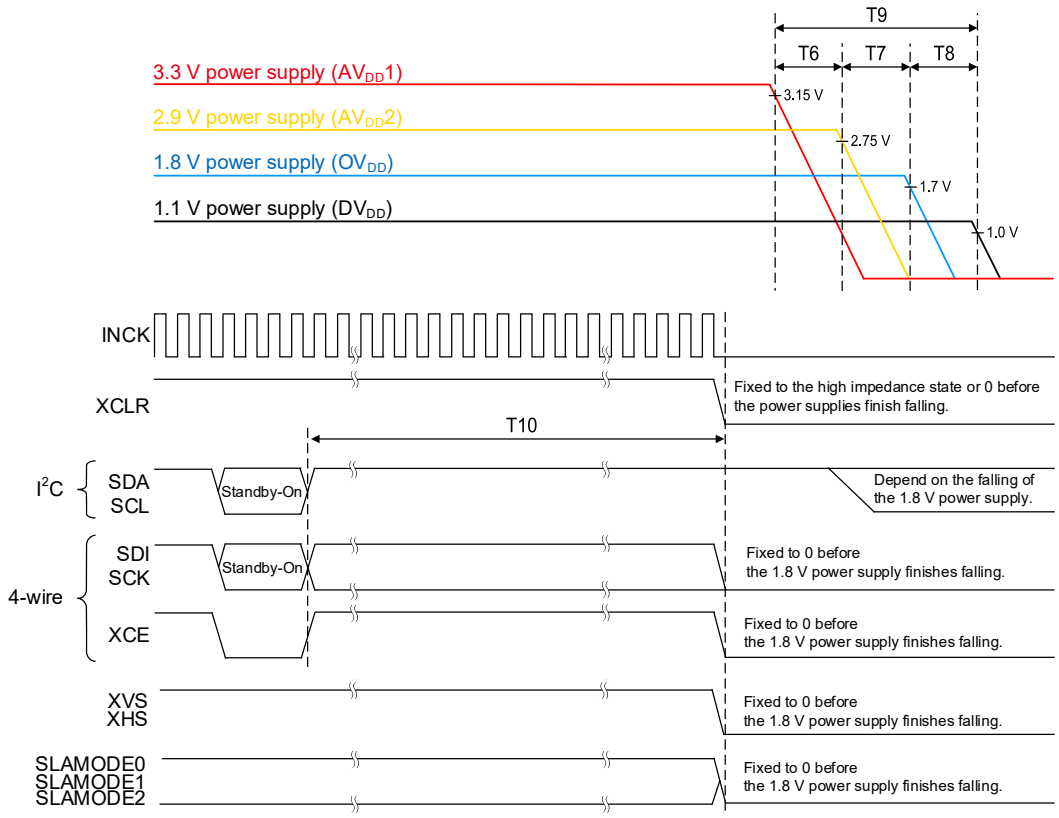
Conform the slew rate limitation shown below when power supply change 0 V to each voltage (0 % to 100 %) in power-on sequence.



Item	Symbol	Power supply	Min.	Max.	Unit	Remarks
Slew rate	SR	DV_{DD} (1.1 V)	—	25	mV/μs	
		OV_{DD} (1.8 V)	—	25	mV/μs	
		$AV_{DD}2$ (2.9 V)	—	25	mV/μs	
		$AV_{DD}1$ (3.3 V)	—	25	mV/μs	

20.3. Power-off Sequence

Turn off the power supplies so that the power supplies fall in order of 3.3 V power supply ($AV_{DD}1$) → 2.9 V power supply ($AV_{DD}2$) → 1.8 V power supply (OV_{DD}) → 1.1 V power supply (DV_{DD}). In addition, all power supplies should finish falling within 200 ms.
Set each digital input pin (INCK, XCE, SCK, SDI, XCLR, XMASTER, XTRIG1, XTRIG2, SLAMODE0, SLAMODE1, SLAMODE2, XVS, and XHS) to 0 V or high impedance before the 1.8 V power supply (OV_{DD}) falls.



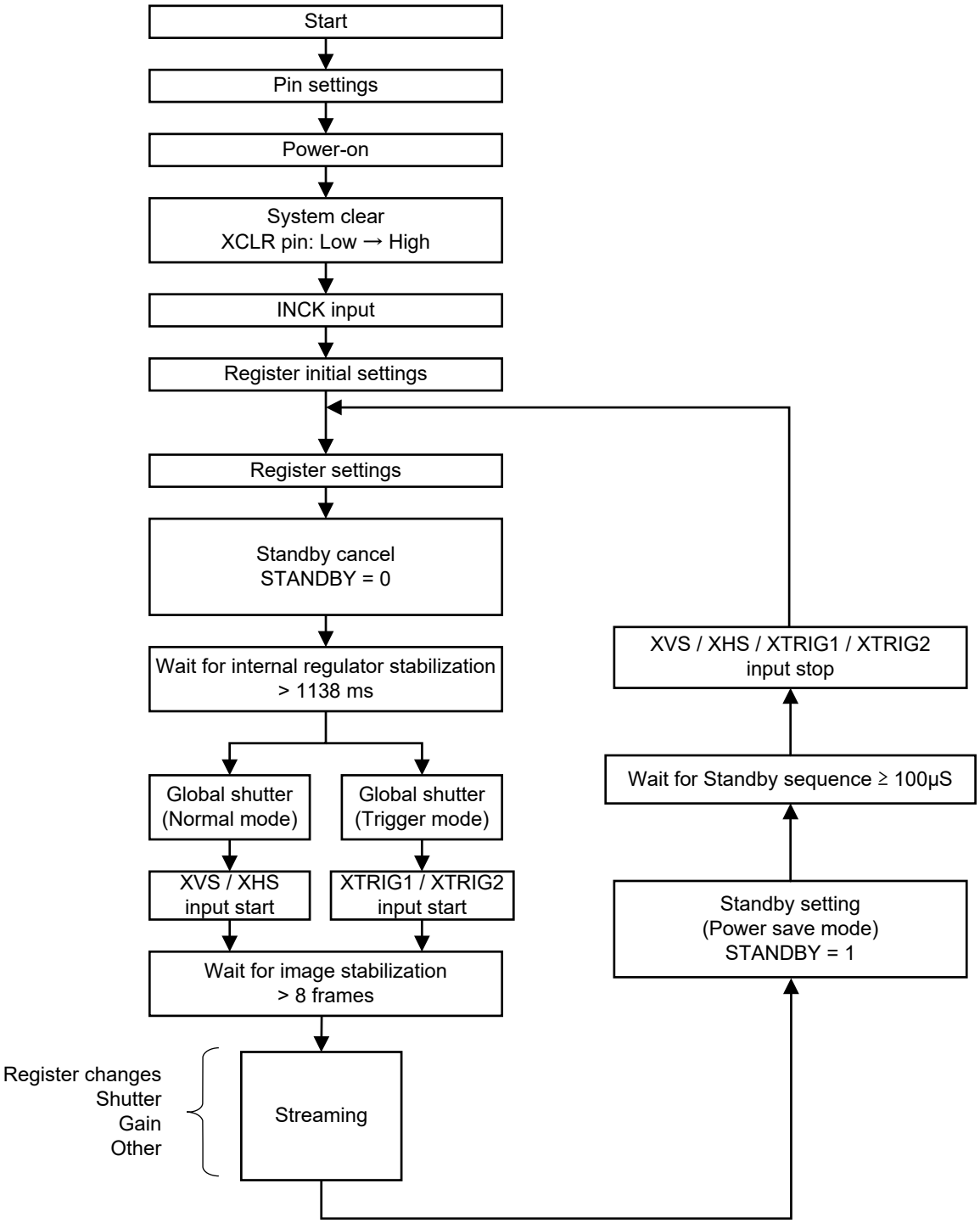
Power-off Sequence

Item	Symbol	Min.	Max.	Unit
3.3 V power supply fall to 2.9 V power supply fall	T6	0	–	ms
2.9 V power supply fall to 1.8 V power supply fall	T7	0	–	ms
1.8 V power supply fall to 1.1 V power supply fall	T8	0	–	ms
Fall time of all power supplies	T9	–	200	ms
“Standby-On” to “Set 0 V or Hi-z each digital input pin”	T10	100	–	μs

21. Sensor Setting Flow

21.1. Setting Flow in Sensor Slave Mode

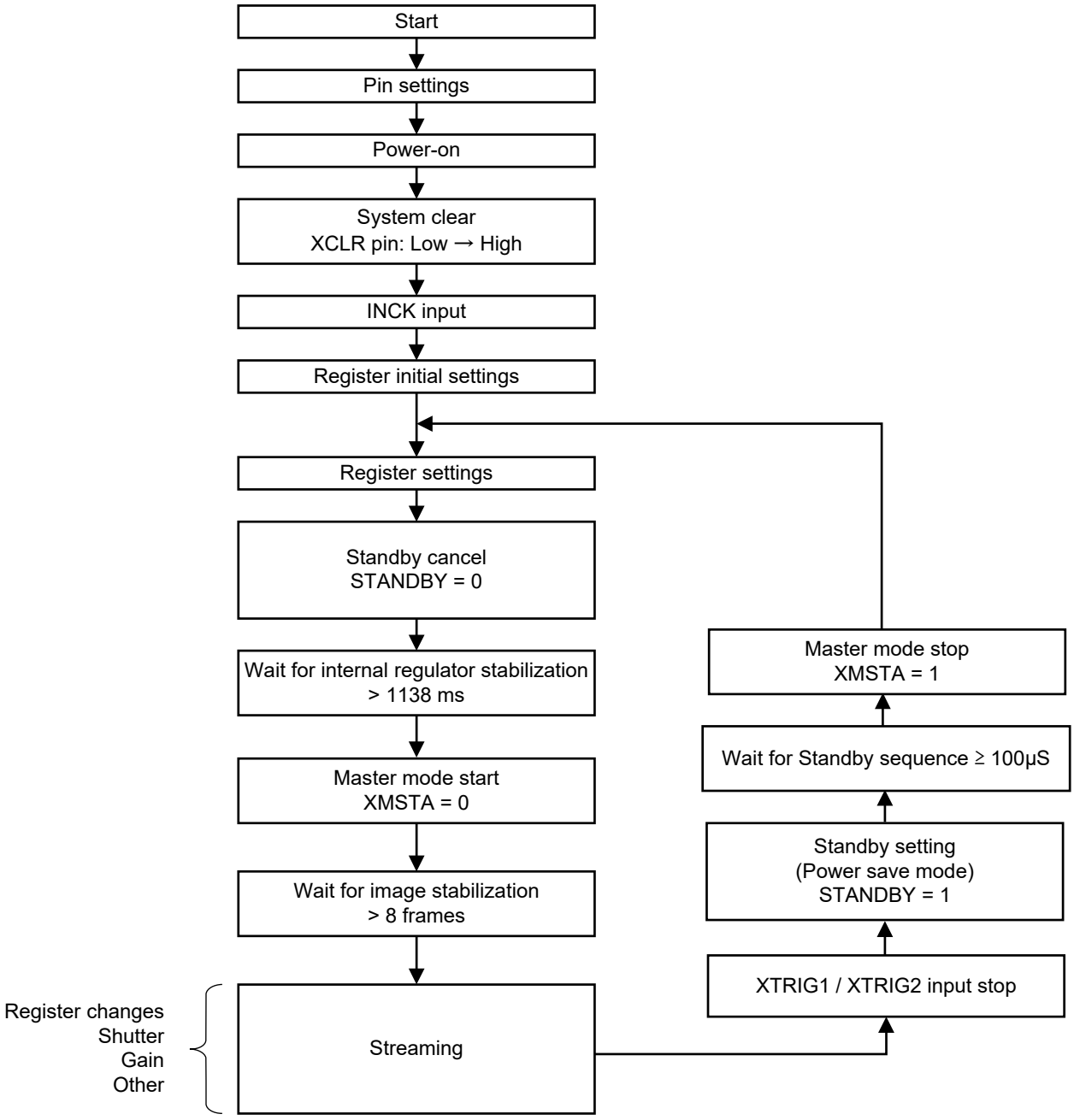
The figure below shows the operation flow in sensor slave mode.
For details from “Power-on” to “System clear”, see section “Power-on sequence”. For details from “Standby cancel” to “Wait for image stabilization”, see section “Standby mode”. “Standby setting (Power save mode)” can be made by setting the STANDBY register to “1” during “Streaming”.



Sensor Setting Flow (Sensor Slave Mode)

21.2. Setting Flow in Sensor Master Mode

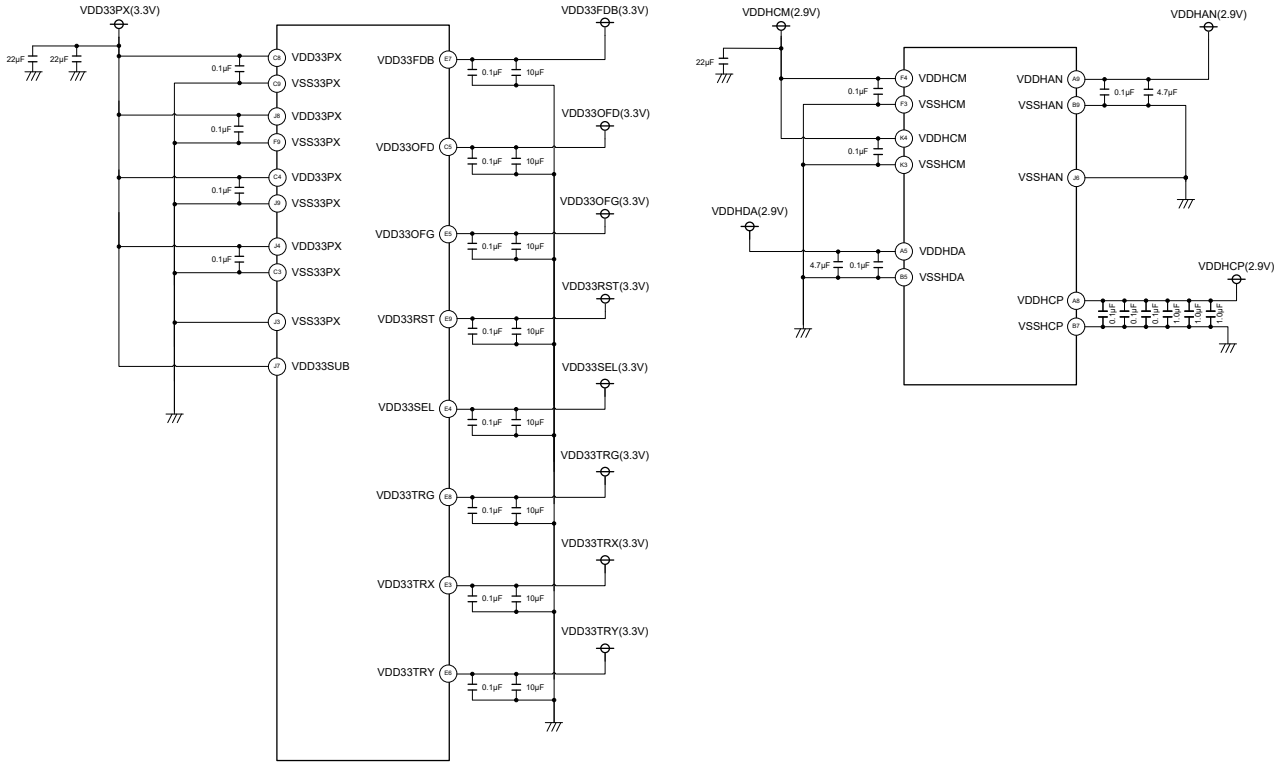
The figure below shows the operation flow in sensor master mode.
For details from “Power-on” to “System clear”, see section “Power-on sequence”. For details from “Standby cancel” to “Wait for image stabilization”, see section “Standby mode”. In master mode, “Master mode start” by setting the master mode start register XMSTA to “0” after “Wait for internal regulator stabilization”.
“Standby setting (Power save mode)” can be made by setting the STANDBY register to “1” during “Streaming”. At this time, set “Master mode stop” by setting XMSTA to “1”.



Sensor Setting Flow (Sensor Master Mode)

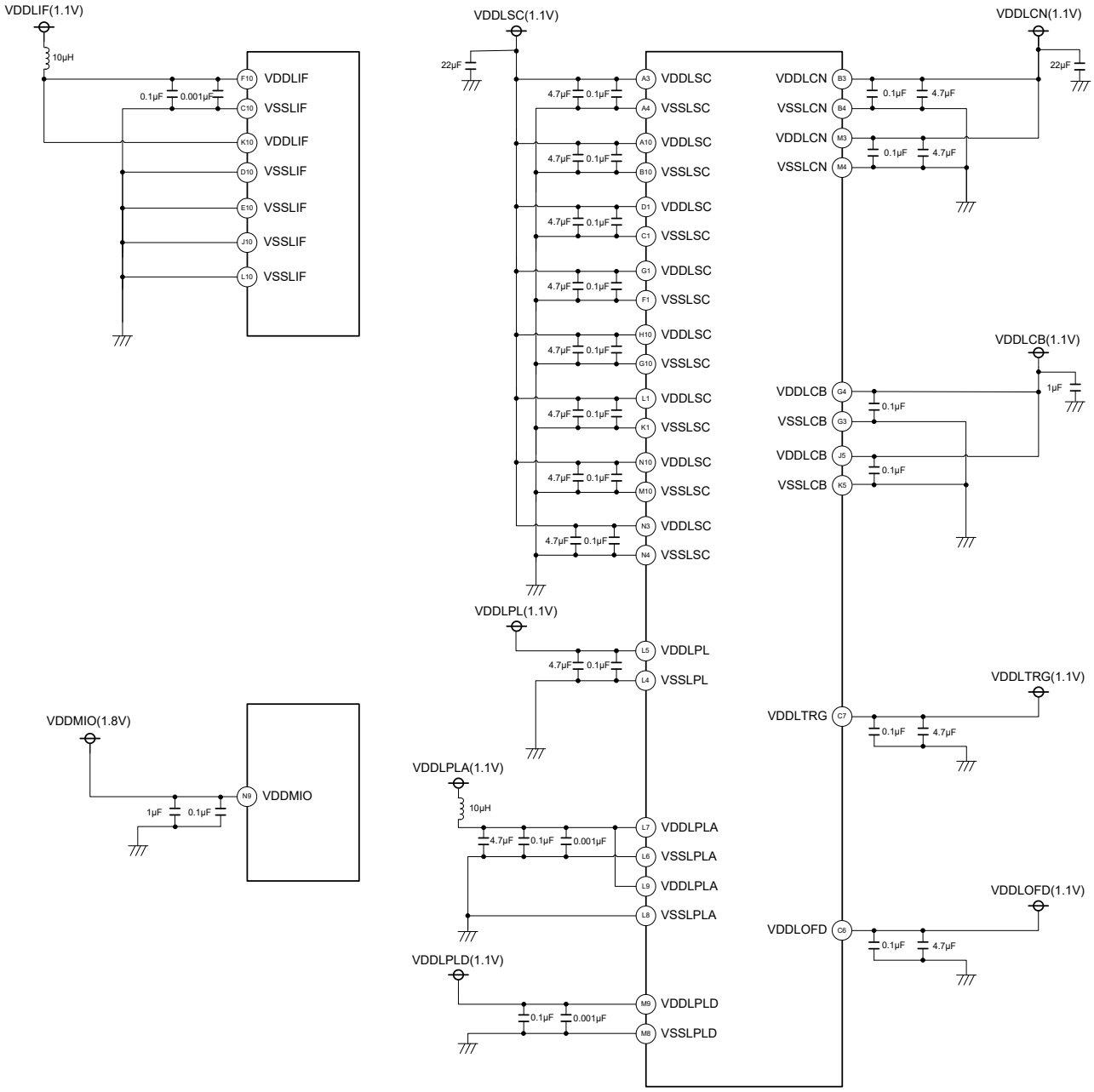
22. Peripheral Circuit

22.1. Analog Power Pins



Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

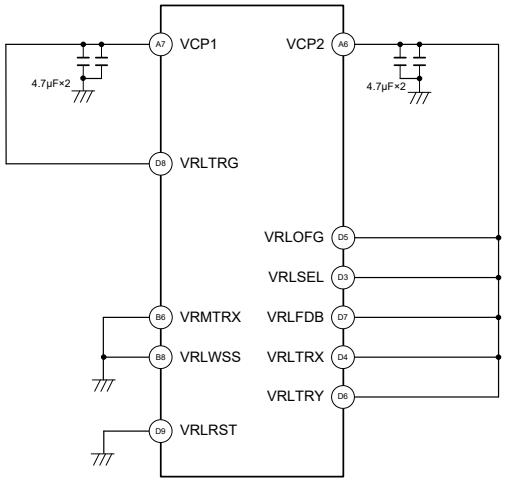
22.2. Digital Power Pins



Pin G4, J5, C6 and C7 are analog power pins. But these pins can be connected to the digital power pins. So, it describes on this page. These pins can be separated from the digital power pins.

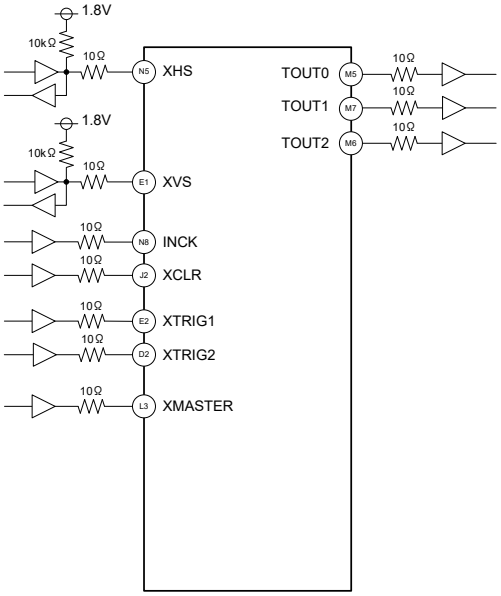
Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

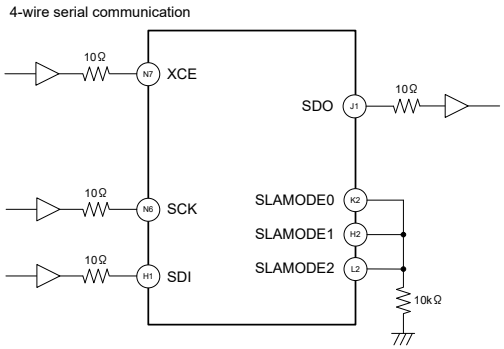
22.3. Analog Other Pins

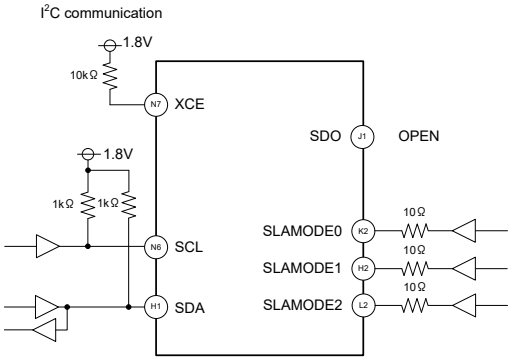


Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

22.4. Digital I/O Pins

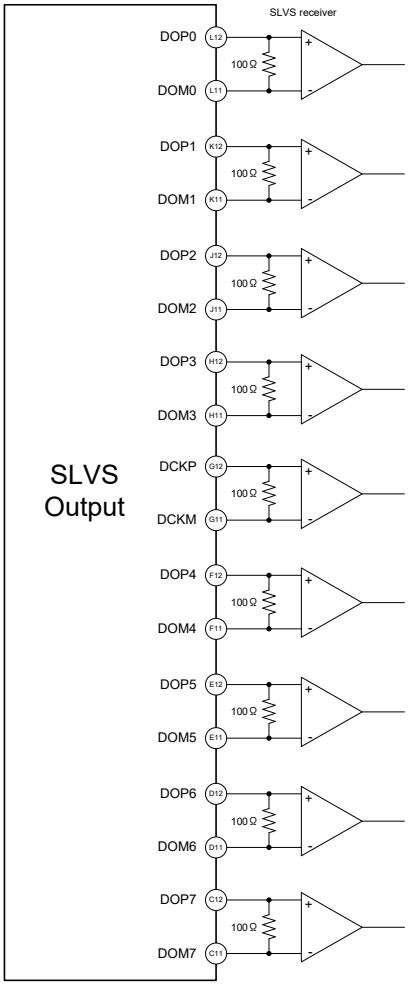






Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

22.5. Output pins



Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

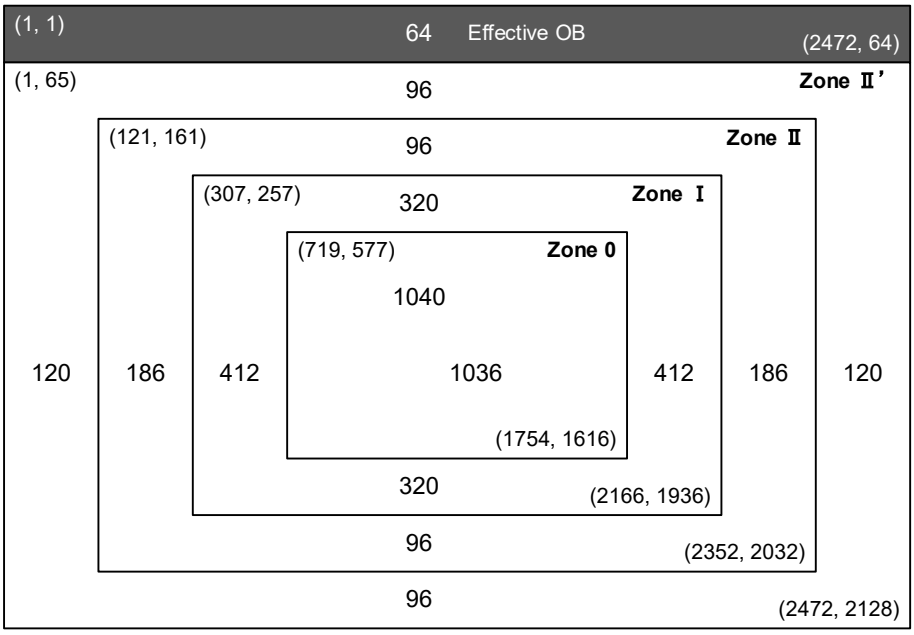
23. Spot Pixel Specifications

($AV_{DD}1$ = 3.3 V, $AV_{DD}2$ = 2.9V, OV_{DD} = 1.8 V, DV_{DD} = 1.1 V, Tj = 60 ˚C, 30 frame/s, Gain: 0 dB)

Type of distortion	Level	Maximum distorted pixels in each zone			Measurement method	Remarks
		0 to II'	Effective OB	Ineffective OB		
Black and white pixels at high light	30 % ≤ D	37	No evaluation criteria applied		1	
White pixels in the dark	5.6 mV ≤ D	915		No evaluation criteria applied	2	1/30 s storage
Black pixels at signal saturated	D ≤ 598 mV	0	No evaluation criteria applied		3	

Note) 1. Zone is specified based on all-pixel drive mode
2. D…Spot pixel level
3. See chapter “Spot Pixel Pattern Specifications” for the use of spot pixels that are close to each other.

23.1. Spot Pixel Zone Definition



24. Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, particle radiation such as cosmic rays etc. may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".)
Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Semiconductor Solutions Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Semiconductor Solutions Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
5.6 mV or higher	2 pcs
10.0 mV or higher	1 pcs
24.0 mV or higher	1 pcs
50.0 mV or higher	0.1 pcs
72.0 mV or higher	0.1 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

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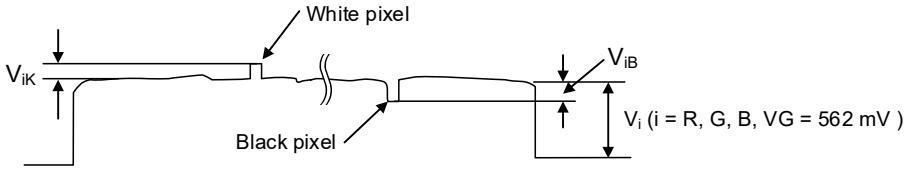
25. Measurement Method for Spot Pixels

After setting to standard imaging condition II, and the device driver should be set to meet bias and clock voltage conditions. Configure the drive circuit according to the example and measure.

(1) Black or white pixels at high light
After adjusting the luminous intensity so that the average value VG of the Gb / Gr signal outputs is 562 mV, measure the local dip point (black pixel at high light, V_{iB}) and peak point (white pixel at high light, V_{iK}) in the Gr / Gb / R / B signal output V_i (i = Gr / Gb / R / B), and substitute the value into the following formula.

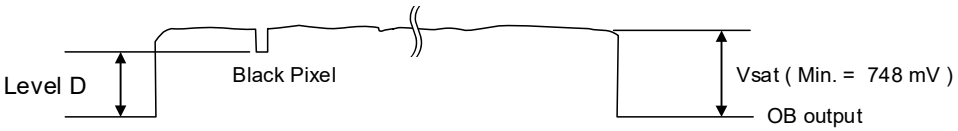
Spot pixel level D = ((V_{iB} or V_{iK}) / Average value of V) × 100 [%]



Signal output waveform of R / G / B channel

(2) White pixels in the dark
Set the device to a dark setting and measure the local peak point of the signal output waveform, using the average value of the dark signal output as a reference.

(3) Black pixels at signal saturated
Set the device to operate in saturation and measure the local dip point, using the OB output as a reference.

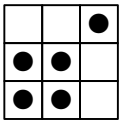
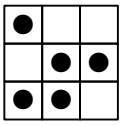
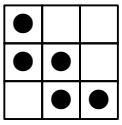
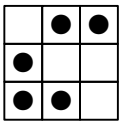


Signal output waveform of R / G / B channel

26. Spot Pixel Pattern Specification

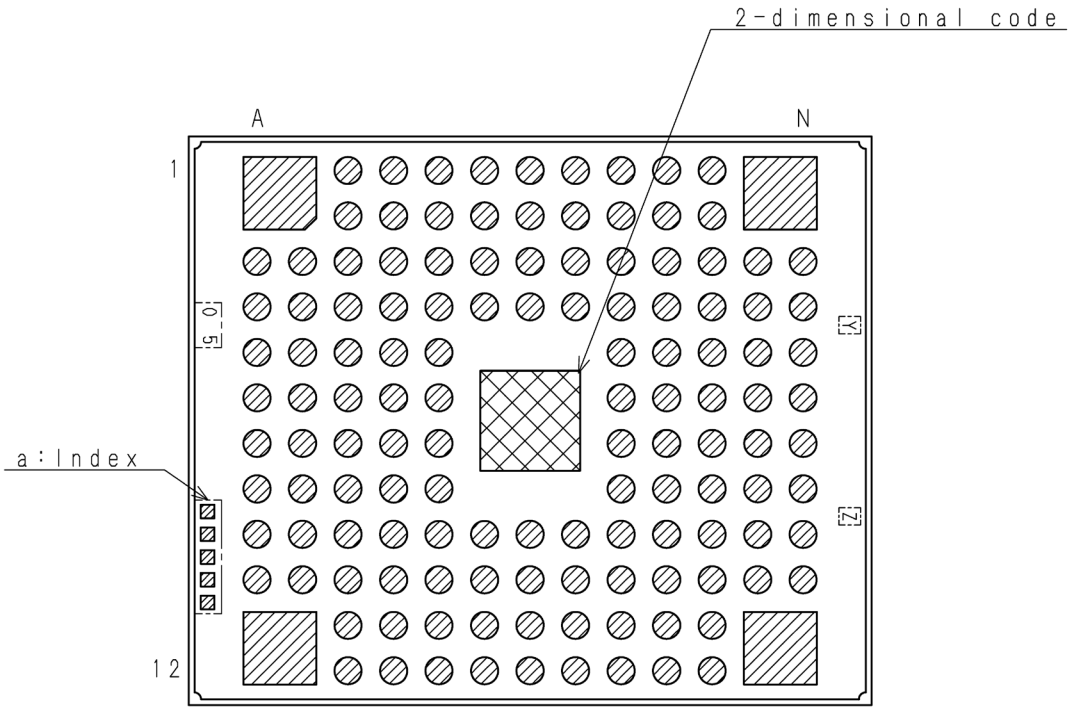
White Pixel, Black Pixel and Bright Pixel are judged from the pattern whether they are allowed or rejected, and counted.

Pixel patterns with 5 or more spot pixels occurring in the 3 × 3 pixels area

No.	Pattern	White pixel Black pixel Bright pixel
1		Rejected
2		Rejected
3		Rejected
4		Rejected

Note) 1. “● ” shows the position of white pixel, black pixel and bright pixel.
2. When 12 or more spot pixels indicated “Rejected” is selected and removed.
3. Spot pixels other than described in the table above are all counted including the number of allowable spot pixels by zone.

27. Marking



Note : One character of alphabet or number shall be placed from Y to Z part.
(Plating option)

As for part "a", up to 5 indexes are arranged.
(Plating option)

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28. Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

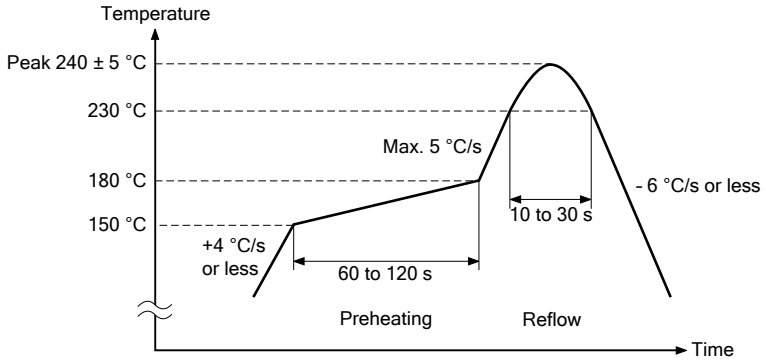
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Recommended temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (- 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.

(b) Perform the reflow soldering only one time.

(c) Finish reflow soldering within 72 h after unsealing the degassed packing. Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.

(d) Perform re-baking only one time under the condition at 125 °C for 24 h.

(e) Note that condensation on glass or discoloration on resin interfaces may occur if the actual temperature and time exceed the conditions mentioned above.

(3) Others

(a) Carry out evaluation for the solder joint reliability in your company.

(b) After the reflow, the paste residue of protective tape may remain around the seal glass. (The paste residue of protective tape should be ignored except remarkable one.)

(c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.

(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.

(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.

(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.

(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

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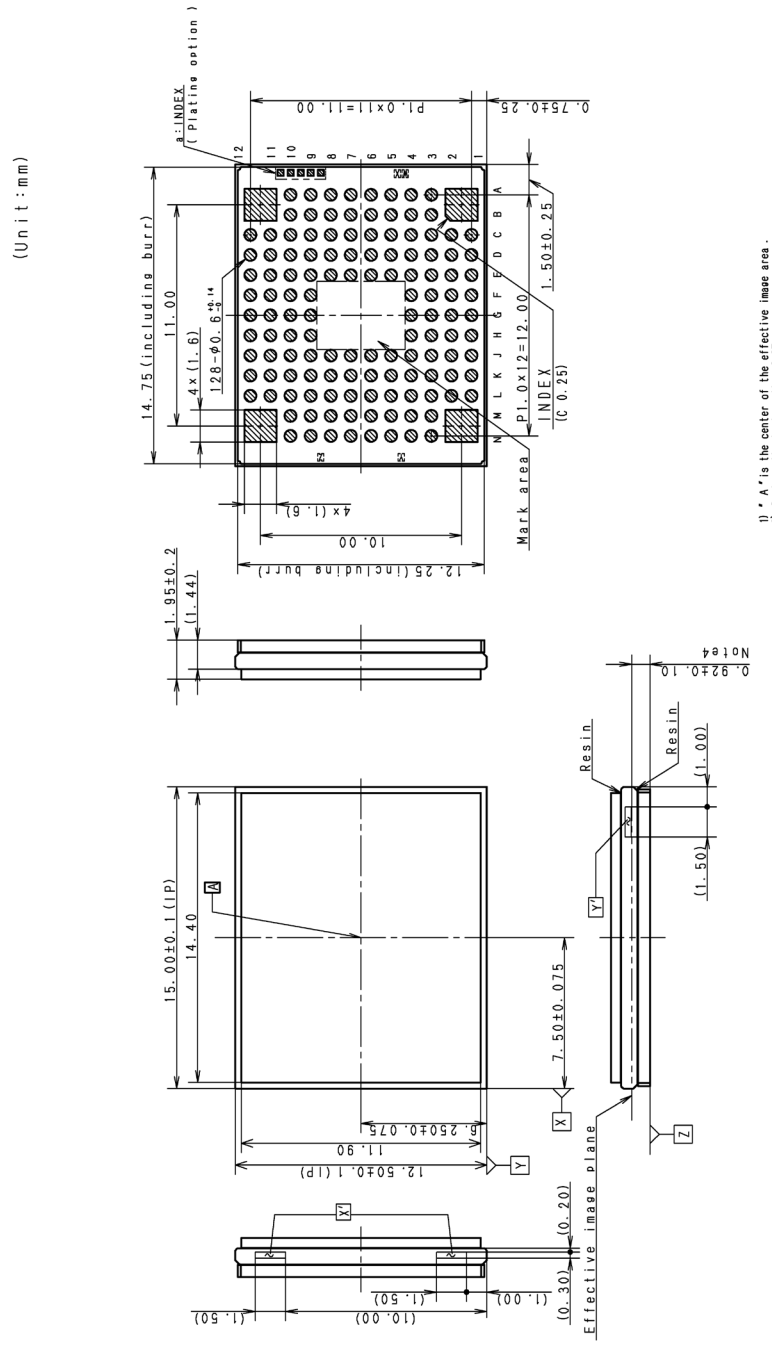
29. Package Outline

(Unit: mm)



1) "A" is the center of the effective image area.
2) Coplanarity is less than 0.07.
Coplanarity is a virtual flat surface calculated at three points(A12, N1, N12) of back side terminal.
3) The rotation angle of the effective image area relative to "X" and "Y" is ±0.5.
4) The height from the bottom "Z" to center of the effective image plane.
5) The tilt of the effective image area to the bottom "Z" is less than 0.05.
6) The thickness of the cover glass is 0.5.
7) As for standard for resin overflow in package outside, it shall be accepted up to outermost line tolerance of package.
8) One character of alphabet or number shall be placed from W to Z part. (Platina option)
9) As for part "a", up to 5 indexes are arranged.

PACKAGE STRUCTURE

CLASSIFICATION	LGA
LEAD TREATMENT	GOLD PLATING
PIN NUMBER	132pin
PACKAGE WEIGHT(Typ.)	0.87g
DRAWING NUMBER	AS-B126(E)

30. List of Trademark Logos and Definition Statements

Pregius S

* Pregius S is a registered trademark or trademark of Sony Group Corporation or its affiliates. Preguis S is a global shutter sensor technology for active pixel-type CMOS image sensors. By Stacking the signal processing on the back illuminated type CMOS Image Sensor it realizes small chip size and high sensitivity, whilst using the high picture quality global shutter pixel technology of Pregius.

Revision History

Date of change	Ver.	Page	Contain of Change
2020/09/17	0.1	—	First Edition
2021/3/12	0.2	3	Update: the TBD of Absolute Maximum Ratings Add: “Do not exceed 4.65V” in the remarks
		16	Update: the TBD (Typ.) and TBD of standby of power consumption
		17	Delete: “When Using SLVS”
		23	Update: the TBD of SLVS output characteristics
		25	Update: TBD of spectral sensitivity characteristics
		26	Delete: F5.6 in the remark column Update: the TBD of image sensor characteristics
		28	Update: the TBD of PLS of Measurement Method
		33	Correction: “Various Function” → “Various Functions”
		38	Update: the text in the chapter of register map
		43, 76, 80, 91	Delete: Chip ID=02h, address=E5h
		58	Correction: the initial value in the Chip ID=04h, address=24h (INCKSEL_D0) and address 26h (INCLSEL_D2) Delete: Chip ID=04h, address=33h
		72	Correction: the frame rate of the data rate 445.5 [Mbps/ch] (All-pixel mode: 8 / 4ch, A/D=8bit) (All-pixel mode: 8ch, A/D=10bit) (1/2 subsampling mode: 8 / 4 / 2ch, A/D=8bit) (1/2 subsampling mode: 8 / 4 / 2ch, A/D=10bit) (1/2 subsampling mode: 8ch, A/D=12bit) Correction: the number of INCK in 1 H of the data rate 445.5 [Mbps/ch] (each readout drive mode: 8 / 4 / 2ch, A/D=8 / 10bit)
		73	Delete: the description of the table reference
		75, 80, 90	Correction: the setting value of INCKSEL_ST2, INCK= 37.125MHz Correction: the setting value of INCKSEL_ST3, INCK= 54MHz
		76, 83	Correction: the initial value of the Chip-ID=04h, address=24h
		80	Delete: the remarks column of VMAX
		80, 81, 82, 83, 88	Correction: change to combined remarks column
		89	Correction: “Minimum horizontal output width after ROI operation” →“Minimum vertical output width after ROI operation” Correction: “Restrictions on ROI mode” → “Restrictions on Overlap ROI mode”
		91	Correction: the setting value of LLBLANK
		92	Correction: the line numbers of vertical blanking period and total in the image drawing
		93, 94, 99, 101, 104, 106, 117	Add: the bit width in the register name (STANDBY, XMSTA, VREVERSE, HREVERSE, VINT_EN_NOR, VINT_EN, REGHOLD)

Date of change	Ver.	Page	Contain of Change
2021/3/12	0.2	94	Correction: the setting value column in the register list of slave mode and master mode Correction: “Readout Drive mode" → “Readout Drive modes
		95	Correction: “packet headers” → “sync codes”
		98	Correction: normal and inverted drive outline in horizontal direction (TOP VIEW)
		100	Correction: the setting value of SHS in the register list of shutter setting
		100, 101, 103, 105	Update: TBD of t_{OFFSET}
		101	Update: List of Exposure Setting Correction: “Readout Drive Mode" → “Readout Drive Modes Delete: “SLVS output” of title in the list
		103, 105	Update: parameter list Correction: address of XMSTA Correction: “Readout Drive mode” → “Readout Drive modes
		105	Update: Calculation Formula of Exposure Time
		109	Add: description of bits width of register “PULSE1_EN_NOR” “PULSE1_EN_TRIG” “PULSE1_POL” “PULSE2_EN_NOR” “PULSE2_EN_TRIG” “PULSE2_POL”
		111	Correction: “Refer”→”See”
		116	Delete: the note 2 Correction: “All-pixel → ROI” → “ROI → ROI”
		118	Correction: the unit of “INCK rising to Communication start” in the table
		120	Correction: the symbol in the list of Power-off Sequence Add: “Standby-On” to “Set 0 V or Hi-z each digital input pin” in the table Update the figure of Power-off Sequence Correction: the table for Power-off Sequence
		121, 122	Correction: “Power ON” → “Power on”
		128	Update: the TBD of Spot Pixel Specifications the TBD of Sport Pixel Zone Definition
		129	Update: the TBD of Example of Annual Number of Occurrence
		130	Correction: “Vi (I” → “V_i (i”
		131	Correction: the TBD of note 2 of Spot pixel pattern
2021/7/29	E21704	1	Delete: tentative
		3	Correction: “–” → ”-”
		8	Delete: TBD values of Chip Center and Optical Center
		16	Update: the TBD of Power Consumption Update: Item column in the table
		26	Update: the TBD of Image Sensor Characteristics
		28	Update: the TBD of Measurement Method
		69, 70, 71, 72, 75	Delete: ”SLVS output”
		72	Update: Example frame rate

Date of change	Ver.	Page	Contain of Change
2021/7/29	E21704	93, 94, 95, 98, 102, 104, 115	Remove "h" from the initial values of 1bit width register
		128	Delete: TBD values of Spot Pixel Specifications Correction: “V_{DD}” → “V_{DD}”, “1.2 V” → “1.1 V”
		130	Update: the TBD of Measurement Method for Spot Pixels
		131	Update: the TBD of Spot Pixel Pattern Specification
		132	Update: the TBD of Marking
		135	Delete: TBD values of Package Outline
		136	Update: Definition Statements