SONY

Diagonal 8.0 mm (Type 1/2) VGA-Pixel Time-of-Flight Image Sensor

IMX556PLR-C

For the latest data sheet, please visit www.sunnywale.com

General Description and Application

The IMX556 is a fully integrated optical Time-of-Flight (ToF) camera sensor. The sensor features 640 x 480 (VGA) time-of-flight pixels based on the DepthSense™ pixel technology. Combined with a modulated light source, this sensor is capable of measuring distance and reflectivity with VGA resolution. This chip operates with analog 2.7 V, digital 1.2 V, and interface 1.8 V triple power supply, and has low power consumption. The device features CSI-2 serial data outputs. (Application: FA cameras, Industrial cameras)

Functions and Features

◆ Back-illuminated Time-of-flight image sensor
◆ High signal to noise ratio (SNR)
◆ Full resolution @max60 frame/s (4phase/frame)
◆ Pixel binning readout function
◆ Independent flipping and mirroring
◆ CSI-2 serial data output (MIPI 4lane, 960 Mbps/lane, D-PHY spec. ver. 1.2 compliant)
◆ 2-wire serial communication (Supports I2C "Fast-mode") / 4-wire SPI
◆ 4-wire SPI Master for Illumination signal
◆ 192 bits of OTP for users
◆ Built-in temperature sensor

E19X02C11

Device Structure

◆ Time-of-Flight Image Sensor

◆ Image size   : Diagonal 8.0 mm (Type 1/2)

◆ Total number of pixels   : 642 (H) × 498 (V) approx. 0.319 M pixels

◆ Number of effective pixels   : 642 (H) × 484 (V) approx. 0.310 M pixels

◆ Number of active pixels   : 640 (H) × 480 (V) approx. 0.307 M pixels

◆ Package size   : 15.50 mm (H) × 15.00 mm (V)

◆ Unit cell size   : 10.0 um (H) × 10.0 um (V)

◆ Substrate material   : Silicon

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	notes
Supply voltage (analog)	VANA	-0.3 to +3.3	V	refer to VSS level
Supply voltage (analog-low voltage)	VDDLMX	-0.3 to +2.0	V	
Supply voltage (digital)	VDIG	-0.3 to +2.0	V	
Supply voltage (interface)	VIF	-0.3 to +3.3	V	
Input voltage (digital)	VI	-0.3 to VIF+0.3 (Not exceed 3.3V)	V	
Output voltage (digital)	VO	-0.3 to VIF+0.3 (Not exceed 3.3V)	V	
Operation temperature	T_{opr}	-30 to +75	˚C	
Storage temperature	T_{stg}	-40 to +85	˚C	
Performance guarantee temperature	T_{spec}	-10 to +60	˚C	

Recommended Operating Voltage

Item	Symbol	Ratings	Unit	notes
Supply voltage (analog)	VANA	2.7 ± 0.1	V	refer to VSS level
Supply voltage (analog-low voltage)	VDDLMX	1.2 ± 0.1	V	
Supply voltage (digital)	VDIG	1.2 ± 0.1	V	
Supply voltage (interface)	VIF	1.8 ± 0.1	V	

USE RESTRICTION NOTICE

This USE RESTRICTION NOTICE ("Notice") is for customers who are considering or currently using the image sensor products ("Products") set forth in this specifications book. Sony Semiconductor Solutions Corporation ("SSS") may, at any time, modify this Notice which will be available to you in the latest specifications book for the Products. You should abide by the latest version of this Notice. If a SSS subsidiary or distributor has its own use restriction notice on the Products, such a use restriction notice will additionally apply between you and the subsidiary or distributor. You should consult a sales representative of the subsidiary or distributor of SSS on such a use restriction notice when you consider using the Products.

Use Restrictions

● The Products are intended for incorporation into such general electronic equipment as office products, communication products, measurement products, and home electronics products in accordance with the terms and conditions set forth in this specifications book and otherwise notified by SSS from time to time.

● You should not use the Products for critical applications which may pose a life- or injury-threatening risk or are highly likely to cause significant property damage in the event of failure of the Products. You should consult your sales representative beforehand when you consider using the Products for such critical applications. In addition, you should not use the Products in weapon or military equipment.

● SSS disclaims and does not assume any liability and damages arising out of misuse, improper use, modification, use of the Products for the above-mentioned critical applications, weapon and military equipment, or any deviation from the requirements set forth in this specifications book.

Design for Safety

● SSS is making continuous efforts to further improve the quality and reliability of the Products; however, failure of a certain percentage of the Products is inevitable. Therefore, you should take sufficient care to ensure the safe design of your products such as component redundancy, anti-conflagration features, and features to prevent mis-operation in order to avoid accidents resulting in injury or death, fire or other social damage as a result of such failure.

Export Control

● If the Products are controlled items under the export control laws or regulations of various countries, approval may be required for the export of the Products under the said laws or regulations.
You should be responsible for compliance with the said laws or regulations.

No License Implied

● The technical information shown in this specifications book is for your reference purposes only. The availability of this specifications book shall not be construed as giving any indication that SSS and its licensors will license any intellectual property rights in such information by any implication or otherwise. SSS will not assume responsibility for any problems in connection with your use of such information or for any infringement of third-party rights due to the same. It is therefore your sole legal and financial responsibility to resolve any such problems and infringement.

Governing Law

● This Notice shall be governed by and construed in accordance with the laws of Japan, without reference to principles of conflict of laws or choice of laws. All controversies and disputes arising out of or relating to this Notice shall be submitted to the exclusive jurisdiction of the Tokyo District Court in Japan as the court of first instance.

Other Applicable Terms and Conditions

● The terms and conditions in the SSS additional specifications, which will be made available to you when you order the Products, shall also be applicable to your use of the Products as well as to this specifications book. You should review those terms and conditions when you consider purchasing and/or using the Products.

General-0.0.9

Contents

1.   PKG Center and Optical Center (Top View)

Unit: mm

A1 pin

Center of Effective pixel area
= Optical Center

（０．３０６，０．４６５）

Sensor scanning
V direction (Normal)

Sensor scannning
H direction (Normal)

PKG Center

（０，０）

Figure 1 PKG Center and Optical Center (Top View) (x and y coordinates in mm)

2.   Pin Configuration
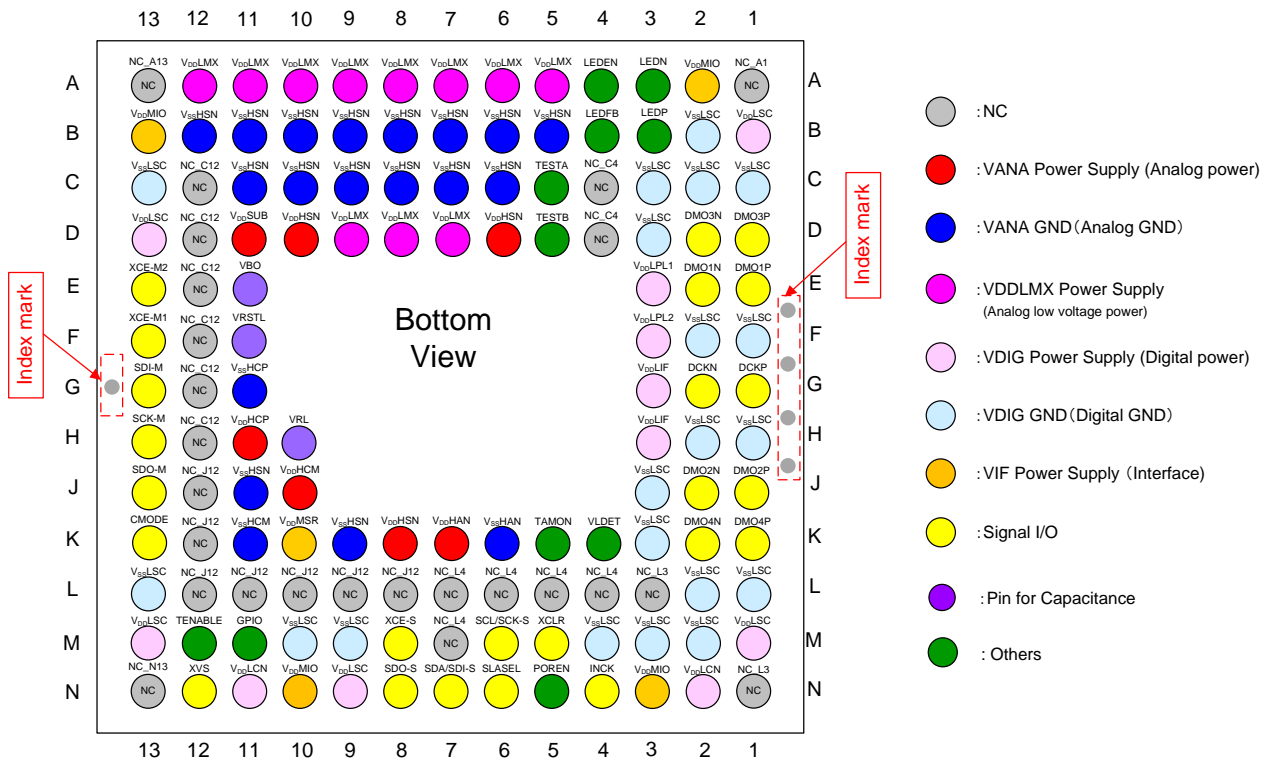
Figure 2 Pin Configuration

(The "NC" pin can be connected to GND.)

3.   Pin Description

Table 1   Pin Description

No.	Pin No	Symbol	I/O	A/D	Description	Remarks
1	A1	NC_A1	—	—	N.C.	
2	A2	VDDMIO	Power	D	VIF power supply	
3	A3	LEDN	O	D	Digital output	LVDS output (CLK -) for illumination signal
4	A4	LEDEN	I/O	D	Digital I/O	LED enable
5	A5	VDDLMX	Power	A	VDDLMX power supply	
6	A6	VDDLMX	Power	A	VDDLMX power supply	
7	A7	VDDLMX	Power	A	VDDLMX power supply	
8	A8	VDDLMX	Power	A	VDDLMX power supply	
9	A9	VDDLMX	Power	A	VDDLMX power supply	
10	A10	VDDLMX	Power	A	VDDLMX power supply	
11	A11	VDDLMX	Power	A	VDDLMX power supply	
12	A12	VDDLMX	Power	A	VDDLMX power supply	
13	A13	NC_A13	—	—	N.C.	
14	B1	VDDLSC	Power	D	VDIG power supply	
15	B2	VSSLSC	GND	D	VDIG GND	
16	B3	LEDP	O	D	Digital output	LVDS output (CLK +) for LED illumination signal
17	B4	LEDFB	I	D	Digital input	Leave this pin open (N.C.) For internal test only.
18	B5	VSSHSN	GND	A	VANA GND	
19	B6	VSSHSN	GND	A	VANA GND	
20	B7	VSSHSN	GND	A	VANA GND	
21	B8	VSSHSN	GND	A	VANA GND	
22	B9	VSSHSN	GND	A	VANA GND	
23	B10	VSSHSN	GND	A	VANA GND	
24	B11	VSSHSN	GND	A	VANA GND	
25	B12	VSSHSN	GND	A	VANA GND	
26	B13	VDDMIO	Power	D	VIF power supply	
27	C1	VSSLSC	GND	D	VDIG GND	
28	C2	VSSLSC	GND	D	VDIG GND	
29	C3	VSSLSC	GND	D	VDIG GND	
30	C4	NC_C4	—	—	N.C.	
31	C5	TESTA	I	A	Test signal input	Leave this pin open (N.C.)
32	C6	VSSHSN	GND	A	VANA GND	
33	C7	VSSHSN	GND	A	VANA GND	
34	C8	VSSHSN	GND	A	VANA GND	
35	C9	VSSHSN	GND	A	VANA GND	
36	C10	VSSHSN	GND	A	VANA GND	
37	C11	VSSHSN	GND	A	VANA GND	
38	C12	NC_C12	—	—	N.C.	
39	C13	VSSLSC	GND	D	VDIG GND	
40	D1	DMO3P	O	D	Digital output	MIPI output (DATA+)
41	D2	DMO3N	O	D	Digital output	MIPI output (DATA-)
42	D3	VSSLSC	GND	D	VDIG GND	
43	D4	NC_C4	—	—	N.C.	

No.	Pin No	Symbol	I/O	A/D	Description	Remarks
44	D5	TESTB	I	A	Test signal input	Leave this pin open (N.C.)
45	D6	VDDHSN	Power	A	VANA power supply	
46	D7	VDDLMX	Power	A	VDDLMX power supply	
47	D8	VDDLMX	Power	A	VDDLMX power supply	
48	D9	VDDLMX	Power	A	VDDLMX power supply	
49	D10	VDDHSN	Power	A	VANA power supply	
50	D11	VDDSUB	Power	A	VANA power supply	
51	D12	NC_C12	—	—	N.C.	
52	D13	VDDLSC	Power	D	VDIG power supply	
53	E1	DMO1P	O	D	Digital output	MIPI output (DATA+)
54	E2	DMO1N	O	D	Digital output	MIPI output (DATA-)
55	E3	VDDLPL1	Power	D	VDIG power supply	
56	E11	VBO	Power	A	VANA power supply	Pin for Capacitance
57	E12	NC_C12	—	—	N.C.	
58	E13	XCE-M2	O	D	Digital output	Communication enable 2nd XCE pin of 4-wire SPI Master
59	F1	VSSLSC	GND	D	VDIG GND	
60	F2	VSSLSC	GND	D	VDIG GND	
61	F3	VDDLPL2	Power	D	VDIG power supply	
62	F11	VRSTL	Power	A	VANA power supply	Pin for Capacitance
63	F12	NC_C12	—	—	N.C.	
64	F13	XCE-M1	O	D	Digital output	Communication enable 1st XCE of 4-wire SPI Master
65	G1	DCKP	O	D	Digital output	MIPI output (CLK+)
66	G2	DCKN	O	D	Digital output	MIPI output (CLK-)
67	G3	VDDLIF	Power	D	VDIG power supply	
68	G11	VSSHCP	GND	A	VANA GND	
69	G12	NC_C12	—	—	N.C.	
70	G13	SDI-M	I/O	D	Digital I/O	Communication data input SDI of 4-wire SPI Master
71	H1	VSSLSC	GND	D	VDIG GND	
72	H2	VSSLSC	GND	D	VDIG GND	
73	H3	VDDLIF	Power	D	VDIG power supply	
74	H10	VRL	Minus	A	Analog input	Pin for Capacitance
75	H11	VDDHCP	Power	A	VANA power supply	
76	H12	NC_C12	—	—	N.C.	
77	H13	SCK-M	O	D	Digital output	Communication clock output SCK of 4-wire SPI Master
78	J1	DMO2P	O	D	Digital output	MIPI output (DATA+)
79	J2	DMO2N	O	D	Digital output	MIPI output (DATA-)
80	J3	VSSLSC	GND	D	VDIG GND	
81	J10	VDDHCM	Power	A	VANA power supply	
82	J11	VSSHSN	GND	A	VANA GND	
83	J12	NC_J12	—	—	N.C.	
84	J13	SDO-M	O	D	Digital output	Communication data output SDO for 4-wire SPI Master
85	K1	DMO4P	O	D	Digital output	MIPI output (DATA+)
86	K2	DMO4N	O	D	Digital output	MIPI output (DATA-)
87	K3	VSSLSC	GND	D	VDIG GND	
88	K4	VLDET	O	A	Analog output	Leave this pin open (N.C.)

No.	Pin No	Symbol	I/O	A/D	Description	Remarks
89	K5	TAMON	O	A	Analog output	Leave this pin open (N.C.)
90	K6	VSSHAN	GND	A	VANA GND	
91	K7	VDDHAN	Power	A	VANA power supply	
92	K8	VDDHSN	Power	A	VANA power supply	
93	K9	VSSHSN	GND	A	VANA GND	
94	K10	VDDMSR	Power	D	VIF power supply	For drive stability
95	K11	VSSHCM	GND	A	VANA GND	
96	K12	NC_J12	—	—	N.C.	
97	K13	CMODE	I	D	Digital input	Communication I/F selection High: 4-wire / Low: I2C
98	L1	VSSLSC	GND	D	VDIG GND	
99	L2	VSSLSC	GND	D	VDIG GND	
100	L3	NC_L3	—	—	N.C.	
101	L4	NC_L4	—	—	N.C.	
102	L5	NC_L4	—	—	N.C.	
103	L6	NC_L4	—	—	N.C.	
104	L7	NC_L4	—	—	N.C.	
105	L8	NC_J12	—	—	N.C.	
106	L9	NC_J12	—	—	N.C.	
107	L10	NC_J12	—	—	N.C.	
108	L11	NC_J12	—	—	N.C.	
109	L12	NC_J12	—	—	N.C.	
110	L13	VSSLSC	GND	D	VDIG GND	
111	M1	VDDLSC	Power	D	VDIG power supply	
112	M2	VSSLSC	GND	D	VDIG GND	
113	M3	VSSLSC	GND	D	VDIG GND	
114	M4	VSSLSC	GND	D	VDIG GND	
115	M5	XCLR	I	D	Digital input	Chip clear
116	M6	SCL / SCK-S	I/O	D	Digital I/O	Communication clock input 4-wire: SCK pin / I2C: SCL pin
117	M7	NC_L4	—	—	N.C.	
118	M8	XCE-S	I	D	Digital input	Communication enable 4-wire: XCE pin / I2C: Fixed to High
119	M9	VSSLSC	GND	D	VDIG GND	
120	M10	VSSLSC	GND	D	VDIG GND	
121	M11	GPIO	I/O	D	Digital I/O	
122	M12	TENABLE	I	D	Digital input	Leave this pin open (N.C.)
123	M13	VDDLSC	Power	D	VDIG power supply	
124	N1	NC_L3	—	—	N.C.	
125	N2	VDDLCN	Power	D	VDIG power supply	
126	N3	VDDMIO	Power	D	VIF power supply	
127	N4	INCK	I	D	Digital input	Clock input
128	N5	POREN	I	D	Digital input	Leave this pin open (N.C.)
129	N6	SLASEL	I	D	Digital input	I2C slave address select
130	N7	SDA / SDI-S	I/O	D	Digital I/O	Communication data input 4-wire: SDI pin / I2C: SDA pin
131	N8	SDO-S	O	D	Digital output	Communication data output 4-wire: SDO pin / I2C: OPEN
132	N9	VDDLSC	Power	D	VDIG power supply	
133	N10	VDDMIO	Power	A/D	VIF power supply	

No.	Pin No	Symbol	I/O	A/D	Description	Remarks
134	N11	VDDLCN	Power	D	VDIG power supply	
135	N12	XVS	I/O	D	Digital I/O	Vertical sync signal
136	N13	NC_N13	—	—	N.C.	

4. Input / Output Equivalent Circuit

Symbol	Equivalent Circuit	Symbol	Equivalent Circuit
TESTA TESTB LEDFB INCK XCLR		LEDEN	
SDA SCL		SDOS SCKM SDOM XCEM1 XCEM2	
TENABLE CMODE SLASEL		LEDP LEDN	
SDIM XVS GPIO		XCES	
VLDET TAMON		POREN	
VDD***		VSS***	

Figure 3   Input / Output Equivalent Circuit

5. Peripheral Circuit Diagram
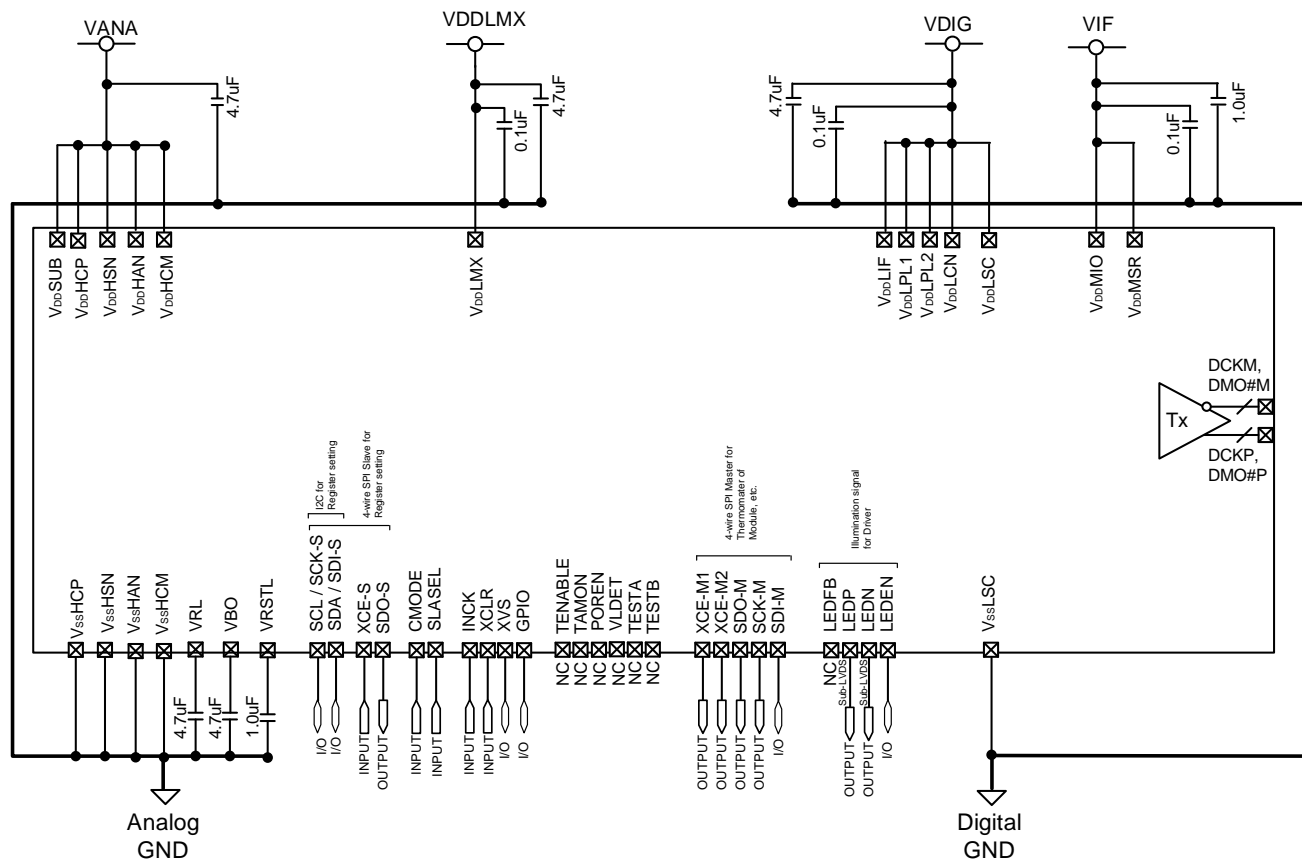
Note: The capacitor values and parts count used for decoupling of power supply lines in this diagram are determined only with Sony's testing environment. The capacitor values and/or parts count for power line decoupling may have to be reviewed and optimized by each manufacture depending on their design.

Figure 4   Peripheral Circuit (Recommended Schematics)

6. Functional Description

6-1 System Outline

IMX556 is a Time-of-Flight (ToF) camera sensor which adopts the pixel architecture based on Current Assisted Photo Demodulator (CAPD) pixel with two tap shutter offers high responsivity, and high-speed image capturing. It is embedded with backside illuminated imaging pixel, low noise analog amplifier, column parallel A/D converters which enables high speed capturing, image binning circuit, timing control circuit for frame rate, CSI-2 image data high speed serial interface, PLL oscillator, and serial communication interface to control these functions.
Several additional image processing functions and peripheral circuits are also included for easy system optimization by the users.
A onetime programmable memory is embedded in the chip for storing the user data. It has 192-bit for users, 2 K-bit as a whole.
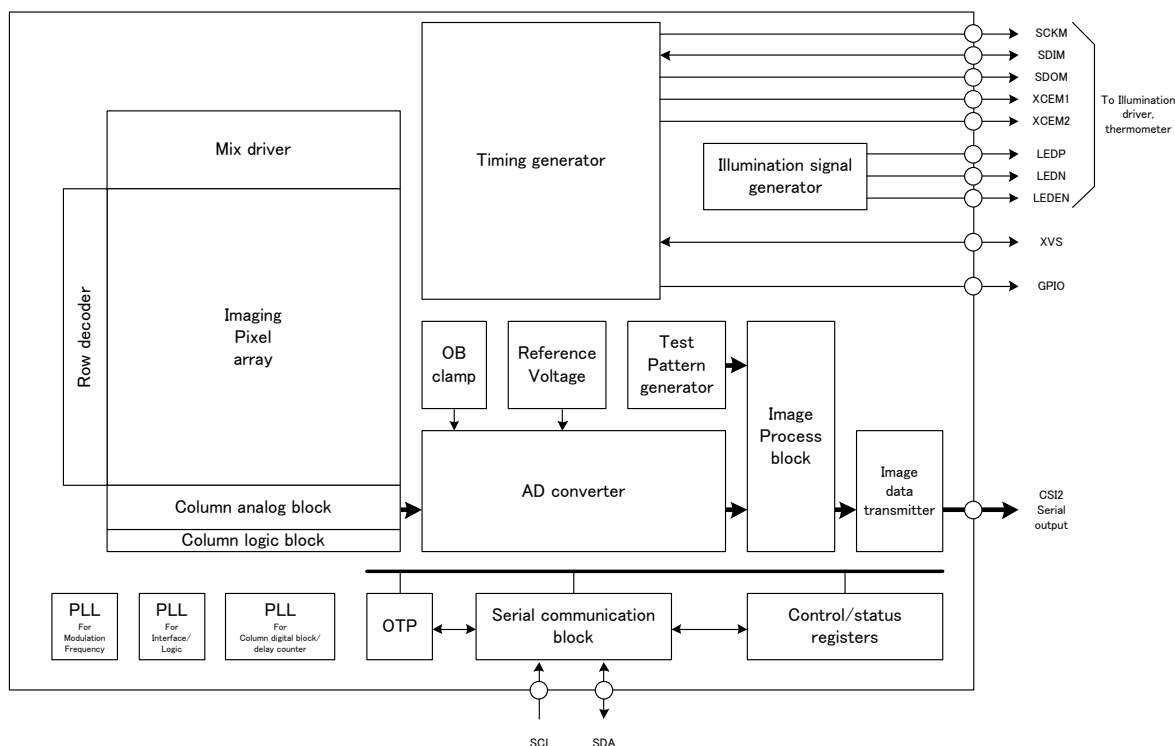

Figure 5   Overview of Functional Block Diagram

6-2 Control Register Setting by Serial Communication

This sensor can write and read the setting values of the various registers shown in the Register Map by 4-wire serial communication or I2C communication. See the Register Map for the addresses and setting values to be set.

6-2-1 Communication System Selection

The communication system is designated by the status of CMODE pin. Establish the CMODE pin status before canceling the system reset. (Do not switch this pin status during operation.) The CMODE pin can be opened. At this time, the communication method is designated to I2C.

Table 2   Communication System Selection

Pin Name	Pin processing	Communication system	Remarks
CMODE	Fixed to Low / Open	I2C	High: VIF
	Fixed to High	4-wire	Low: GND

6-2-2 I2C Communication Operation Specifications

The 2-wire serial communication method conforms to the Camera Control Interface (CCI). CCI is an I2C fast-mode compatible interface.
This I2C serial communication circuit can be used to access the control-registers and status-registers.
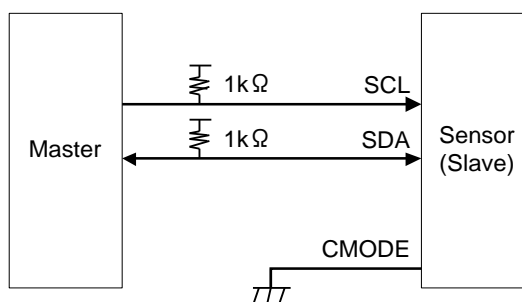
Figure 6   I2C Communication

Table 3   Description of I2C Communication Pins

Pin Name	Description
SDA	Serial data input/output pin
SCL	Serial clock input pin

The control registers and status registers of this sensor are mapped on the 16-bit address space. The register categories are shown below. Detail register information is shown in each chapter/section in this document and in Register Map.

Table 4   Abstract of Register Address Map for I2C Communication

	Address Range	Description
I²C register	0x0000 - 0x532F	Configuration register Read only and read/write dynamic register
	0x5330 - 0xFFFF	Reserved

6-2-3   I2C Communication Protocol

The 2-wire serial communication method conforms to the Camera Control Interface (CCI). CCI is an I2C fast-mode
I2C communication supports a 16-bit register address and 8-bit data message type.

| S | Slave Address [7:1] | R/W | A | Register Address [15:8] | A | Register Address [7:0] | A | Data [7:0] | A/Ā | P |

From Master to Slave
Direction dependant on operation
From Slave to Master

S = Start Condition
(Sr = Repeated Start Condition)
P = Stop Condition

A = Acknowledge
Ā = Negative Acknowledge
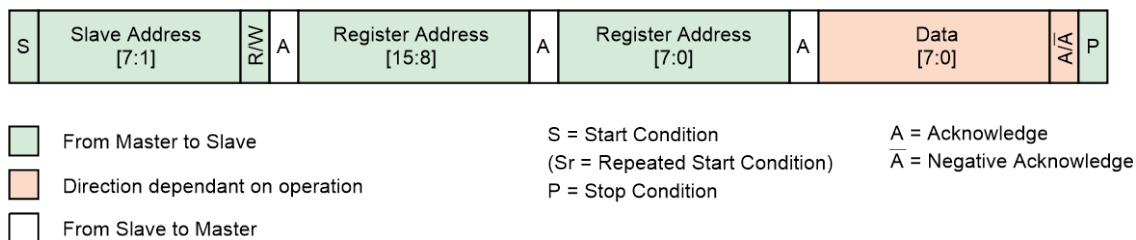
Figure 7   I2C Communication Protocol

This sensor has a default slave address shown as below. The slave address is selectable by pin connection of SLASEL and register of IIC_SLAVE_ADR_SEL. When called by the selected slave address, serial communication interface is activated. Duplication of the address on the same bus must be prevented.

Note: If you want to use Slave Address0 (or 1, 2, 3, 4) by setting SLASEL = high, you must write the OTP (IIC_SLAVE_ADR_SEL [2:0] and IIC_SLAVE_ADR0 to 4 [6:0]) referencing "OTP Manual".
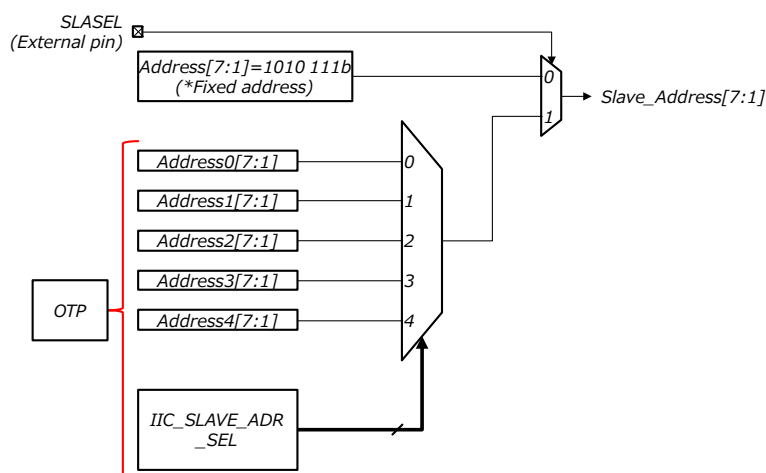
Figure 8   Slave Address (I2C)

Table 5   I2C Slave Setting

SLASEL (Pin)	IIC_SLAVE_ADR_SEL[2:0] (OTP)	Slave Address	
		[7:1]	[0]
0	—	1010 111b (Fixed value)	
1	3'h0	IIC_SLAVE_ADR0 [6:0] (OTP)	0: Write (Master → Sensor) 1: Read (Sensor → Master)
	3'h1	IIC_SLAVE_ADR1 [6:0] (OTP)	
	3'h2	IIC_SLAVE_ADR2 [6:0] (OTP)	
	3'h3	IIC_SLAVE_ADR3 [6:0] (OTP)	
	3'h4	IIC_SLAVE_ADR4 [6:0] (OTP)	

6-2-4   Specification of Communication Bus State

6-2-4-1   Idle State

Idle state is specified as follows; neither master nor slave device drives the SDA or SCL, and these bus lines are pulled up to VDD(VIF) via register.

6-2-4-2   Issue "Start Condition"

While the I2C communication bus is in idle state, master device (ex. subsequent image processing LSI, etc.) issues the communication-start: Start condition S by driving SDA from "High" to "Low" level. Serial data are transmitted in 8-bit-unit MSB first format. For every 8-bit data transmission, the slave device issues acknowledge or negative acknowledge (explained later). A (acknowledge)/Ā (negative acknowledge).

Data (SDA) is transmitted in sync with the SCL cycle. SDA toggles while SCL is "Low "and holds the value while SCL is "High".
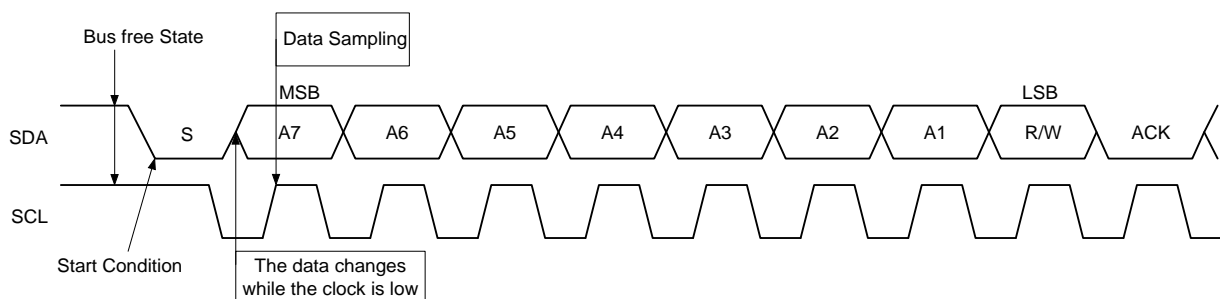
Figure 9 Start Condition

6-2-4-3   Issue "Stop Condition"

After A (acknowledge)/Ā (negative acknowledge) and while SCL is High, master device issues communication-stop condition: "Stop condition" P by driving SDA from a low to high level. After issuing a "Stop condition", master release I2C serial bus enters into an idle state.
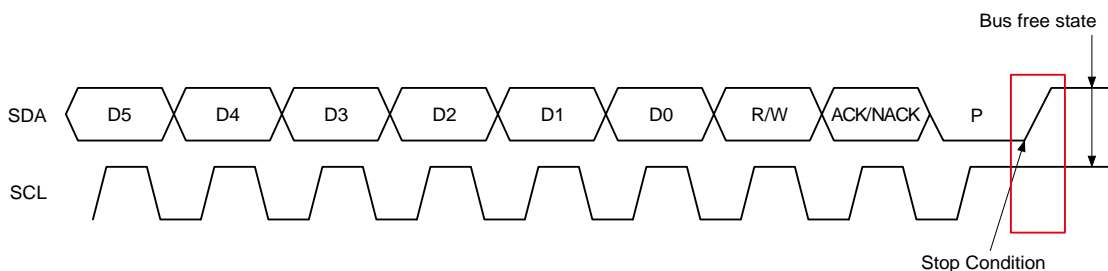
Figure 10 Stop Condition

6-2-4-4   Issue "Repeated Start Condition"

Master device can issue a start condition after previous transaction without issuing a stop condition. In this case this start condition is recognized as the "Repeated started condition" Sr.
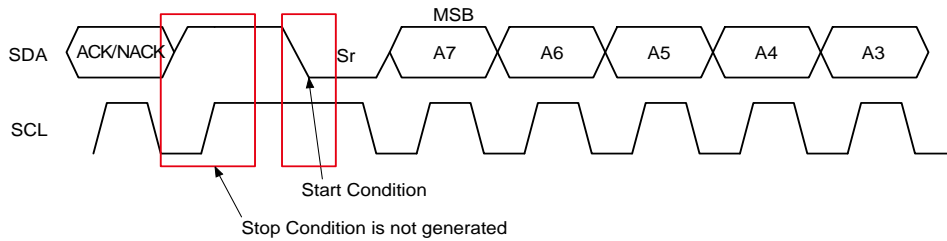
Figure 11 Repeated Start Condition

6-2-4-5   Issue "Acknowledge/Negative Acknowledge"

After transmitting each byte, a master or slave device issues an acknowledgement or negative acknowledgement and can release the bus to the idle state. When negative acknowledgement is issued, the master must issue the stop and terminate the communication immediately.
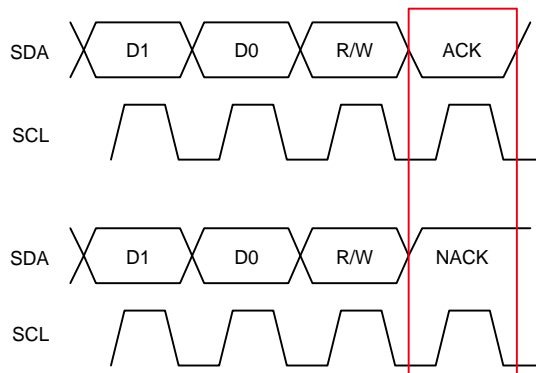
Figure 12 Acknowledge and Negative Acknowledge

6-2-5 Read/Write Operation of I2C Serial Communication

This sensor has an index function that indicates which address is to be accessed. When reading/writing the value from/to a requested address, the master must set the address value to the index. Index value is designated by 2 bytes of dummy write operation after the slave address transmission. The index value is automatically incremented by "one" with the "Acknowledge/Negative Acknowledge" for the following data transfer.
This sensor supports four read modes and two write modes being compliant to Camera Control Interface (CCI).

Table 6 Read/Write Operations Supported by I2C Serial Communication

|		
	1	CCI single read from random location (Single read from an arbitrary address)
	2	CCI single read from current location (Single read from the held address)
Access mode	3	CCI sequential read starting from random location (Sequential read starting from an arbitrary address)
	4	CCI sequential read starting from current location (Sequential read starting from the held address)
	5	CCI single write to random location (Single write to an arbitrary address)
	6	CCI sequential write starting from random location (Sequential write starting from an arbitrary address)

6-2-5-1 CCI Single Read from Random Location

The upper part of the below figure below shows the sensor internal index value, and the lower part shows the SDA data flow. The master sets the sensor index value of M by designating the sensor slave address with a write request. Then the Master generates the Start condition. The Start condition is generated without generating the Stop condition, so it becomes the Repeated Start condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the data at the index address on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop condition to end the communication.

When reading single datum from the requested address register, the master device starts write-operation with the slave address of this sensor and by making 2 bytes of dummy write master sets the address value (M) to the index. After that master issues the "start condition" again instead of issuing a "stop condition". This "start condition" is recognized as "repeated start condition". Then transmitting the read request with the slave address, this sensor issues the "Acknowledge" and starts transmitting the register value from indexed address (M). Master issues the "Negative Acknowledge" and "stop condition" after receiving the transmission.
The figure below indicates the transition of index value and data on SDA line.
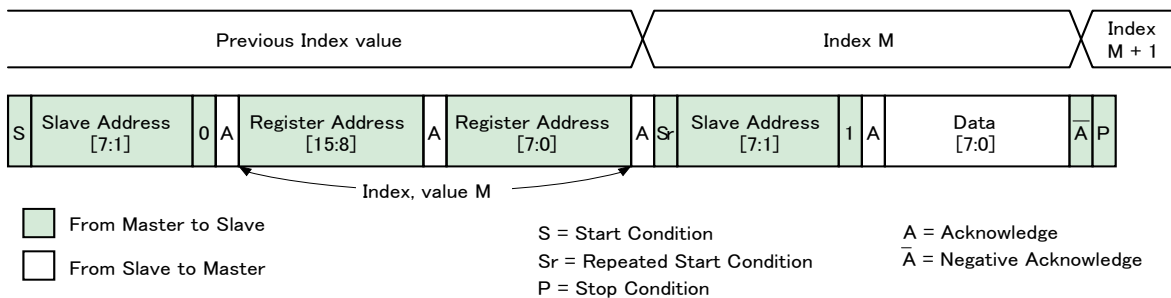
Figure 13 CCI Single Read from Random Location

6-2-5-2   CCI Single Read from Current Location

When master transmits slave address, but does not designate an index, the previous value is held. And the index value is incremented at the "Acknowledge/Negative Acknowledge" after reading/writing the register value. When master knows the current index value is set to the requested address, master transmits the slave address and read request, then the value in the register appears on SDA line right after the "Acknowledge" issued by this sensor. Master issues the "Negative Acknowledge" and "Stop" and terminates the communication. Since the index value is incremented by "one" with this "Negative Acknowledge", master can read the register value of the next address with the same procedure.
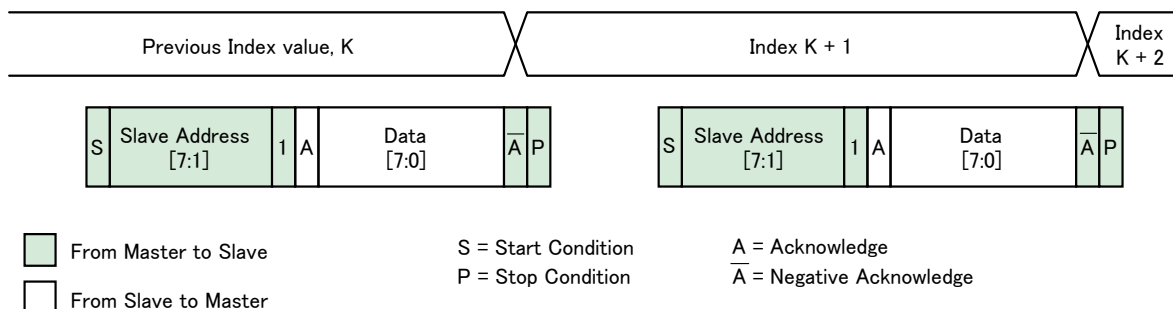
Figure 14 CCI Single Read from Current Location

6-2-5-3   CCI Sequential Read Starting from Random Location

When reading the data from an arbitrary address sequentially, master reads the first data by the similar procedure to "CCI single read from random location" but issues the "Acknowledge" instead of "Negative Acknowledge", the index is incremented by "one" with this "Acknowledge" then master can repeat the read operation. This operation is terminated when master issues the "Negative Acknowledge", "Stop condition", and the communication is terminated.
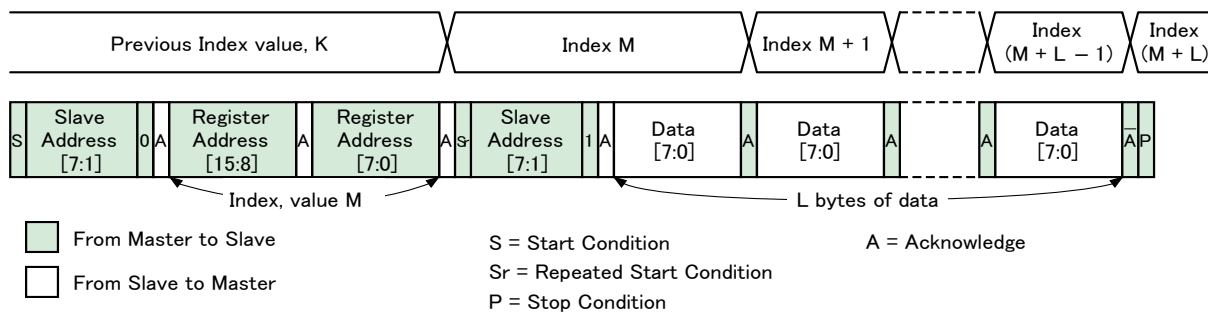
Figure 15 CCI Sequential Read Starting from Random Location

6-2-5-4 CCI Sequential Read Starting from Current Location

When master knows the current index value is set to the requested address, master transmits the slave address and read request, then the value from the register appears on SDA line right after the "Acknowledge" issued by this sensor. Master issues the "Acknowledge" after receiving 1-byte of the data and this sensor continuously transmits the data from the next address of register since the index value is incremented by "one" with this "Acknowledge". By repeating issue of the "Acknowledge" for every 1-byte reading, master can read the data sequentially. After reading necessary bytes of data, master issues "Negative Acknowledge" and "stop condition" and then terminates the communication.
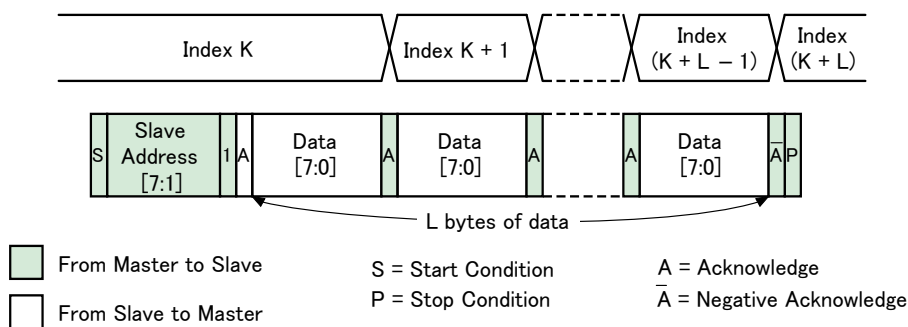
Figure 16 CCI Sequential Read Starting from Current Location

6-2-5-5 CCI Single Write to Random Location

When writing single datum to a register of target address, the master device starts write-operation with the slave address of this sensor and by making 2-bytes of dummy write master sets the address value (M) to the index. And then master transmits the data to be written to the register addressed by index value. Master issues "stop condition" after it transmits the data and terminates the communication.
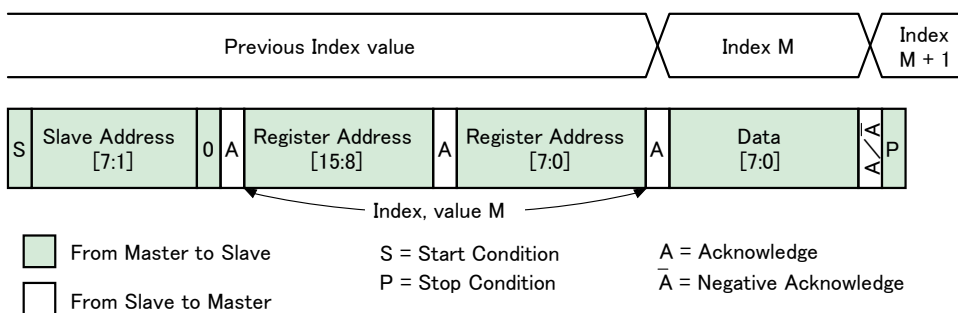
Figure 17 CCI Single Write to Random Location

6-2-5-6   CCI Sequential Write Starting from Random Location

When master writes the data sequentially from the requested address, master uses a similar procedure to do "CCI single write to random location" and without issuing a "stop condition" and continuously transmits the data after each "Acknowledge" issued. This sensor issues "Acknowledge" for each 1-byte write operation. After transmitting necessary data, master issues a "stop condition" and terminates the communication.

| From Master to Slave | S = Start Condition | A = Acknowledge |
| From Slave to Master | P = Stop Condition | $\overline{A}$ = Negative Acknowledge |
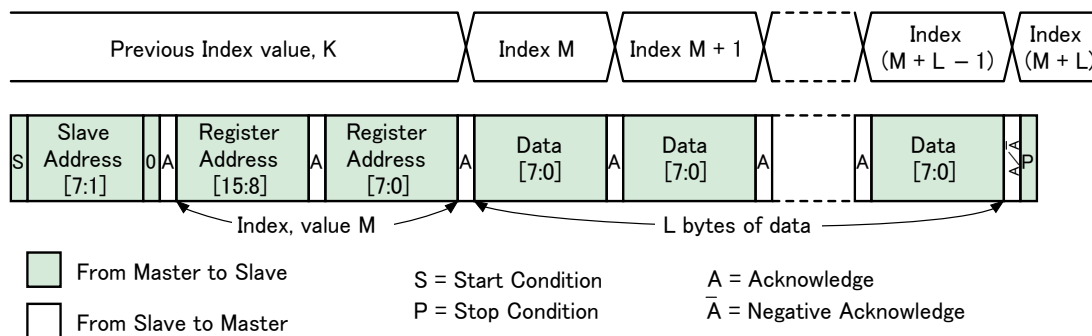
Figure 18 CCI Sequential Write Starting from Random Location

6-2-6 I2C Serial Communication Register Update Timing

There are two types of registers in terms of the update timing of the transmitted data: the immediate type and the double buffered type. For immediate type registers, the transmitted data will be written to the registers immediately. As for the v-latched or double buffered type registers, the actual update timing of the register contents are controlled to the proper timing and become valid in the next frame. Users can transmit the commands regardless of the internal update timing of this sensor. The registers of double buffered types are indicated with "✔" mark at the "Grouped Parameter Hold" column of "IMX556_Register_Map_Ver**.xlsx".

Parameters are updated
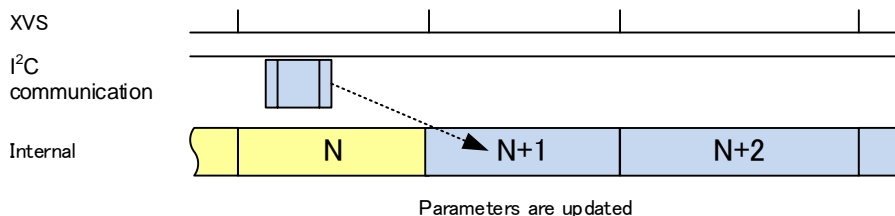
Figure 19 I2C Serial Communication Register Update Timing Diagram

(v-latched type registers)

6-2-7   SPI Slave 4-wire Serial Communication Operation Specifications

SPI 4-wire serial communication uses to access the control-registers and status-registers in the sensor. The figure below shows the pin for 4-wire serial communication.
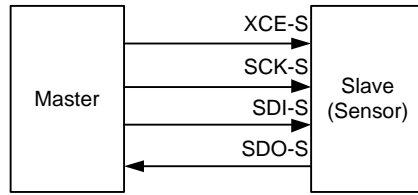
Figure 20   SPI Slave 4-wire Communication

6-2-8   SPI Slave 4-wire Serial Communication Protocol

1. Follow the communication procedure below when writing registers.
2. Set XCE Low to enable the chip's communication function. Serial data input is executed using SCK and SDI.
3. Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
4. Input the start address value to the first byte and second byte.
    Write: Input the address as it is (enable Write)
    Read: Input the address which MSB bit is change to 1 from original (disable Write)
5. Input the data to the third and subsequent bytes. The data in the third byte is written to the register address designated by the second byte, and the register address is automatically incremented thereafter when writing the data for the fourth and subsequent bytes.
6. The register values from the start address are output from the SDO pin. The register values before the write operation are output. The actual register values are the input data in the case of Write (MSB = 0).
    Input data is ignored in the case of Read (MSB = 1).
7. Set XCE High to end communication.

Note) When writing data to multiple registers with discontinuous addresses, access to undesired registers can be avoided by repeating the above procedure multiple times.
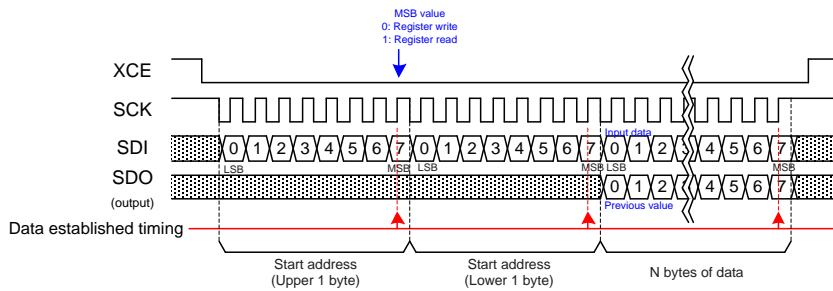
Figure 21   SPI Slave 4-wire Serial Communication (Continuous Addresses)
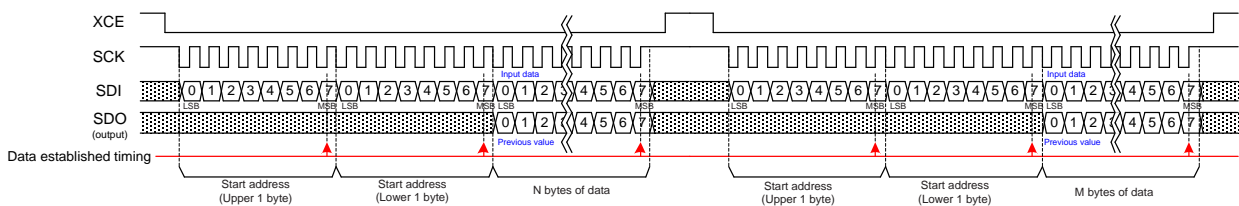
Figure 22   SPI Slave 4-wire Serial Communication (Discontinuous Addresses)

6-2-9 Register Value Reflection Timing to Output Data

The 2-wire serial communication method conforms to the Camera Control Interface(CCI). CCI is an I2C fast-mode
Perform serial communication in the communication period which is shown below.
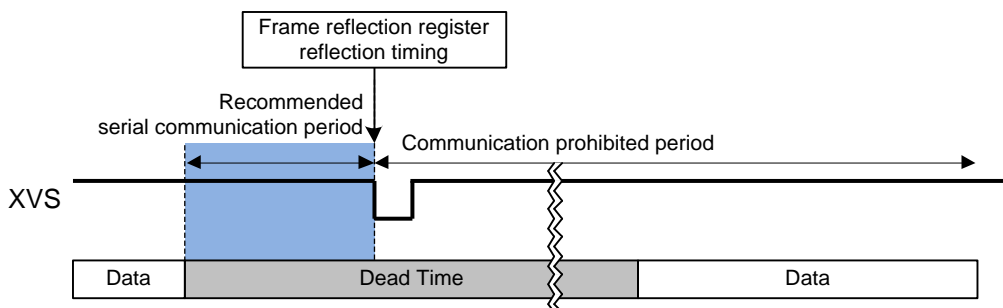
Figure 23   Register Communication Timing

6-2-10 Grouped Parameter Hold Setting

The image shooting parameters are assigned with many registers and they need to be changed within one frame
period of the image. However, the communication speed is limited and setting al of necessary registers might not
be completed. So, the v-latched type registers have the "group CSI_LANE_MODE parameter hold" function to
behave to be updated at once. While "Grouped parameter hold" register to "1" the transmitted data are held in the
buffer registers and after resets "Group parameter hold" register to "0", imaging parameter register values are
updated as if they are transmitted at the same time and realize a smooth transition for changing the imaging
condition.

Table 7 Grouped Parameter Hold Function

Address	Bit	Register Name	Description
0x0102	[0]	GRP_PARAM_HOLD	This register is a hold control register for updating multiple parameters within the same frame. 0: hold release 1: hold
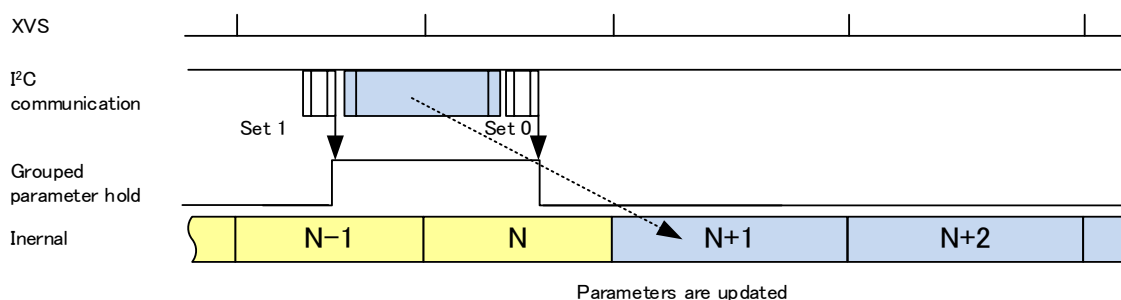
Figure 24 GRP_PARAM_HOLD Function Timing Diagram

6-2-11 SPI Master Serial Communication Operation Specifications

SPI Master serial communication uses to access the setting registers of the peripheral device from the sensor.
The figure below shows the system with SPI-Master control with SPI Master serial communication.
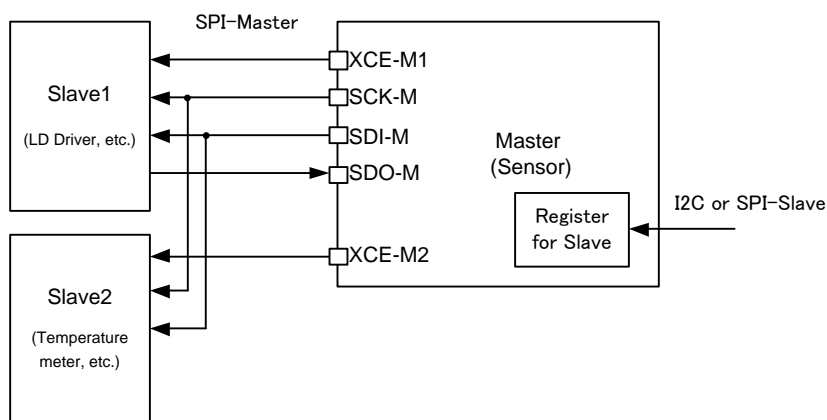
Figure 25   SPI Master Communication

When SPI Master 3-wire connection is used in your system, SDO-M terminal needs to be NC.
The sending address and value must be sent in advance by I2C or SPI-Slave from the system controller, etc.
When Start Trigger setting register in the sensor is set to "Start transaction", the sensor sends the communication by SPI-Master according to the sensor's register values.
The sensor can add the data which is acquired from SPI-Master into the output as MIPI Embedded data. If the temperature meter is connected with the sensor, the sensor can add its temperature data in embedded data line.

Refer to "SPI Master Manual" for detail specification and how to send the data of SPI-Master.

Table 8   Setting Registers for SPI Master

Address	Bit	Register Name	Description
0x0400	[0]	SEND1_STTRIG	Transmit channel 1 Start trigger 0: not start 1: start transaction in case of SEND1_CTRL_STTTRIG_SEL = 0
0x0401	[0]	SEND1_ENABLE	Transmit channel 1 Enable 0: Off 1: On
0x0403	[6:5]	SEND1_CTRL_DEVSEL	Select of Slave Device for Transmit channel 1 2'b00 : not select 2'b01 : device1 (SS1) 2'b10 : device2 (SS2) 2'b11 : device1 (SS1)
	[7]	SEND1_CTRL_STTRIG_SEL	Select of start trigger 0: start by register (SEND1_STTRIG) 1: start by internal sync signal (LDD_THRM_TIM_W)
0x0405	[7:0]	SEND1_DIVIDE	Number of transactions for Transmit channel 1 8'h00 : transaction x 1 8'h01 : transaction x 2 … 8'h0f : transaction x 16 8'h1x : prohibit
0x0407	[7:0]	SEND1_TX_BUF_NO	Start pointer of TX buffer for Transmit channel 1 8'd0 - 8'd46 is only available.
0x0410	[0]	SEND2_STTRIG	Transmit channel 2 Start trigger 0: not start 1: start transaction in case of SEND2_CTRL_STTTRIG_SEL = 0

Address	Bit	Register Name	Description
0x0411	[0]	SEND2_ENABLE	Transmit channel 2 Enable 0: Off 1: On
0x0413	[6:5]	SEND2_CTRL_DEVSEL	Select of Slave Device for Transmit channel 2 2'b00 : not select 2'b01 : device1 (SS1) 2'b10 : device2 (SS2) 2'b11 : device1 (SS1)
	[7]	SEND2_CTRL_STTRIG_SEL	Select of start trigger 0 : start by register (SEND2_STTRIG) 1 : start by internal sync signal (LDD_THRM_TIM_W)
0x0415	[7:0]	SEND2_DIVIDE	Number of transactions for Transmit channel 2 8'h00 : transaction x 1 8'h01 : transaction x 2 … 8'h0f : transaction x 16 8'h1x : prohibit
0x0417	[7:0]	SEND2_TX_BUF_NO	Start pointer of TX buffer for Transmit channel 2 8'd0 - 8'd46 is only available.
0x0420	[0]	THERMO_STTRIG	Thermometer channel Start trigger 0 : not start 1 : start transaction in case of THERMO_CTRL_STTRIG_SEL = 0
0x0421	[0]	THERMO_ENABLE	Thermometer channel Enable 0: Off 1: On
0x0423	[6:5]	THERMO_CTRL_DEVSEL	Select of Slave Device for Thermometer channel 2'b00 : not select 2'b01 : device1 (SS1) 2'b10 : device2 (SS2) 2'b11 : device1 (SS1)
	[7]	THERMO_CTRL_STTRIG_SEL	Select of start trigger 0: start by register (THERMO_STTRIG) 1: start by internal sync signal (LDD_THRM_TIM_R)
0x0425	[7:0]	THERMO_DIVIDE	Number of transactions for Thermometer channel 8'h00 : transaction x 1 8'h01 : transaction x 2 … 8'h0f : transaction x 16 8'h1x : prohibit
0x0426	[7:0]	THERMO_RX_BUF_NO	Start pointer of RX buffer for Thermometer channel 8'd0 - 8'd15 is only available.
0x0427	[7:0]	THERMO_TX_BUF_NO	Start pointer of TX buffer for Thermometer channel 8'd0 - 8'd46 is only available.
0x042A	[7:0]	THERMO_BIDIR_3WIO	Number of Tx byte in Tx/Rx CH 8'd0 : All Rx 8'd1 : 1st byte is Tx, after Rx 8'd2 : 1st,2nd byte is Tx, after Rx … 8'd48 : 1st - 48th byte is Tx, after Rx 8'd49 - 8'd255 is prohibited.
0x0430	[0]	GENERAL_STTRIG	General channel Start trigger 0: not start 1: start transaction in case of GENERAL_CTRL_STTRIG_SEL = 0
0x0431	[0]	GENERAL_ENABLE	General channel Enable 0 : Off 1 : On

Address	Bit	Register Name	Description
0x0433	[6:5]	GENERAL_CTRL_DEVSEL	Select of Slave Device for General channel 2'b00 : not select 2'b01 : device1 (SS1) 2'b10 : device2 (SS2) 2'b11 : device1 (SS1)
0x0435	[7:0]	GENERAL_DIVIDE	Number of transactions for General channel 8'h00 : transaction x 1 8'h01 : transaction x 2 ・・・ 8'h0f : transaction x 16 8'h1x : prohibit
0x0436	[7:0]	GENERAL_RX_BUF_NO	Start pointer of RX buffer for General channel 8'd0 - 8'd15 is only available.
0x0437	[7:0]	GENERAL_TX_BUF_NO	Start pointer of TX buffer for General channel 8'd0 - 8'd46 is only available.
0x043A	[7:0]	GENERAL_BIDIR_3WIO	Number of Tx byte in Tx/Rx CH 8'd0 : All Rx 8'd1 : 1st byte is Tx, after Rx 8'd2 : 1st,2nd byte is Tx, after Rx ・・・ 8'd48 : 1st - 48th byte is Tx, after Rx 8'd49 - 8'd255 is prohibited.
0x0443	[7:0]	COMMON_THERMO_STPOINT	Start point of Temp Data 8'd0 - 8'd15 is only available.
0x0450	[0]	SS1_CPHA	Slave Device 1 Setting 0 : sample data when idle to active 1 : sample data when active to idle
	[1]	SS1_CPOL	Slave Device 1 Setting 0 : Low : idle High : active (positive pulse) 1 : High : idle Low : active (negative pulse)
	[2]	SS1_POL	Slave Device 1 Setting for select signal(XCEM1) 0 : Low : active (negative pulse) 1 : High : active (positive pulse)
	[3]	SS1_FIRSTBIT	Slave Device 1 Setting 0 : LSB first 1 : MSB first
	[4]	SS1_BIDIR_WIRE	Set the SPI connection to slave device 1 1: SPI 4-wire connection (SDO and SDI terminal are for unidirectional communication) 0: SPI 3-wire connection (SDO terminal is for SDO/ SDI bidirectional communication)
	[6]	SS1_KGS_LDD	Slave Device 1 Setting 0 : normal mode 1 : Rx timing 1/2SCK delay
0x0454	[0]	SS2_CPHA	Slave Device 2 Setting 0 : sample data when idle to active 1 : sample data when active to idle
	[1]	SS2_CPOL	Slave Device 2 Setting 0 : Low : idle High : active (positive pulse) 1 : High : idle Low : active (negative pulse)
	[4]	SS2_BIDIR_WIRE	Set the SPI connection to slave device 2 1: SPI 4-wire connection (SDO and SDI terminal are for unidirectional communication) 0: SPI 3-wire connection (SDO terminal is for SDO/ SDI bidirectional communication)
	[6]	SS2_KGS_LDD	Slave Device 2 Setting 0: normal mode 1: Rx timing 1/2SCK delay

Address	Bit	Register Name	Description
0x0500 to 0x052F	[7:0]	SPI_TX_DATA00 to SPI_TX_DATA47	Tx buffer 00 - 47
0x0580 to 0x058F	[7:0]	SPI_RX_DATA00 to SPI_RX_DATA15	Rx buffer 00 - 15
0x40E6	[0]	LDD_THRM_TIM_W_EN	Internal sync enable for SPI-Master (Transmit channel 1 and 2) 0: Off 1: On
0x40E7	[0]	LDD_THRM_TIM_W_SEL	Internal sync timing for SPI-Master (Transmit channel 1 and 2) 0: start of phase 1: start of readout
0x40E8	[7:0]	LDD_THRM_TIM_W_H	Internal sync timing for SPI-Master (Transmit channel 1 and 2) * 32'hFFFFFFFF is prohibited.
0x40E9	[7:0]		
0x40EA	[7:0]		
0x40EB	[7:0]		
0x40EC	[0]	LDD_THRM_TIM_R_EN	Internal sync enable for SPI-Master (Thermometer channel and General channel) 0 : Off 1 : On
0x40ED	[0]	LDD_THRM_TIM_R_SEL	Internal sync timing for SPI-Master (Thermometer channel and General channel) 0 : start of phase 1 : start of readout
0x40F0	[7:0]	LDD_THRM_TIM_R_H	Internal sync timing for SPI-Master (Thermometer channel and General channel) * 32'hFFFFFFFF is prohibited.
0x40F1	[7:0]		
0x40F2	[7:0]		
0x40F3	[7:0]		

6-3   Image Readout Operation

By setting the parameters of PLL, image size, start/end position of the imaging area, direction of reading image, binning, integration time, and output format via 2-wire serial communication, IMX556 outputs the image data.

6-3-1   Physical Alignment of Imaging Pixel Array (Top View)

The figure below shows the physical alignment of the imaging pixel array with A1 pin located at the upper left corner.
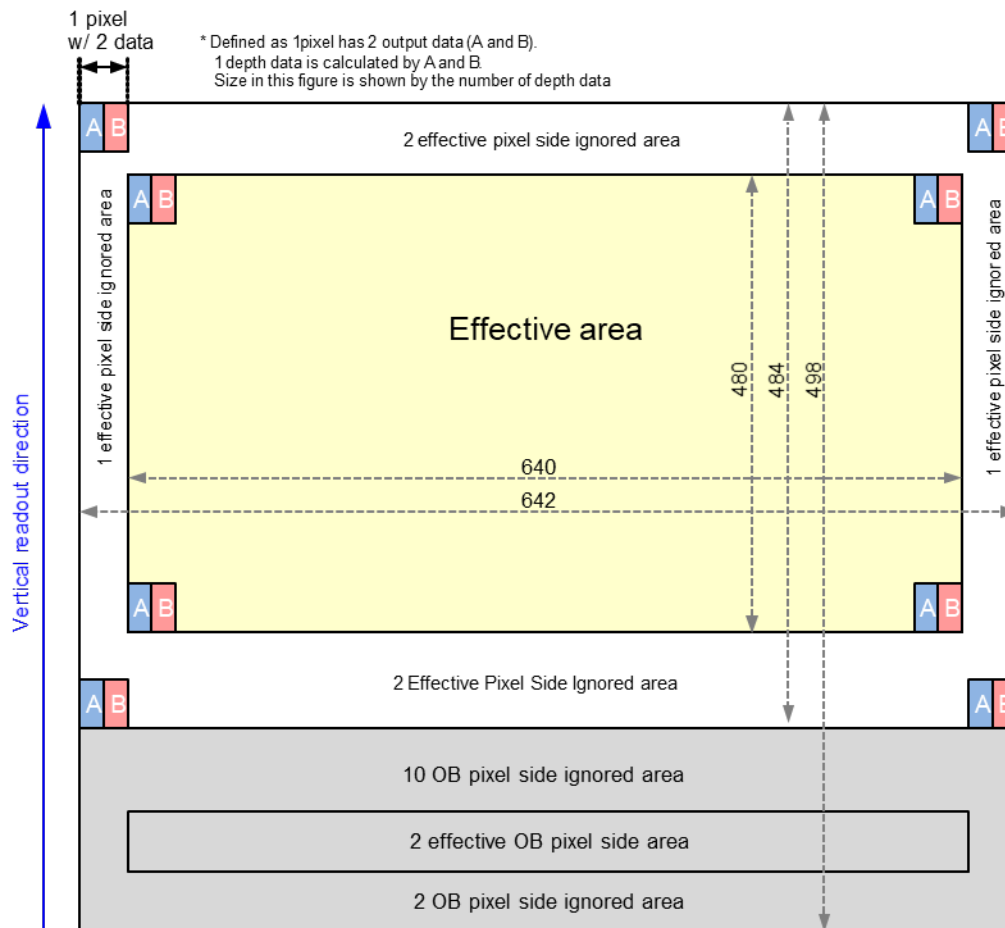
Figure 26   Physical Alignment of the Imaging Pixel Array (Top View)

6-3-2 Order of Reading Image Date

Default readout direction is shown in the figure below.

Default readout direction
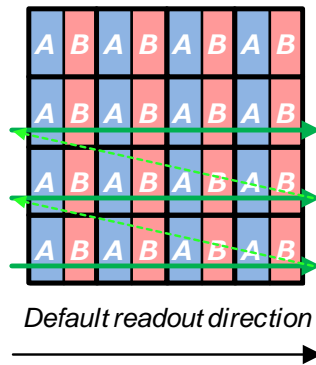
Figure 27   Readout Direction

6-4 Output Image Format

This is the output image diagram of full pixel output mode. Image data is output from the upper left corner of the diagram.
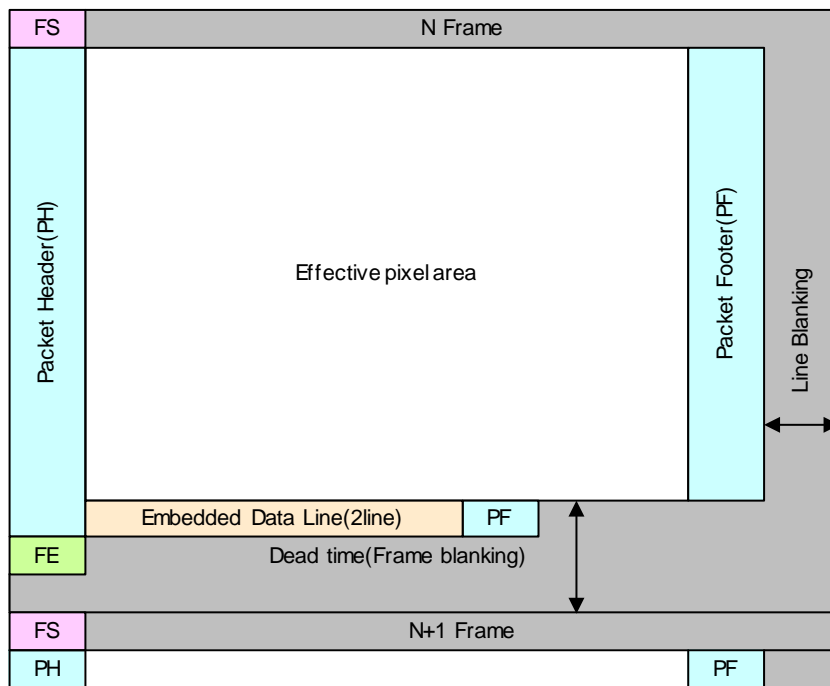
Figure 28   Full Pixel Output Mode Data Structure
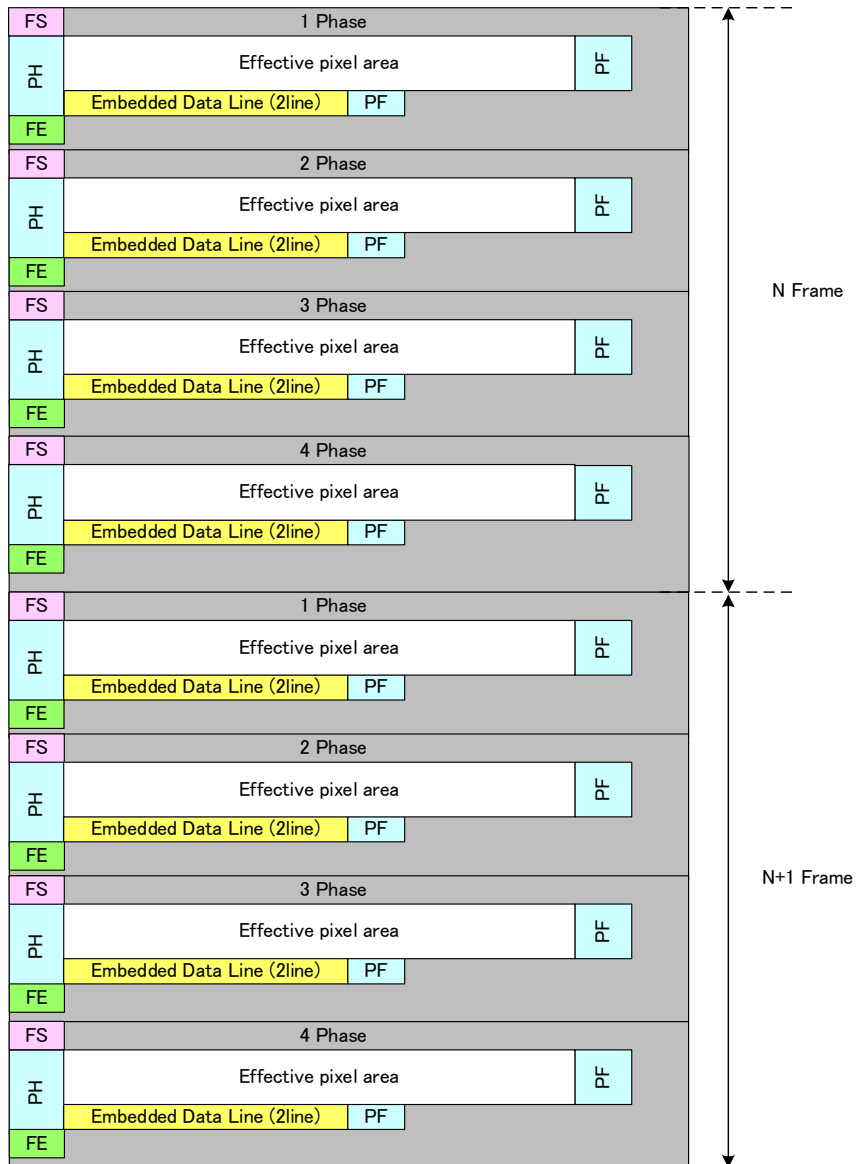
Figure 29   Frame Start (FS) and Frame End (FE) Output Data Structure

6-4-1   Image Size of Mode

IMX556 can capture and output full size, cropped image. Examples are shown in the table below. Definitions of each parameter are shown in the below figure.
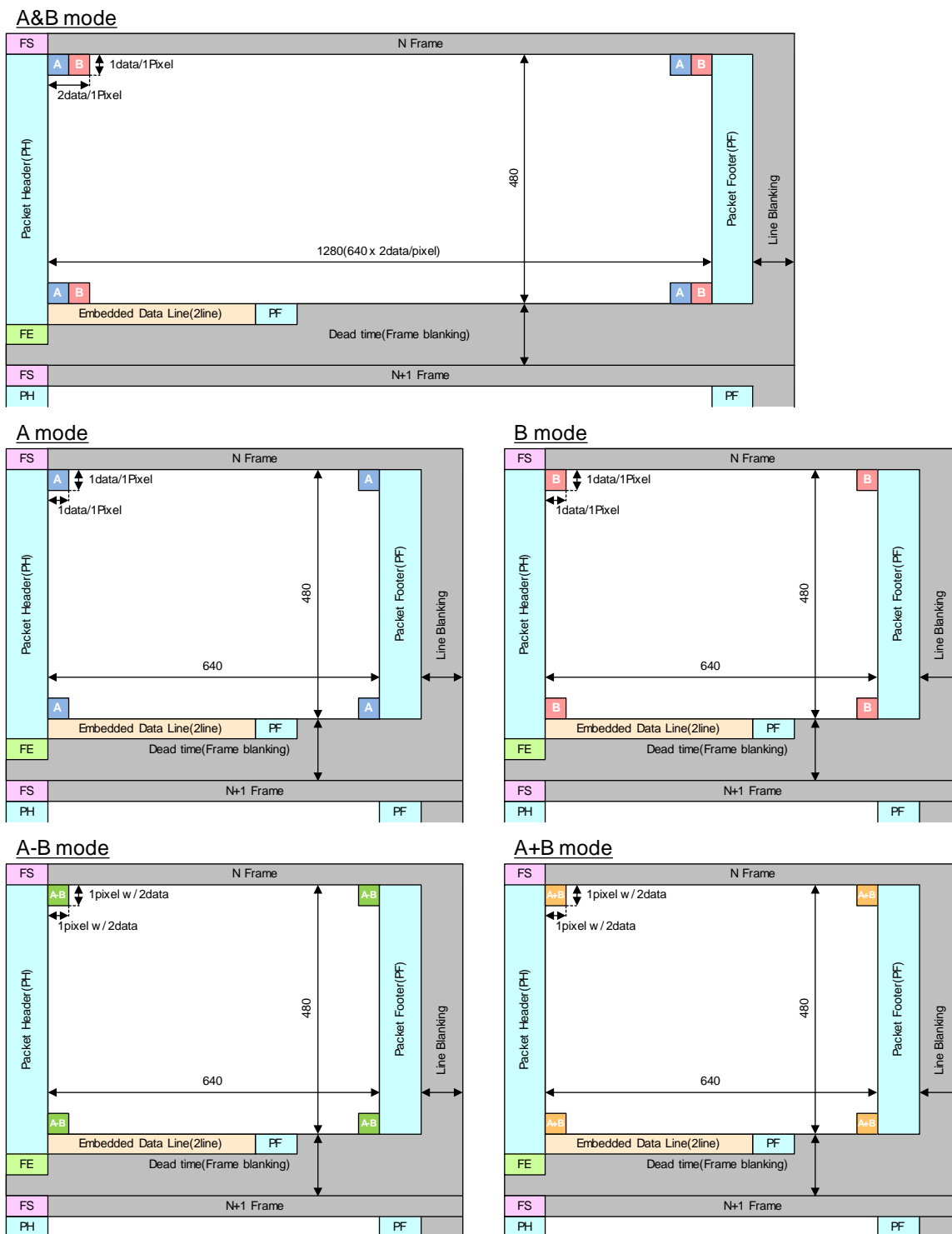
Figure 30   Image Size Parameter Definition

Table 9   Modes and Image Sizes

		Modes			
		Full pixel No Binning A&B mode		Full pixel No Binning A,B,A-B,A+B mode	
Number of vertical lines in imaging area		480		480	
Number of horizontal pixels in effective area		1280		640	
Number of lines and start position		Start position	Number of lines	Start position	Number of lines
Name of the areas	Frame start	1	1	1	1
	Number of vertical pixels in effective area	2	480	2	480
	Embedded data lines	482	2	482	2
	Frame end	484	1	484	1

6-4-2   Contents of Packet Header

The contents of the first byte in the packet header (data identifier) and the corresponding register settings are described in the table below.
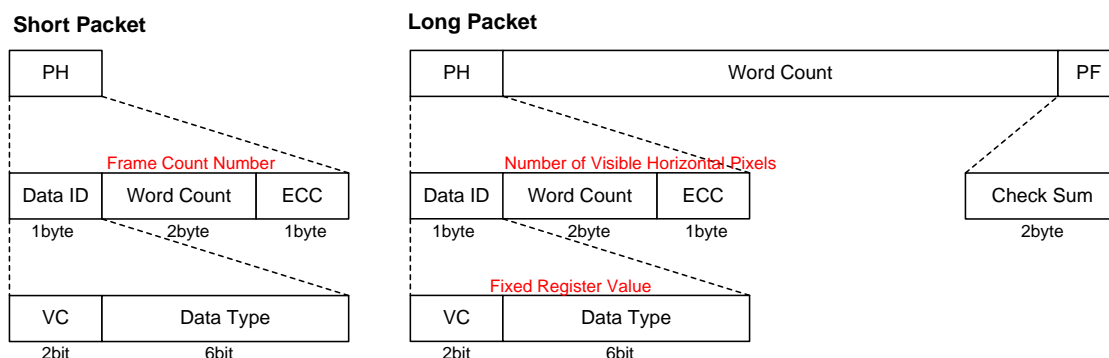
Figure 31 Short Packet & Long Packet Structures
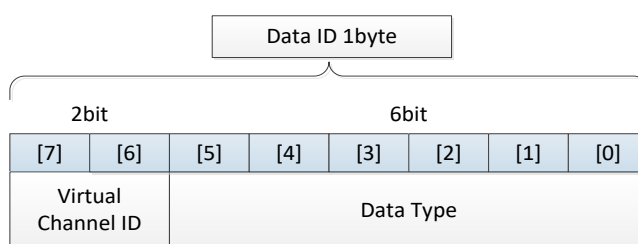
Figure 32 Configuration of Data ID

Table 10 Data Identifier

	Bit assignment	Value	Description	Corresponding Reg(I2C)	Note
Packet header	[7:6] Virtual Channel ID	2'h0(Default)		0x0810 CSI_CHID [1:0]	Refers LSB 2bits
	[5:0] Data types	6'h00	Frame Start Code	NA	
		6'h01	Frame End Code	NA	
		6'h12	Embedded Data	NA	For embedded data line
		6'h2C	RAW12	NA	

6-4-3 Data Type

Types of data in each line are shown below.

Table 11 Image Pixel Area and Data Type

Image Pixel Area	Data Type
Embedded data lines	Embedded data
Effective pixels	RAW12

6-4-4 Embedded Data Line Control

It is possible to output certain 2-wire serial register contents on the 2 lines just before the FE sync code of the frame. Undefined value is output when not outputting embedded data.

Table 12 Embedded Data Line Control

	Address	Bit	Register Name	Description
I²C register	0x2c0c	[7:0]	EBD_X_OUT_SIZE[10:3]	Pixel number of H direction for outputting the EBD data
	0x2c0d	[7:5]	EBD_X_OUT_SIZE[2:0]	(<= 131d are prohibited)
	0x3c18	[2:0]	EBD_SIZE_V	0 is no EBD 1 is EBD 1 line 2 is EBD 2 line others are prohibited

The sequence of EBD in each output format is as shown in the figures below.
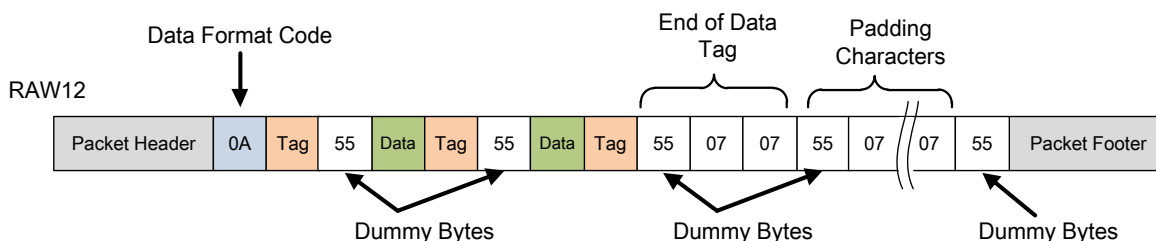
Figure 33 Embedded Data Lines Alignment in RAW12 Mode

Addresses and the end of register values are distinguished by "Tags" embedded in the data sequence.

Table 13 Embedded Data Line Tag

Tag	Data Byte Description
07h	End of Data (Data Byte Value = 07H)
aah	CCI Register Index MSB [15:8]
a5h	CCI Register Index LSB [7:0]
5ah	Auto increment the CCI index after the data byte – valid data Data byte contains valid CCI register data

Readout Start Position

Default readout position of IMX556 starts from the lower left when PIN1 is placed at the upper right corner. Because the lens inverts the image vertically and horizontally.
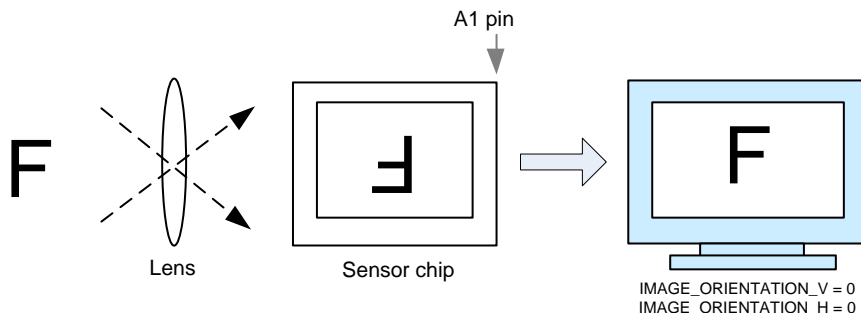
Figure 34 Readout Start Position

Vertical flip and horizontal mirror readout modes can be specified by the register below. And when readout start and end positions are matching the readout size, the same area is displayed when flipping/mirroring the image.
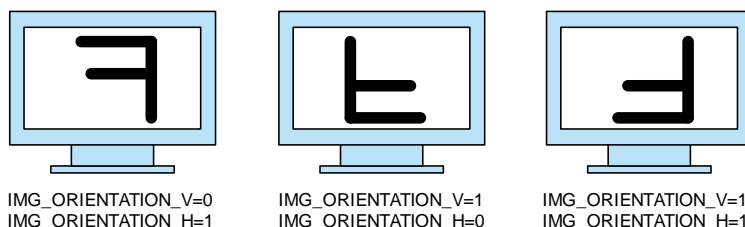
Figure 35 Readout Image for Each Combination of Flip and Mirror

6-5 Image Signal Interface (MIPI Transmitter)

IMX556 outputs image signal by CSI-2 high speed serial interface consisted of one pair of clock line and four pairs of data line. See MIPI Alliance Specification for D-PHY version 1.20.00 for details.

Because signal is transmitted by differential pair, impedance (generally 100 Ω) between differential pair near the receiver side during HS mode is required. Otherwise, select receiver with build-in impedance between differential pair. Different delay time of differential pairs may reduce the input timing margin of ISP device, which leads to malfunction. Therefore, delay time within and among differential pairs must be as similar as possible in layout.

6-6   Sequencer

- Integration time can be set between 0.25 to 1000us.
- The setting range of the number of phases in a frame is 1 to 8. The angle difference for each phase between the illumination signal modulation (MOD) and the sensor exposure signal mixing (MIX) can be set in 45[deg] steps.
- Frame & phase timing: the dead time between each phase and between each micro frame can be set separately, therefore the dead time can be set to a lumped dead time after all phases (all phases in a frame are in a short sequence) or a divided dead time (phases are spread in a frame).
- MIX (Pixel exposure signals) and MOD (Illumination signals) can be set to static high/low during a phase independently.

6-6-1   Frame Structure

The definition of each frame for Phase, Micro frame and Frame (= depth frame) shows below. Phase is composed of Reset Sequence, Integration and Read Out. The micro frame includes a number of phases, and the maximum number of phases is 8. The frame (depth frame) is composed of the initial startup period and Micro frame. Use Start Up Pre time setting (DPTH_SU_NUM_WAIT_A) when Frame start timing is needed to change. Changing Start Up period (DPTH_SU_NUM) is prohibited. IDLE time setting (SUB_VBLK*) can control the dead time at the end of each phases. The setting range of IDLE time is related to HMAX. HMAX is different from each mode. Refer to "Readout Mode" section below.
The transition to Wait Vsync state is performed after micro frame is completed.
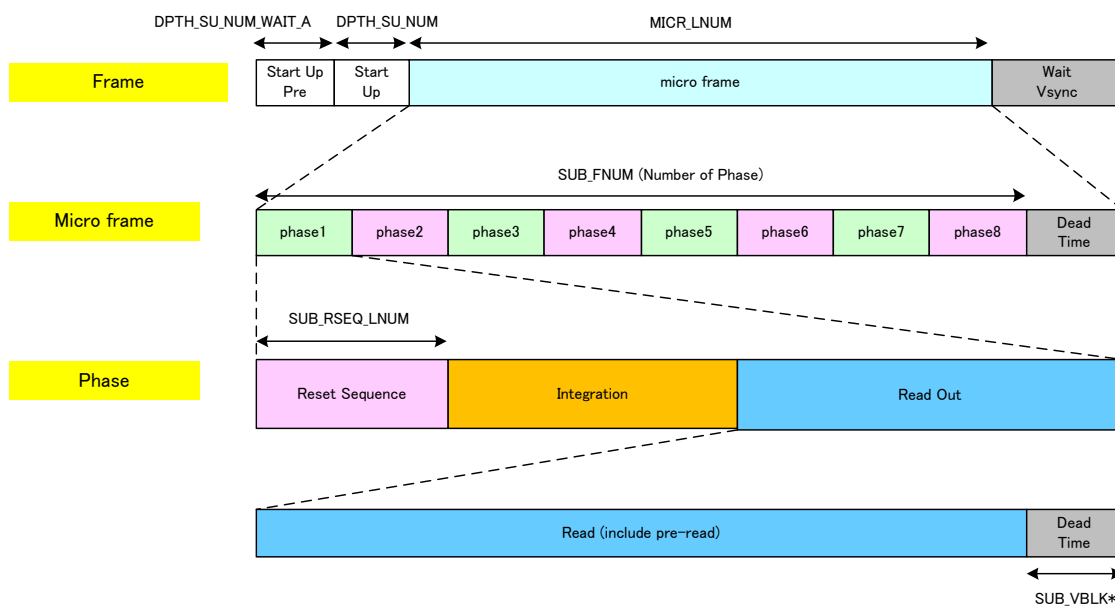
Figure 36 Frame Structure

The total time length of all phases is changed by the number of phases (SUB_FNUM setting).
(Case1) When MICR_LNUM is longer than the total time of all phases, the dead time is inserted at the end of the last frame.
(Case2) When MICR_LNUM is shorter than the total time of all phases, the state transition for next frame is performed after the last phase output is completed.
In the case of setting the dead time to be in the last of Frame only, Set MICR_LNUM register to longer value than the total time of all phases period.
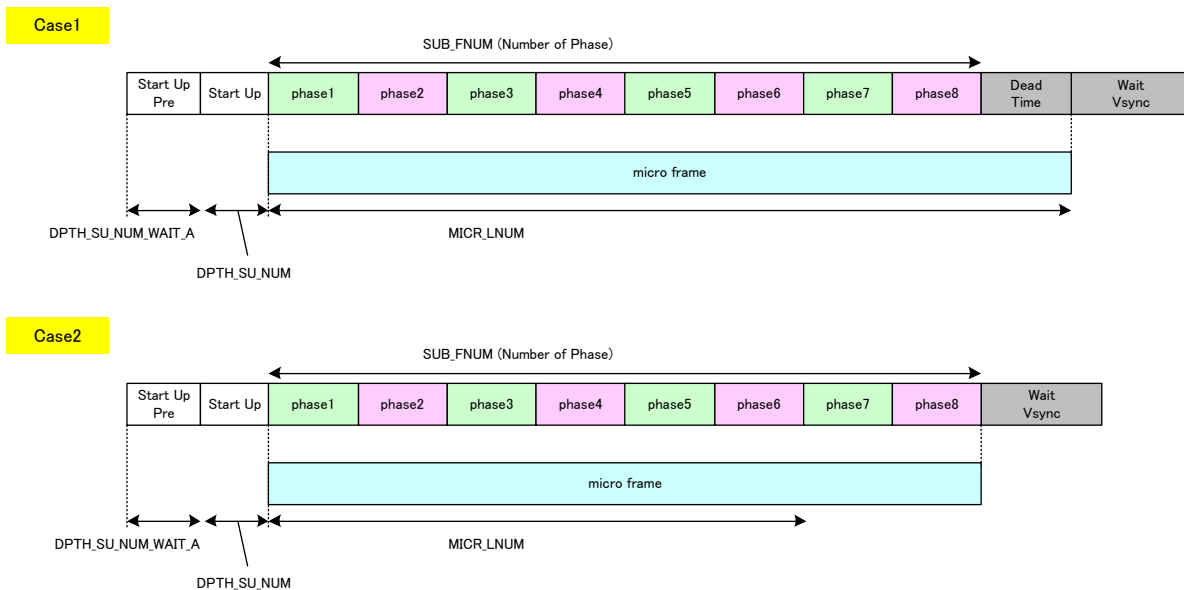
Figure 37 Use Case of MICR_LNUM Setting

Table 14 Register Table for Frame Setting

Address	Bit	Register Name	Description
0x2108	[7:0]	MICR_LNUM[31:24]	Length of micro frame = MICR_LNUM * HMAX [clk@120MHz]
0x2109	[7:0]	MICR_LNUM[23:16]	
0x210a	[7:0]	MICR_LNUM[15:8]	
0x210b	[7:0]	MICR_LNUM[7:0]	
0x21d4	[7:0]	DPTH_SU_NUM_WAIT_A[15:8]	start-up pre time of each frame
0x21d5	[7:0]	DPTH_SU_NUM_WAIT_A[7:0]	= DPTH_SU_NUM_WAIT_A * HMAX [clk@120MHz]
0x21e8	[3:0]	SUB_FNUM	Number of phases 4'd1: Phase1 enable 4'd2: Phase1 to 2 enable 4'd3: Phase1 to 3 enable 4'd4: Phase1 to 4 enable 4'd5: Phase1 to 5 enable 4'd6: Phase1 to 6 enable 4'd7: Phase1 to 7 enable 4'd8: Phase1 to 8 enable (4'd0 and 4'd9 to 4'd15 are prohibited)
0x4010	[7:0]	DPTH_SU_NUM	Start Up period = DPTH_SU_NUM * HMAX [clk@120MHz]
0x4015	[4:0]	SUB_RSEQ_LNUM[12:8]	Line count of Reset Sequence = SUB_RSEQ_LNUM * HMAX [clk@120MHz] (13'd0 is prohibited)
0x4016	[7:0]	SUB_RSEQ_LNUM[7:0]	
0x21c8	[7:0]	SUB_VBLK0	V-Blanking for phase1 (= SUB_VBLK0 * HMAX [clk@120MHz]) (4'd0 to 4'd4 are prohibited)

Address	Bit	Register Name	Description
0x21c9	[7:0]	SUB_VBLK1	V-Blanking for phase2 (= SUB_VBLK1 * HMAX[clk@120MHz]) (4'd0-4'd4 are prohibited)
0x21ca	[7:0]	SUB_VBLK2	V-Blanking for phase3 (= SUB_VBLK2 * HMAX[clk@120MHz]) (4'd0-4'd4 are prohibited)
0x21cb	[7:0]	SUB_VBLK3	V-Blanking for phase4 (= SUB_VBLK3 * HMAX[clk@120MHz]) (4'd0-4'd4 are prohibited)
0x21cc	[7:0]	SUB_VBLK4	V-Blanking for phase5 (= SUB_VBLK4 * HMAX[clk@120MHz]) (4'd0-4'd4 are prohibited)
0x21cd	[7:0]	SUB_VBLK5	V-Blanking for phase6 (= SUB_VBLK5 * HMAX[clk@120MHz]) (4'd0-4'd4 are prohibited)
0x21ce	[7:0]	SUB_VBLK6	V-Blanking for phase7 (= SUB_VBLK6 * HMAX[clk@120MHz]) (4'd0-4'd4 are prohibited)
0x21cf	[7:0]	SUB_VBLK7	V-Blanking for phase8 (= SUB_VBLK7 * HMAX[clk@120MHz]) (4'd0-4'd4 are prohibited)

The frame rate of the output image from this sensor can be calculated by the formula below.

Table 15 Formula of Frame Timing

No.	Item	Unit	Calculation
[1]	ResetSeq	[H]	= SUB_RSEQ_LNUM
[2]	Integration length	[H]	= roundup ((EXAREA_INTG00 to 07 + 75) / HMAX) + 1
[3]	ReadOut	[H]	= (Y_ADD_END - Y_ADD_STA + 1) + 7 + SUB_VBLK*
[4]	Phase length	[us]	= ([1] + [2] + [3]) * HMAX / 120
[5]	Frame length	[us]	= (DPTH_SU_NUM_WAIT_A + DPTH_SU_NUM + MICR_LNUM) * HMAX / 120
[6]	Frame rate / second	[fps]	= 1 / ([5] * 1e-6)

6-6-2   Angle Differences

The angle difference setting between the illumination pulse and the exposure signal of each phase can be set by the sensor register individually in 45° steps.
GDA means the sensor internal signal of A pixel exposure.
GDB means the sensor internal signal of B pixel exposure signal.
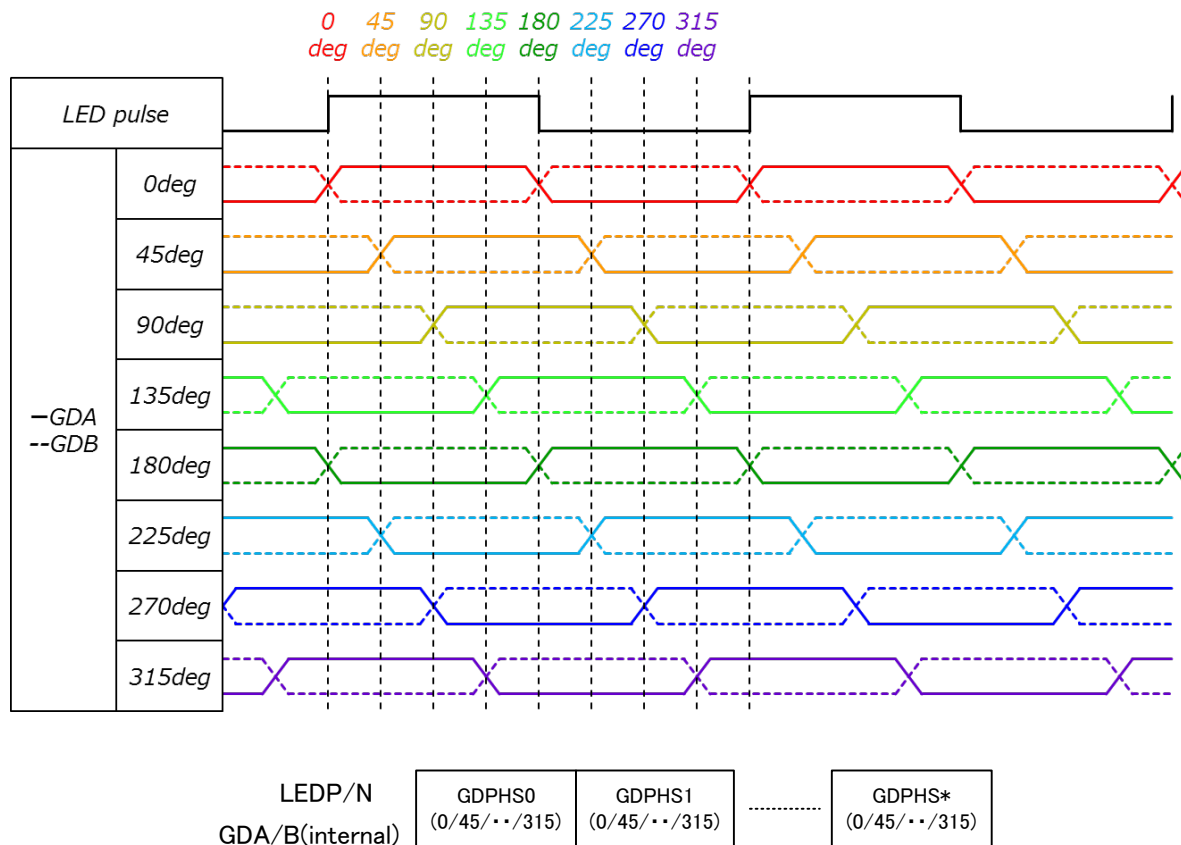
Figure 38 Angle Difference between Illumination and Mix

Table 16 Register Table for Angle Difference

Address	Bit	Register Name	Description
0x21b4	[6:4]	GDPHS1	360 [deg] x GDPHS / 8 for phase2
0x21b4	[2:0]	GDPHS0	360 [deg] x GDPHS / 8 for phase1
0x21b5	[6:4]	GDPHS3	360 [deg] x GDPHS / 8 for phase4
0x21b5	[2:0]	GDPHS2	360 [deg] x GDPHS / 8 for phase3
0x21b6	[6:4]	GDPHS5	360 [deg] x GDPHS / 8 for phase6
0x21b6	[2:0]	GDPHS4	360 [deg] x GDPHS / 8 for phase5
0x21b7	[6:4]	GDPHS7	360 [deg] x GDPHS / 8 for phase8
0x21b7	[2:0]	GDPHS6	360 [deg] x GDPHS / 8 for phase7

6-6-3   Integration Time Duration

The integration time setting for each phase can be set individually. A cycle unit of the integration time is approx. 8.3ns@120MHz/1clk. The integration time can be set by the register shown as the table below.
The maximum number of one exposure time setting is 1 msec, and the minimum setting is 250 nsec.
Integration time should be set by units of HMAX.

$$250ns < \frac{EXAREA\_INTG\_0n[31:0] + (SUB\_RSEQ\_LNUM \times HMAX - \alpha)}{120MHz} < 1ms \; (*\, n = 0\sim7)$$

The ratio of Integration time to Frame length must be lower than 40%.

$$\frac{Total\ Integration\ time}{Frame\ length} = \frac{(SUB\_RSEQ\_LNUM \times HMAX - \alpha) \times n + \sum_{n=0}^{7}(EXAREA\_INTG\_0n[31:0] \times INTG\_REP\_0n[7:0])}{(DPTH\_SU\_NUM\_WAIT\_A[15:0] + DPTH\_SU\_NUM[7:0] + MICR\_LNUM[31:0]) \times HMAX[13:0]} < 0.4$$

- No Binning A&B output mode@MIPI 960Mbps/lane x 4lane (HMAX = 1300clk/120MHz)：α =6500clk
- Other@MIPI 960Mbps/lane x 4lane (HMAX = 694clk/120MHz)：α =6246clk
- INTG_REP_0n[7:0] = 1 fix

Table 17 Register Table for Integration Time

Address	Bit	Register Name	Description
0x2120	[7:0]	EXAREA_INTG_00[31:0]	Integration time (clk@120MHz) for phase1
0x2121	[7:0]		
0x2122	[7:0]		
0x2123	[7:0]		
0x2124	[7:0]	EXAREA_INTG_01[31:0]	Integration time (clk@120MHz) for phase2
0x2125	[7:0]		
0x2126	[7:0]		
0x2127	[7:0]		
0x2128	[7:0]	EXAREA_INTG_02[31:0]	Integration time (clk@120MHz) for phase3
0x2129	[7:0]		
0x212a	[7:0]		
0x212b	[7:0]		
0x212c	[7:0]	EXAREA_INTG_03[31:0]	Integration time (clk@120MHz) for phase4
0x212d	[7:0]		
0x212e	[7:0]		
0x212f	[7:0]		
0x2130	[7:0]	EXAREA_INTG_04[31:0]	Integration time (clk@120MHz) for phase5
0x2131	[7:0]		
0x2132	[7:0]		
0x2133	[7:0]		
0x2134	[7:0]	EXAREA_INTG_05[31:0]	Integration time (clk@120MHz) for phase6
0x2135	[7:0]		
0x2136	[7:0]		
0x2137	[7:0]		

Address	Bit	Register Name	Description
0x2138	[7:0]	EXAREA_INTG_06[31:0]	Integration time (clk@120MHz) for phase7
0x2139	[7:0]		
0x213a	[7:0]		
0x213b	[7:0]		
0x213c	[7:0]	EXAREA_INTG_07[31:0]	Integration time (clk@120MHz) for phase8
0x213d	[7:0]		
0x213e	[7:0]		
0x213f	[7:0]		

Table 18 Restrictions of EXAREA_INTG_0* Register Setting Values

FMOD	EXAREA_INTG_0* [dec]
100	30 or HMAX[d] * N
99	30 or HMAX[d] * N
…	
12	30 or HMAX[d] * N
11	33 or HMAX[d] * N
10	36 or HMAX[d] * N
9	40 or HMAX[d] * N
8	45 or HMAX[d] * N
7	52 or HMAX[d] * N
6	60 or HMAX[d] * N
5	72 or HMAX[d] * N
4	90 or HMAX[d] * N

6-6-4   Static High/Low Function for Illumination Signal (Laser) and MIX Signal (GDA/GDB)

The register settings of GDA/GDB: Exposure signals (MIX) and Illumination signal for Laser (MOD) are shown below.
Set the register (GD*CNSTH*) to 2'b10 in case that GDA/GDB is set to fixed low.
Set GD*CNSTH* to 2'b11 in case that GDA/GDB is set to fixed High, and then GDA/GDB is fixed to High in the integration period only.
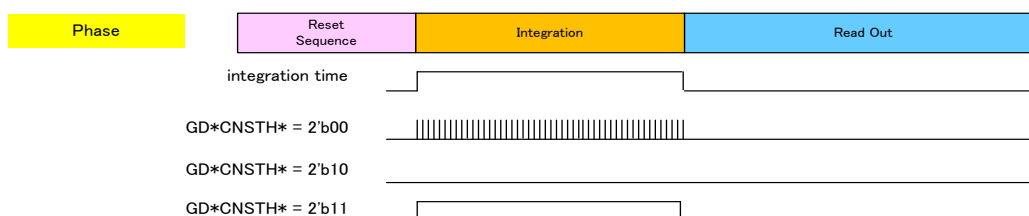
Figure 39 Figure Static Function

Table 19 Register Table for Static Function

Address	Bit	Register Name	Description
0x21a8	[7:6]	GDACNSTH3	Static Low/High setting (GDA) for phase4 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through GDA enable signal (for Test)
0x21a8	[5:4]	GDACNSTH2	Static Low/High setting (GDA) for phase3 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through GDA enable signal (for Test)
0x21a8	[3:2]	GDACNSTH1	Static Low/High setting (GDA) for phase2 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through GDA enable signal (for Test)
0x21a8	[1:0]	GDACNSTH0	Static Low/High setting (GDA) for phase1 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through GDA enable signal (for Test)
0x21a9	[7:6]	GDACNSTH7	Static Low/High setting (GDA) for phase8 0 : Normal (pulse) 2 : Low fix (for Test) 3 : through GDA enable signal (for Test)
0x21a9	[5:4]	GDACNSTH6	Static Low/High setting (GDA) for phase7 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through GDA enable signal (for Test)
0x21a9	[3:2]	GDACNSTH5	Static Low/High setting (GDA) for phase6 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through GDA enable signal (for Test)
0x21a9	[1:0]	GDACNSTH4	Static Low/High setting (GDA) for phase5 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through GDA enable signal (for Test)
0x21ac	[7:6]	GDBCNSTH3	Static Low/High setting (GDB) for phase4 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through GDB enable signal (for Test)
0x21ac	[5:4]	GDBCNSTH2	Static Low/High setting (GDB) for phase3 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through GDB enable signal (for Test)
0x21ac	[3:2]	GDBCNSTH1	Static Low/High setting (GDB) for phase2 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through GDB enable signal (for Test)
0x21ac	[1:0]	GDBCNSTH0	Static Low/High setting (GDB) for phase1 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through GDB enable signal (for Test)
0x21ad	[7:6]	GDBCNSTH7	Static Low/High setting (GDB) for phase8 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through GDB enable signal (for Test)

Address	Bit	Register Name	Description
0x21ad	[5:4]	GDBCNSTH6	Static Low/High setting (GDB) for phase7 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through GDB enable signal (for Test)
0x21ad	[3:2]	GDBCNSTH5	Static Low/High setting (GDB) for phase6 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through GDB enable signal (for Test)
0x21ad	[1:0]	GDBCNSTH4	Static Low/High setting (GDB) for phase5 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through GDB enable signal (for Test)
0x21b0	[7:6]	GDLSRCNSTH3	Static Low/High setting (laser) for phase4 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through illumination signal (for Test)
0x21b0	[5:4]	GDLSRCNSTH2	Static Low/High setting (laser) for phase3 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through illumination signal (for Test)
0x21b0	[3:2]	GDLSRCNSTH1	Static Low/High setting (laser) for phase2 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through illumination signal (for Test)
0x21b0	[1:0]	GDLSRCNSTH0	Static Low/High setting (laser) for phase1 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through illumination signal (for Test)
0x21b1	[7:6]	GDLSRCNSTH7	Static Low/High setting (laser) for phase8 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through illumination signal (for Test)
0x21b1	[5:4]	GDLSRCNSTH6	Static Low/High setting (laser) for phase7 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through illumination signal (for Test)
0x21b1	[3:2]	GDLSRCNSTH5	Static Low/High setting (laser) for phase6 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through illumination signal (for Test)
0x21b1	[1:0]	GDLSRCNSTH4	Static Low/High setting (laser) for phase5 0 : Normal (pulse) 2 : Low fix (for Test) 3 : Through illumination signal (for Test)

6-6-5   Modulation frequency

The modulation frequency (FMOD) for the frame can be set from 4 MHz to 100 MHz in 1 MHz steps. The modulation frequency can be changed in the streaming period only. The setting registers are shown in the table below. The changing of External clock frequency is permitted in Chip Standby or Software Standby period in front of Power-On sequence, but the changing in the streaming period is prohibited.

Table 20 Register Table for Modulation Frequency Setting

Address	Bit	Register Name	Description
0x1006	[7:0]	EXCK_FREQ[15:8]	External clock frequency [MHz]
0x1007	[7:0]	EXCK_FREQ[7:0]	(= INCK frequency) *Please make sure to send this register at first after Power-On.
0x1042	[3:0]	PL_RC_VT	
0x1046	[3:0]	PL_RC_OP	
0x1048	[2:0]	PL_FC_MX[10:8]	
0x1049	[7:0]	PL_FC_MX[7:0]	PLL settings
0x104a	[3:0]	PL_RC_MX	
0x104b	[1:0]	PL_RES_MX	
0x21be	[3:0]	DIVSELPRE	MIX divider settings
0x21bf	[1:0]	DIVSEL	

Refer to the additional material (FMOD_Setting) for the actual setting values for each frequency.

To change the modulation frequency in the streaming, perform the following sequence.
1. Send the register: GRP_PARAM_HOLD = 1
2. Send the necessary register shown above (Changing the INCK frequency is prohibited)
3. Send the register: GRP_PARAM_HOLD = 0 (FMOD is changed from the next frame)

The INCK frequency can be chosen from 8 / 16 / 32 MHz. The settings of each frequency are shown below. The External clock frequency (INCK) can be changed in Chip Standby period only, but changing the frequency in Streaming and SW-STB is prohibited.

Table 21 Setting Variation

Register Name	INCK		
	8 MHz	16 MHz	32 MHz
EXCK_FREQ	16'h0800	16'h1000	16'h2000
PL_RC_VT	4'h1	4'h2	4'h4
PL_RC_OP	4'h1	4'h2	4'h4
PL_RC_MX	4'h1	4'h2	4'h4

6-6-6　Master, Slave

The start-up operation of ToF process has 2 patterns: Start-up from external (Slave operation) and Start-up from Internal (Master operation). Default setting is Slave mode. The mode changing of Master/Slave can be set in Chip Standby/Software Standby period only. The mode changing of Master/Slave is prohibited in Streaming status.
The figure below shows an overview of Slave mode operation. Internal status is changed from SW-Standby to Wake Up when MODE_SEL register is set to 1. External XVS is accepted after WakeUp. XVS pulses which are input before Wake-up are ignored. The sensor can accept XVS pulse input in Wait Vsync period only. ToF operation is started after the external XVS accepting. Next XVS is ignored until the 1 Frame output is completed.
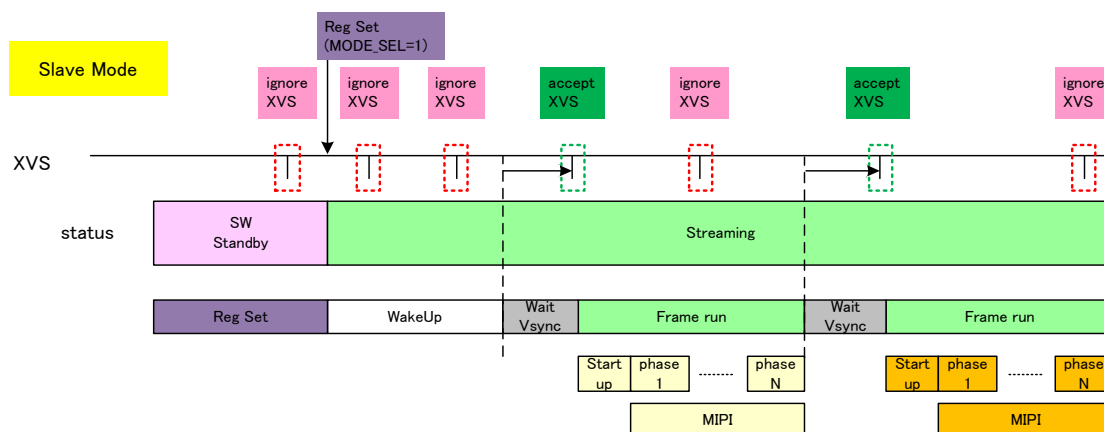
Figure 40 Sequence of Slave Mode

	Min	Max
Input XVS pulse width [clock@120MHz]	8	—
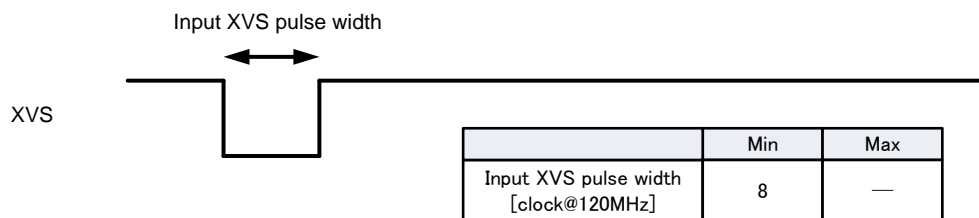
Figure 41 Input XVS Pulse Spec for Slave Mode

The figure below shows an overview of Master mode. After the register sending for Master mode in SW-Standby period, the state is shift to Streaming state when MODE_SEL = 1 is sent. Frame operation is started automatically after WakeUp sequence.
In the case of Repeat Off mode, the output is stopped after 1 Frame completed unless next XVS is input.
In the case of Repeat On mode, next frame starting automatically.
User can select the mode by changing the sensor register value.
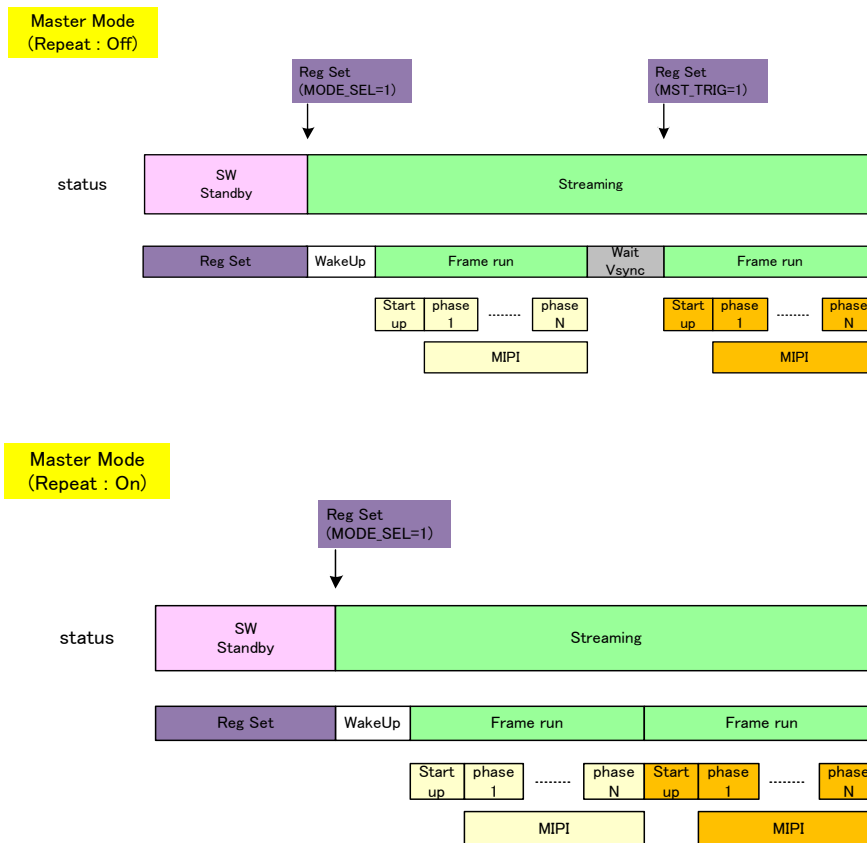
Figure 42 Sequence of Master Mode

Table 22 Register table for Master/Slave Setting

Address	Bit	Register Name	Description
0x2020	[0]	TMASTER	0 : Slave Mode 1 : Master Mode
0x2100	[3]	DPTHMAP_REP	Repeat Setting in Master Mode 0 : Stop after 1 frame 1 : Auto restart after frame (1'b1 is prohibited in Slave Mode)
0x2100	[0]	MST_TRIG	Restart trigger in Master mode 1 : Restart (it's only available after previous frame is finished)

6-6-7   VSYNC Output Control

This sensor can output internal V sync via monitor terminal as XVS. V sync is the timing of the depth map unit. See the following table for register settings.

Table 23 Monitor Terminal Setting

	Address	Bit	Register Name	Setting Value
I2C register	0x2f05	[2:0]	TESTSEL1	XVS pin monitor setting 1: XVS output Other: none
	0x2f06	[3:0]	TESTMNT1[11:8]	XVS pin monitor setting [11:8] = 9h [7:0] = 7Ah
	0x2f07	[7:0]	TESTMNT1[7:0]	

6-7　Binning

Binning mode is available for Full, 2x2, 4x4 and 8x8 selections. The Binning is executed each Tap A and Tap B. Binning mode is decided by BINNING_MODE register.

| Full resolution | 2x2binning | 4x4binning | 8x8binning |
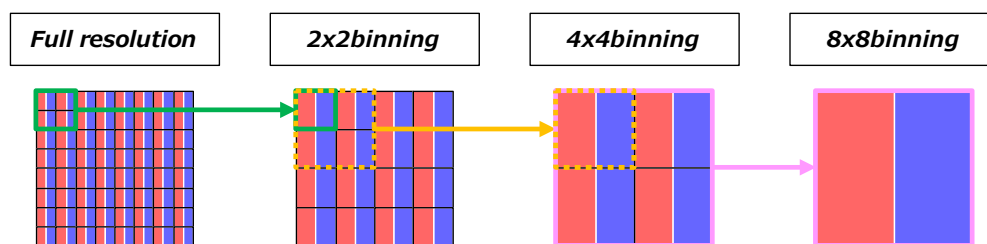
Figure 43 Binning

Table 24 Register Table for Binning

Address	Bit	Register Name	Description
0x14a5	[1:0]	BINNING_MODE	Binning Mode 0 : 1x1 (full) 1 : 2x2 2 : 4x4 3 : 8x8

6-8　Statistics

IMX556 can gather the statistic information internally.
　　Count of pixel values < Threshold (variable low threshold is set through I2C)
　　Count of pixel values > Threshold (variable high threshold is set through I2C)
The statistic information is gathered from each phase and sent out as meta-data in Embedded data. It can be read through I2C also.
If the count of pixel values is < low_threshold or > high_threshold, the pixel data can also output with error information for each pixel.

Table 25 Register Table for Statistics

Address	Bit	Register Name	Description
0x1433	[0]	RNGCHKEN	0 : No check high/low threshold of pixel values 1 : Check high/low threshold of pixel values
0x1434	[2:0]	LOWTHR0[10:8]	Low threshold of pixel values (phase1)
0x1435	[7:0]	LOWTHR0[7:0]	
0x1436	[2:0]	LOWTHR1[10:8]	Low threshold of pixel values (phase2)
0x1437	[7:0]	LOWTHR1[7:0]	
0x1438	[2:0]	LOWTHR2[10:8]	Low threshold of pixel values (phase3)
0x1439	[7:0]	LOWTHR2[7:0]	
0x143a	[2:0]	LOWTHR3[10:8]	Low threshold of pixel values (phase4)
0x143b	[7:0]	LOWTHR3[7:0]	
0x143c	[2:0]	LOWTHR4[10:8]	Low threshold of pixel values (phase5)
0x143d	[7:0]	LOWTHR4[7:0]	
0x143e	[2:0]	LOWTHR5[10:8]	Low threshold of pixel values (phase6)
0x143f	[7:0]	LOWTHR5[7:0]	
0x1440	[2:0]	LOWTHR6[10:8]	Low threshold of pixel values (phase7)
0x1441	[7:0]	LOWTHR6[7:0]	
0x1442	[2:0]	LOWTHR7[10:8]	Low threshold of pixel values (phase8)
0x1443	[7:0]	LOWTHR7[7:0]	

Address	Bit	Register Name	Description
0x1448	[2:0]	HIGHTHR0[10:8]	High threshold of pixel values (phase1)
0x1449	[7:0]	HIGHTHR0[7:0]	
0x144a	[2:0]	HIGHTHR1[10:8]	High threshold of pixel values (phase2)
0x144b	[7:0]	HIGHTHR1[7:0]	
0x144c	[2:0]	HIGHTHR2[10:8]	High threshold of pixel values (phase3)
0x144d	[7:0]	HIGHTHR2[7:0]	
0x144e	[2:0]	HIGHTHR3[10:8]	High threshold of pixel values (phase4)
0x144f	[7:0]	HIGHTHR3[7:0]	
0x1450	[2:0]	HIGHTHR4[10:8]	High threshold of pixel values (phase5)
0x1451	[7:0]	HIGHTHR4[7:0]	
0x1452	[2:0]	HIGHTHR5[10:8]	High threshold of pixel values (phase6)
0x1453	[7:0]	HIGHTHR5[7:0]	
0x1454	[2:0]	HIGHTHR6[10:8]	High threshold of pixel values (phase7)
0x1455	[7:0]	HIGHTHR6[7:0]	
0x1456	[2:0]	HIGHTHR7[10:8]	High threshold of pixel values (phase8)
0x1457	[7:0]	HIGHTHR7[7:0]	
0x145d	[3:0]	ERRCOUNTL0[19:16]	Count of pixel values < low_threshold (LOWTHR*) for phase1
0x145e	[7:0]	ERRCOUNTL0[15:8]	
0x145f	[7:0]	ERRCOUNTL0[7:0]	
0x1461	[3:0]	ERRCOUNTL1[19:16]	Count of pixel values < low_threshold (LOWTHR*) for phase2
0x1462	[7:0]	ERRCOUNTL1[15:8]	
0x1463	[7:0]	ERRCOUNTL1[7:0]	
0x1465	[3:0]	ERRCOUNTL2[19:16]	Count of pixel values < low_threshold (LOWTHR*) for phase3
0x1466	[7:0]	ERRCOUNTL2[15:8]	
0x1467	[7:0]	ERRCOUNTL2[7:0]	
0x1469	[3:0]	ERRCOUNTL3[19:16]	Count of pixel values < low_threshold (LOWTHR*) for phase4
0x146a	[7:0]	ERRCOUNTL3[15:8]	
0x146b	[7:0]	ERRCOUNTL3[7:0]	
0x146d	[3:0]	ERRCOUNTL4[19:16]	Count of pixel values < low_threshold (LOWTHR*) for phase5
0x146e	[7:0]	ERRCOUNTL4[15:8]	
0x146f	[7:0]	ERRCOUNTL4[7:0]	
0x1471	[3:0]	ERRCOUNTL5[19:16]	Count of pixel values < low_threshold (LOWTHR*) for phase6
0x1472	[7:0]	ERRCOUNTL5[15:8]	
0x1473	[7:0]	ERRCOUNTL5[7:0]	
0x1475	[3:0]	ERRCOUNTL6[19:16]	Count of pixel values < low_threshold (LOWTHR*) for phase7
0x1476	[7:0]	ERRCOUNTL6[15:8]	
0x1477	[7:0]	ERRCOUNTL6[7:0]	
0x1479	[3:0]	ERRCOUNTL7[19:16]	Count of pixel values < low_threshold (LOWTHR*) for phase8
0x147a	[7:0]	ERRCOUNTL7[15:8]	
0x147b	[7:0]	ERRCOUNTL7[7:0]	
0x1481	[3:0]	ERRCOUNTH0[19:16]	Count of pixel values > high_threshold (HIGHTHR*) for phase1
0x1482	[7:0]	ERRCOUNTH0[15:8]	
0x1483	[7:0]	ERRCOUNTH0[7:0]	
0x1485	[3:0]	ERRCOUNTH1[19:16]	Count of pixel values > high_threshold (HIGHTHR*) for phase2
0x1486	[7:0]	ERRCOUNTH1[15:8]	
0x1487	[7:0]	ERRCOUNTH1[7:0]	
0x1489	[3:0]	ERRCOUNTH2[19:16]	Count of pixel values > high_threshold (HIGHTHR*) for phase3
0x148a	[7:0]	ERRCOUNTH2[15:8]	
0x148b	[7:0]	ERRCOUNTH2[7:0]	
0x148d	[3:0]	ERRCOUNTH3[19:16]	Count of pixel values > high_threshold (HIGHTHR*) for phase4
0x148e	[7:0]	ERRCOUNTH3[15:8]	
0x148f	[7:0]	ERRCOUNTH3[7:0]	

Address	Bit	Register Name	Description
0x1491	[3:0]	ERRCOUNTH4[19:16]	Count of pixel values > high_threshold (HIGHTHR*) for phase5
0x1492	[7:0]	ERRCOUNTH4[15:8]	
0x1493	[7:0]	ERRCOUNTH4[7:0]	
0x1495	[3:0]	ERRCOUNTH5[19:16]	Count of pixel values > high_threshold (HIGHTHR*) for phase6
0x1496	[7:0]	ERRCOUNTH5[15:8]	
0x1497	[7:0]	ERRCOUNTH5[7:0]	
0x1499	[3:0]	ERRCOUNTH6[19:16]	Count of pixel values > high_threshold (HIGHTHR*) for phase7
0x149a	[7:0]	ERRCOUNTH6[15:8]	
0x149b	[7:0]	ERRCOUNTH6[7:0]	
0x149d	[3:0]	ERRCOUNTH7[19:16]	Count of pixel values > high_threshold (HIGHTHR*) for phase8
0x149e	[7:0]	ERRCOUNTH7[15:8]	
0x149f	[7:0]	ERRCOUNTH7[7:0]	

6-9 Readout

6-9-1 Readout Mode

The image of each readout mode shows below. There is Tap A/B in one pixel. The number of horizontal output data for A&B mode is double of other modes.
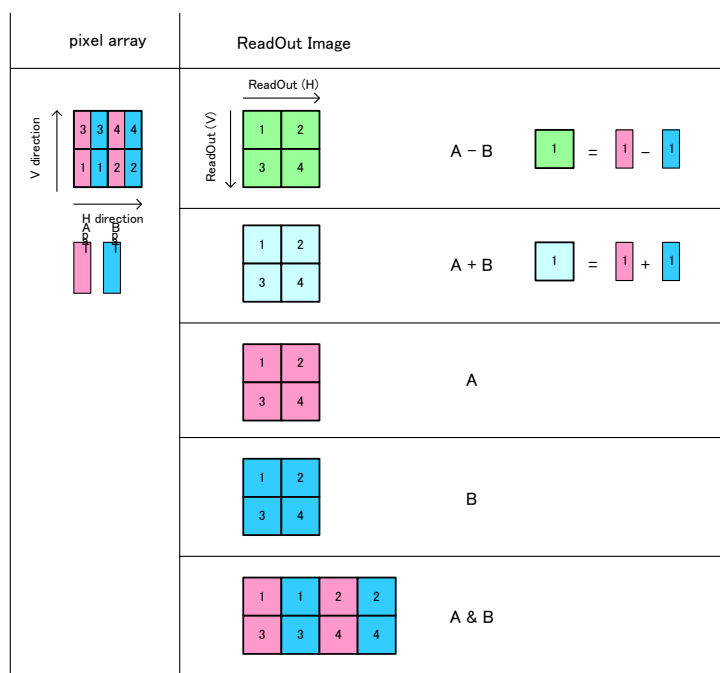

Figure 44 Readout Image depend on Readout Mode

The register setting list for each readout mode (A / B selection, Binning selection, MIPI Lane number selection) is shown below.

Table 26 Readout Mode

Mode	Binning	MIPI Lane	DUTOF _MODE	BINNING _MODE	CSI_LANE _MODE	REQUESTED _LINK_BIT _RATE_MBPS	HMAX	SUB_RSEQ _LNUM	DPTH_SU _NUM
A-B	1x1	4 Lanes	0	0	3	32'h0f000000	14'd694	13'd9	8'd95
	2x2			1			14'd694	13'd9	8'd95
	4x4			2			14'd694	13'd9	8'd95
	8x8			3			14'd694	13'd9	8'd95
A+B	1x1		1	0			14'd694	13'd9	8'd95
	2x2			1			14'd694	13'd9	8'd95
	4x4			2			14'd694	13'd9	8'd95
	8x8			3			14'd694	13'd9	8'd95
A	1x1		2	0			14'd694	13'd9	8'd95
	2x2			1			14'd694	13'd9	8'd95
	4x4			2			14'd694	13'd9	8'd95
	8x8			3			14'd694	13'd9	8'd95
B	1x1		3	0			14'd694	13'd9	8'd95
	2x2			1			14'd694	13'd9	8'd95
	4x4			2			14'd694	13'd9	8'd95
	8x8			3			14'd694	13'd9	8'd95
A&B	1x1		4	0			14'd1388	13'd5	8'd52
	2x2			1			14'd694	13'd9	8'd95
	4x4			2			14'd694	13'd9	8'd95
	8x8			3			14'd694	13'd9	8'd95
A-B	1x1	2 Lanes	0	0	1	32'h07800000	14'd1388	13'd5	8'd52
	2x2			1			14'd1388	13'd5	8'd52
	4x4			2			14'd1388	13'd5	8'd52
	8x8			3			14'd1388	13'd5	8'd52
A+B	1x1		1	0			14'd1388	13'd5	8'd52
	2x2			1			14'd1388	13'd5	8'd52
	4x4			2			14'd1388	13'd5	8'd52
	8x8			3			14'd1388	13'd5	8'd52
A	1x1		2	0			14'd1388	13'd5	8'd52
	2x2			1			14'd1388	13'd5	8'd52
	4x4			2			14'd1388	13'd5	8'd52
	8x8			3			14'd1388	13'd5	8'd52
B	1x1		3	0			14'd1388	13'd5	8'd52
	2x2			1			14'd1388	13'd5	8'd52
	4x4			2			14'd1388	13'd5	8'd52
	8x8			3			14'd1388	13'd5	8'd52
A&B	1x1		4	0			14'd2776	13'd3	8'd30
	2x2			1			14'd1388	13'd5	8'd52
	4x4			2			14'd1388	13'd5	8'd52
	8x8			3			14'd1388	13'd5	8'd52

Table 27 Register Table for Readout Mode

Address	Bit	Register Name	Description
0x0800	[5:0]	HMAX[13:8]	1H duration (clk)
0x0801	[7:0]	HMAX[7:0]	
0x0828	[2:0]	DUTOF_MODE	0: Tap-A - Tap-B 1: Tap-A + Tap-B 2: Raw Tap-A only 3: Raw Tap-B only 4: Raw Tap-A and Tap-B
0x100c	[7:0]	REQUESTED_LINK_BIT_RATE_MBPS[31:24]	Output Data Rate [Mbps] Bit[31:16] integer Bit[15:0] decimal * initial values = 960 [Mbps/Lane] x 4 [Lane] = 16'h0f00 (integer)
0x100d	[7:0]	REQUESTED_LINK_BIT_RATE_MBPS[23:16]	
0x100e	[7:0]	REQUESTED_LINK_BIT_RATE_MBPS[15:8]	
0x100f	[7:0]	REQUESTED_LINK_BIT_RATE_MBPS[7:0]	
0x1010	[1:0]	CSI_LANE_MODE	The Number of Lanes 0 : prohibited 1 : 2Lane 2 : prohibited 3 : 4Lane
0x14a5	[1:0]	BINNING_MODE	Binning Mode 0 : 1x1 (full) 1 : 2x2 2 : 4x4 3 : 8x8

Table 28 MIPI Transmitter

	Pin Name	2Lane	4Lane
MIPI transmitter	DCKP/DCKN	Clock lane	Clock lane
	DMO1P/DMO1N	Data lane 1	Data lane 1
	DMO2P/DMO2N	Data lane 2	Data lane 2
	DMO3P/DMO3N	Not used (LP only)	Data lane 3
	DMO4P/DMO4N	Not used (LP only)	Data lane 4

6-9-2   Mirror/Flip

The readout order of the pixel array can be reversed.
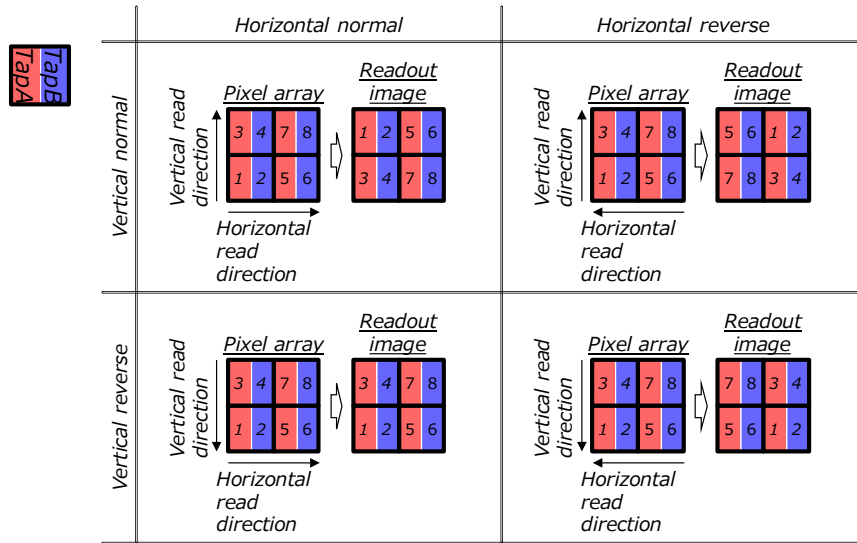
Figure 45 Mirror/Flip Output Image

Table 29 Register Table for Mirror/Flip

Address	Bit	Register Name	Description
0x080c	[0]	IMG_ORIENTATION_V	Image orientation for Vertical direction 0 : Normal 1 : Reverse
0x080d	[0]	IMG_ORIENTATION_H	Image orientation for Horizontal direction 0 : Normal 1 : Reverse

6-9-3 ROI Setting

ROI settings show below.

· The read pixel area is set by the registers of the horizontal start address, the horizontal width, the vertical start address and the vertical end address. Note that these settings are not the address after binning when using Binning mode. Set ROI registers to the value before binning.

· Horizontal setting is set by HCROP_STA (Horizontal start address) and HCROP_WID (Horizontal width) registers. Note that HCROP_SAT setting must be changed in the case that the horizontal reverse mode reads the same area as the horizontal normal mode.

· Vertical setting is set by Y_ADD_STA (Vertical start address) and Y_ADD_END (Vertical end address) registers. Note that the unit for Y_ADD_STA/END setting is 2 lines.

ROI (full, HV reverse)

ROI (full, HV normal)
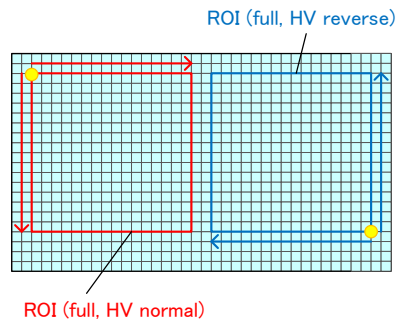
Note that
you have to change "HCROP_STA" in H reverse mode
if you want to read out the same region as H normal mode.
* above/below chart is in case of not changing
"HCROP_STA" in H reverse mode

ROI (HV normal)   ROI (HV reverse)

2x2 binning

1pixel (TapA/B)   1pixel (TapA/B)

4x4 binning

1pixel (TapA/B)   1pixel (TapA/B)

8x8 binning

1pixel (TapA/B)   1pixel (TapA/B)
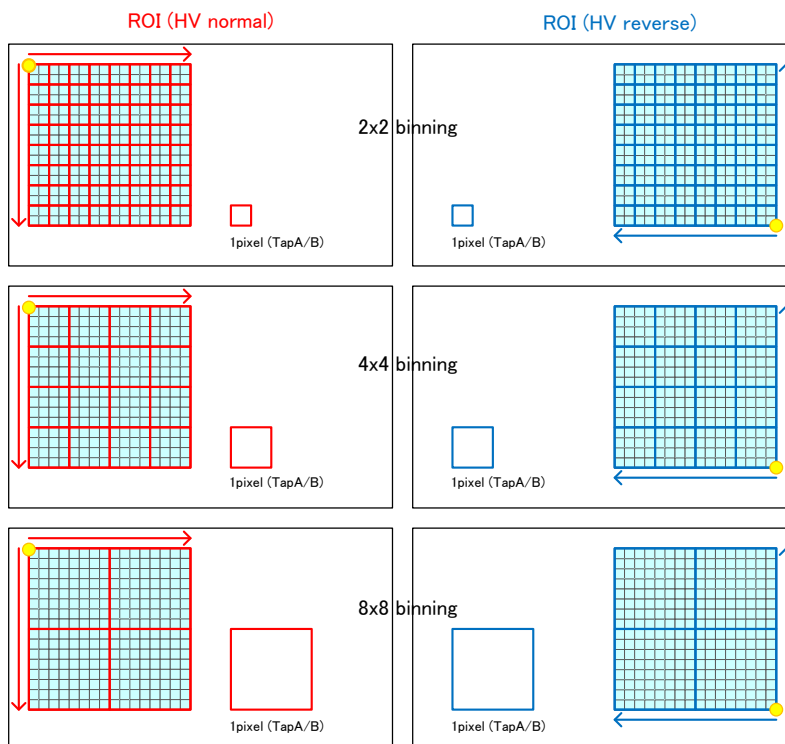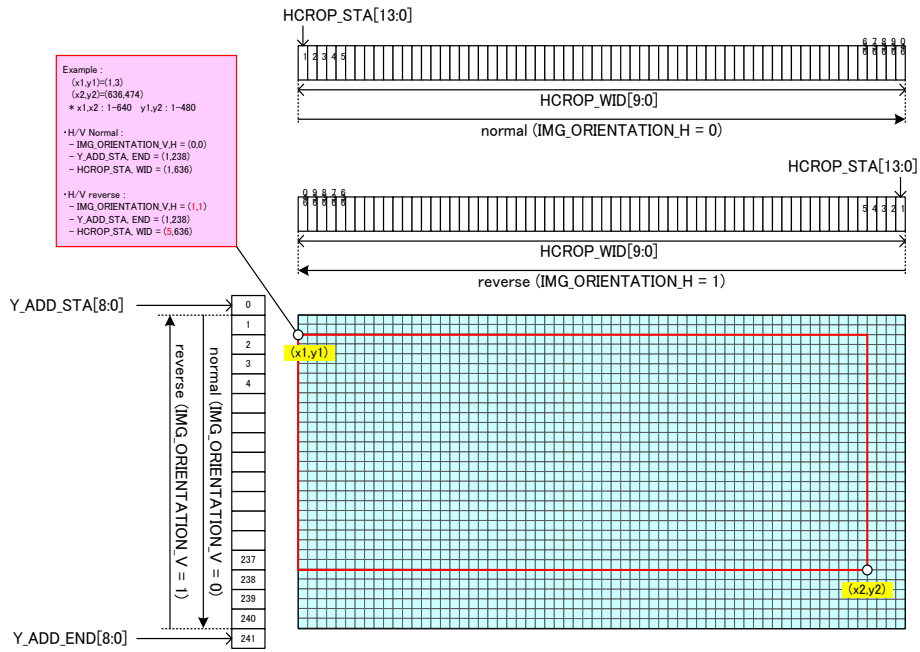
Figure 46 ROI Setting

Table 30 Register Table for ROI

Address	Bit	Register Name	Description
0x0804	[5:0]	HCROP_STA[13:8]	H start address (pix)
0x0805	[7:0]	HCROP_STA[7:0]	
0x0806	[1:0]	HCROP_WID[9:8]	H width (pix)
0x0807	[7:0]	HCROP_WID[7:0]	
0x0808	[0]	Y_ADD_STA[8]	V start address (2line)
0x0809	[7:0]	Y_ADD_STA[7:0]	
0x080a	[0]	Y_ADD_END[8]	V end address (2line)
0x080b	[7:0]	Y_ADD_END[7:0]	

6-9-4 ROI Setting Constraint

The start coordinate (x1,y1), the end coordinate (x2,y2) and H/V size setting registers for the readout region are shown below. The setting ranges and restrictions of x1 and x2 for each binning mode also are shown below. The setting value over the range is prohibited.

Table 31 Constraint of x1,x2

Binning	X position		X size	Register	
	x1	x2	x2 - x1 + 1	HCROP_STA	HCROP_WID
1x1	"1 to 633"	"8 to 640"	"8 to 640" and "multiples of 4"	"1 to 633"	" > = 8" and "multiples of 4"
2x2	"1 to 625"	"16 to 640"	"16 to 640" and "multiples of 8"	"1 to 625"	" > = 16" and "multiples of 8"
4x4	"1 to 609"	"32 to 640"	"32 to 640" and "multiples of 16"	"1 to 609"	" > = 32" and "multiples of 16"
8x8	"1 to 577"	"64 to 640"	"64 to 640" and "multiples of 32"	"1 to 577"	" > = 64" and "multiples of 32"

The table shown below is the formulas for HCROP_STA/WID setting values by using x1 and x2.

Table 32 Formula for HCROP_STA/WID

Register Name	IMG_ORIENTATION_H	
	0	1
HCROP_STA	(x1)	640 - (x2) + 1
HCROP_WID	(x2) − (x1) + 1	

The setting ranges and restrictions of y1 and y2 for each binning mode are shown below. The setting value over the range is prohibited.

Table 33 Constraint of y1,y2

Binning	Y position		Y size	Register
	y1	y2	y2 - y1 + 1	Y_ADD_END - Y_ADD_STA – 1
1x1	"1 to 479"	"2 to 480"	"2-480" and "multiples of 2"	">= 1"
2x2	"1 to 479"	"2 to 480"	"2-480" and "multiples of 2"	">= 1"
4x4	"1 to 477"	"4 to 480"	"4-480" and "multiples of 4"	">= 2" and "multiples of 2"
8x8	"1 to 473"	"8 to 480"	"8-480" and "multiples of 8"	">= 4" and "multiples of 4"

The table shown below is the formula of Y_ADD_STA/END setting value by using y1 and y2 address.

Table 34 Formula for Y_ADD_STA/END

Register Name	IMG_ORIENTATION_V	
	0	1
Y_ADD_STA	((y1) - 1) / 2	
Y_ADD_END	(y2) / 2 + 1	

6-10 Embedded Data

Embedded data list shows below. Meta-Data is output as 2 lines data after the pixel data output. Refer to "Output Interface" for the Meta-Data output location.

Table 35 Embedded Data

Line	Pixel	Data	Description
0	E000	8'h0A	Data Format Code (= 0x0A)
0	E058	DEPTH_MAP_ID	ID information (bit [7:0]) * DEPTH_MAP_ID is just a register updated every frame * we can find which id of register-configuration is set in each phase by this Data
0	E078	THRM_DT_DEG	Temperature
0	E127	8'h07	End of Data (= 0x07)
0	E128	8'h07	End of Data (= 0x07)
0	E129	8'h07	End of Data (= 0x07)
0	E130	8'h07	End of Data (= 0x07)
0	E131	8'h07	End of Data (= 0x07)
1	E050	RNGCHK_COUNT_LOW[19:16]	Count of pixel values < low_threshold for each phase
1	E052	RNGCHK_COUNT_LOW[15:8]	Count of pixel values < low_threshold for each phase
1	E054	RNGCHK_COUNT_LOW[7:0]	Count of pixel values < low_threshold for each phase
1	E058	RNGCHK_COUNT_HIGH[19:16]	Count of pixel values > high_threshold for each phase
1	E060	RNGCHK_COUNT_HIGH[15:8]	Count of pixel values > high_threshold for each phase
1	E062	RNGCHK_COUNT_HIGH[7:0]	Count of pixel values > high_threshold for each phase
1	E090	DEPTH_MAP_NUMBER	Depth map counter (bit [7:0]) = frame counter in case of IMX556 * free-run counter
1	E096	SUB_FRAME_NUMBER	phase counter (bit [3:0])
1	E127	8'h07	End of Data (= 0x07)
1	E128	8'h07	End of Data (= 0x07)
1	E129	8'h07	End of Data (= 0x07)
1	E130	8'h07	End of Data (= 0x07)
1	E131	8'h07	End of Data (= 0x07)

6-11 Output Interface

6-11-1 MIPI Overview

Pixel data is output according as the MIPI specification. MIPI specification overview is shown below.
  Number of Lane: 2 Lanes or 4 Lanes (the number of Lane can be changed at only Chip/SW-standby.)
  Number of Bit: 12 bits / pixel
Output data rate: 960 Mbps / Lane (the output data rate can be changed at only Chip/SW-standby.)

6-11-2 MIPI Pin

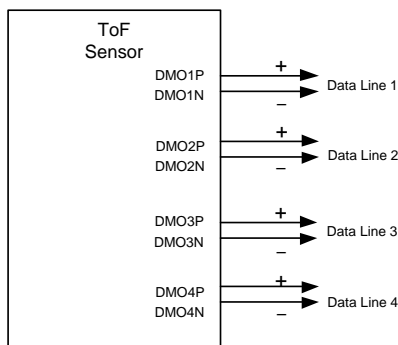Data and Clock from each lane show below.

Figure 47 MIPI Pin Assignment

6-11-3 MIPI RAW12

Assignment of 12 bits of output data shows below.
In case that the output data is over the threshold which is set by the register, MSB of the pixel data can have the error flag by setting RNGCHEN register to 1 and RNGCHK_OUTMODE register to 0. So, the pixel data is 11 bits length. Therefore, the bit accuracy is reduced.
When RNGCHKEN is set to 1 and RNGCHK_OUTMODE is set to 1, the pixel data is change to Error code.

Table 36 Error Mode Table

Mode	Without Error Info (RNGCHKEN = 0)	With Error Info (RNGCHKEN = 1)	
		Error Flag (RNGCHK_OUTMODE = 0)	Error Code (RNGCHK_OUTMODE = 1)
A − B	[11:0] = Pixel data (signed)	[11] = Error flag [10:0] = Pixel data (signed)	[11:0] = Pixel data (signed) Error code = 12'h800
A + B	[11:0] = Pixel data (unsigned)	[11] = Error flag [10:0] = Pixel data (unsigned)	[11:0] = Pixel data (unsigned) Error code = 12'hFFF
A	[11] = 0 [10:0] = Pixel data	[11] = Error flag [10:0] = Pixel data	[11] = 0 [10:0] = Pixel data
B	[11] = 0 [10:0] = Pixel data	[11] = Error flag [10:0] = Pixel data	[11] = 0 [10:0] = Pixel data
A & B	[11] = 0 [10:0] = Pixel data	[11] = Error flag [10:0] = Pixel data	[11] = 0 [10:0] = Pixel data

Table 37 Register Table for Error Info

Address	Bit	Register Name	Description
0x14bb	[0]	RNGCHK_OUTMODE	0 : Error flag 1 : Error code (A - B: 12'h800 A + B: 12'hfff)

6-11-4 MIPI Pixel Data Format

The figure below shows the image output format of each Lane for each Lane number.
P0, 1, 2 and 3 in the figure below correspond to one output pixel data.
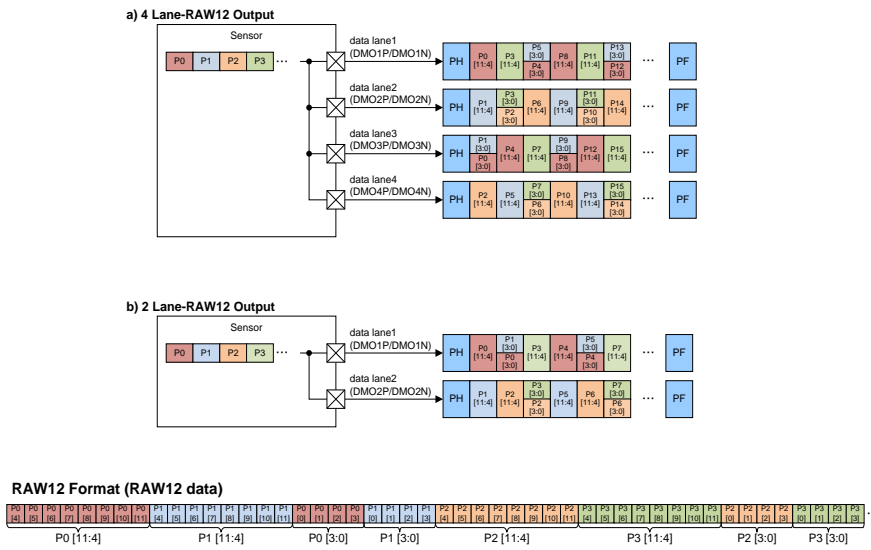

Figure 48 MIPI Pixel Data Format

6-11-5 MIPI Embedded Data Format

Embedded data is output on two lines after effective pixels.
The data in each line is composed of Tag, Data, dummy data shown as below.
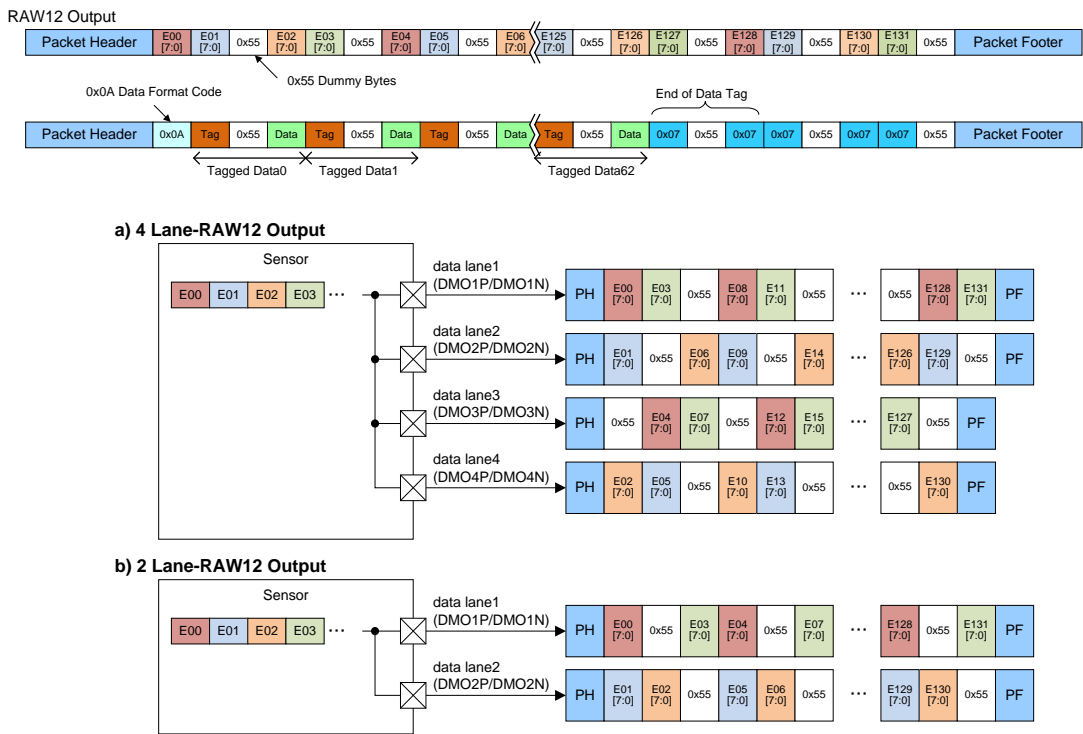Information inside the sensor is stored in the Data part.

Figure 49 MIPI Embedded Data Format

6-11-6 CLK Mode during Frame Blanking

This is a function to stop the MIPI clock during Frame Blanking.
The details of the register and timing are shown below.

Table 38 CLK Mode Setting Register during Frame Blanking

	Address	Bit	Name	Description
I²C register	0x1c40	[0]	FRAME_BLANKSTOP_CL	FRAME_BLANKSTOP_CL Control RUN/STOP of CSI-2 during Frame Blanking 0 : Stay in HS mode (Clock/Strobe output) during CLK Frame Blanking 1 : Transition to LP11 (Clock/Strobe stop) during CLK Frame Blanking Details are as follows: - When a valid frame starts, transition to HS-Clock status. - When the frame ends (after EOF output), transition from HS-Clock to LP11.

■FRAME_BLANKSTOP_CL =0
Clock (CL continuous_mode)
CKP/CKN

LP11   LP11   SOF
Data
D*P/D*N   EOF

Figure 50 CLK Mode during Frame Blanking (FRAME_BLANKSTOP_CL =0)

■FRAME_BLANKSTOP_CL =1
Clock (CL non-continuous_mode)   LP11   HS
CKP/CKN

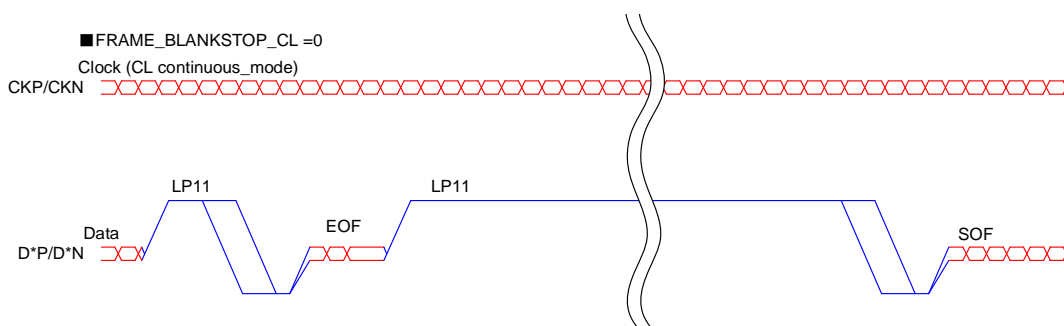LP11   LP11   SOF
Data
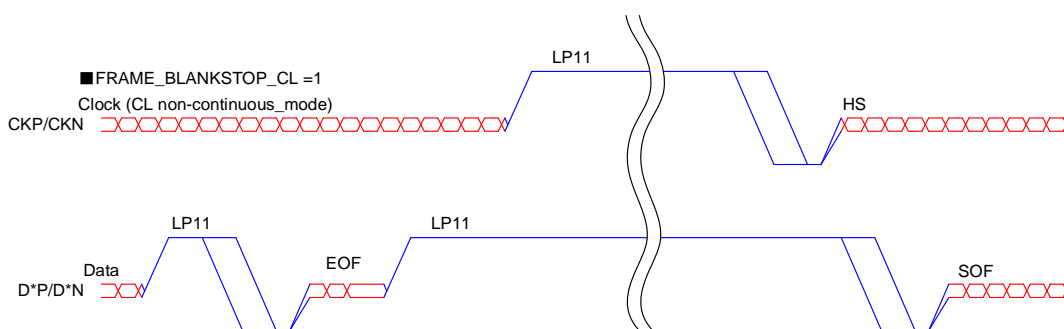D*P/D*N   EOF

Figure 51 CLK Mode during Frame Blanking (FRAME_BLANKSTOP_CL =1)

6-12 OTP (One Time Programmable Read Only Memory)

OTP for Customer Area is 3 ROWS (ROW00 to 02) (1ROW = 64 bits).
Map assignment of the customer area is shown in the table below.
Refer to the additional material (OTP manual) for how to write the value to OTP for Customer area.

Table 39 OTP Map for Customer Area

Address	ROW	Byte	Name	Bit
0x0300		0	Reserved (When you use the Slave address 0 to 4, please write to 8'h00.)	[7:0]
0x0301		1	IIC_SLAVE_ADR_SEL	[2:0]
0x0302	00	2	IIC_SLAVE_ADR0	[6:0]
0x0303		3	IIC_SLAVE_ADR1	[6:0]
0x0304		4	IIC_SLAVE_ADR2	[6:0]
0x0305		5	IIC_SLAVE_ADR3	[6:0]
0x0306		6	IIC_SLAVE_ADR4	[6:0]
0x0307		7	—	
0x0308		0	—	
0x0309		1	—	
0x030a		2	—	
0x030b	01	3	—	
0x030c		4	—	
0x030d		5	—	
0x030e		6	—	
0x030f		7	—	
0x0310		0	—	
0x0311		1	—	
0x0312		2	—	
0x0313	02	3	—	
0x0314		4	—	
0x0315		5	—	
0x0316		6	—	
0x0317		7	—	

6-13 Temperature Sensor

Internal temperature information can be read from the register or Embedded data. Since the temperature information is acquired during the readout period, this register value can be read after first phase.

Table 40 Register Setting for Temperature Sensor

Address	Bit	Register Name	Description
0x1400	[0]	THRM_SIGNED	Display format of temperature (THRM_DT_DEG) 0: offset binary 1: signed (2's complement)
0x1403	[7:0]	THRM_DT_DEG	Temperature [deg] Temperature = THRM_DT_DEG - 40 (THRM_SIGNED = 0) Temperature = THRM_DT_DEG (THRM_SIGNED = 1) Measurable range: - 40 to 125 [deg]

6-14 Light Source Control (Delay Adjustment)

It is possible to adjust the delay between the illumination timing and the exposure timing. The exposure timing can be delayed by using the sensor registers.

◆ There are three stages of delay adjustment: Coarse / Fine / Super Fine.

◆ The 1 step width of Coarse delay adjustment differs depending on Modulation frequency (FMOD).
   Formula of Coarse delay step
       Case of FMOD =51 MHz to 100 MHz: Step = (1 / FMOD) / 8
       Case of FMOD = 21 MHz to 50 MHz: Step = (1 / FMOD) / 16
       Case of FMOD = 4 MHz to 20 MHz: (1 / FMOD) / 32

◆ The 1 step width of delay adjustment of Fine / Super Fine is a fixed delay. However, since it is an analog delay, it is affected by Process/Voltage/Temperature condition.

◆ Coarse delay adjustment has the number of steps which is enough to cover one Modulation frequency cycle.

◆ Fine delay adjustment has the number of steps which is enough to cover the 1step width of coarse delay adjustment. However, when Modulation frequency is less than 5 MHz, the number of steps of fine delay adjustment is insufficient to cover the 1step width of coarse delay adjustment.

◆ Super Fine delay adjustment has the number of steps which is enough to cover the 1step width of fine delay adjustment.
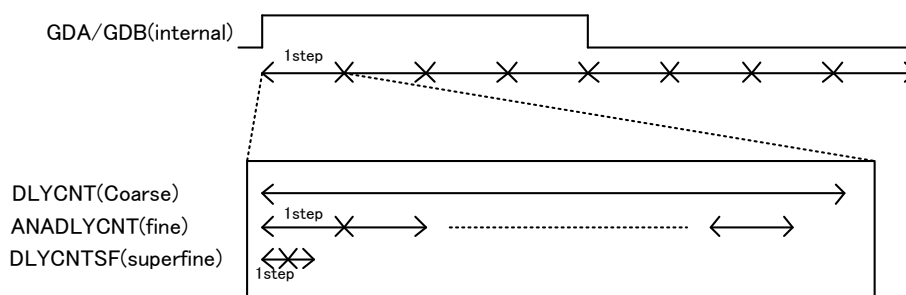

Figure 52 Delay Adjustment System

Table 41 Register Table for Delay Adjustment

Delay	Address	Bit	Register Name	1step (ps)	Note
coarse	0x201c	[7:0]	DLYCNT	Depend on FMOD	see the below table 32 to 255 (dec) is prohibited
fine	0x201d	[7:0]	ANADLYCNT	Typ 75ps	69 to 255 (dec) is prohibited
super fine	0x201e	[3:0]	DLYCNTSF	Typ 20ps	7 to 15(dec) is prohibited

7. How to Operate IMX556

7-1 Power on Reset

The XCLR pin is set to "LOW" and the power supplies are brought up. Then the XCLR pin should be set to "High" after INCK supplied.

7-2 Power on Sequence

7-2-1 Power on Slew Rate

Maximum slew rate (mV/us) is specified for each power supply to avoid oscillation during power on.
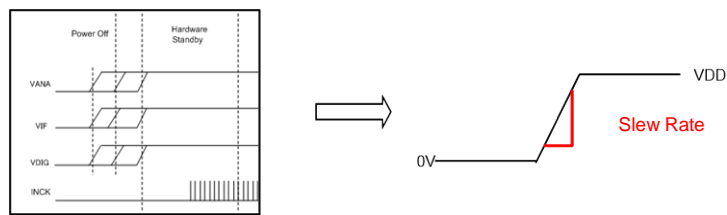

Figure 53 Power on Slew Rate

Table 42 Limitation on Power-on Slew Rate

Power Supplies	Slew Rate			Comment
	Min	Max	Unit	
VANA, VIF, VDIG,	—	25	mV/us	

7-2-2   Startup Sequence with I2C Serial Communication (External Reset/Sensor Master Mode)

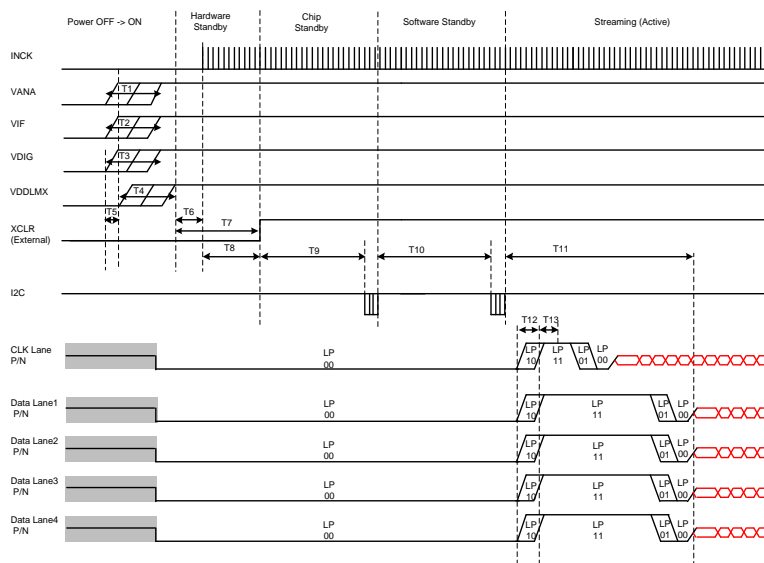Follow the power supply start up sequence below.

Figure 54   Startup Sequence with I2C Serial Communication (External Reset/Sensor Master Mode)

* Presence of INCK during Power Off is acceptable despite of above chart.

Table 43 Startup Sequence Timing Constraints (I2C Serial Communication Mode with External Reset/ Sensor Master Mode)

Item	Label	Min.	Max.	Unit	Comment
VANA rising – VANA ON	T1	VANA, VIF, VDIG may rise in any order.		us	
VIF rising – VIF ON	T2			us	
VDIG rising – VDIG ON	T3	VANA, VIF, VDDLMX may rise in any order.		us	
VDDLMX rising – VDDLMX ON	T4			us	
VDIG rising – VDDLMX rising	T5	0	-	us	
VANA, VIF, VDIG and VDDLMX rising - INCK start	T6	0	-	us	Presence of INCK during Power off is acceptable
VANA, VIF, VDIG and VDDLMX rising - XCLR rising	T7	100	-	us	
INCK start – XCLR rising	T8	0	-	us	
INCK start and XCLR rising till CCI Read version ID register wait time	T9	100	-	us	
STANDBY OFF till Send Streaming Command wait time	T10	12	-	ms	
Start of first streaming from Sending Streaming Command.	T11	-	2.8ms + Integration time	ms	
DPHY power up	T12	1	1,1	ms	
DPHY initialize	T13	100	110	us	

Note) XCLR needs to be Low until all power supplies complete power-on

7-2-3   Startup Sequence with I2C Serial Communication (External Reset/Sensor Slave Mode)

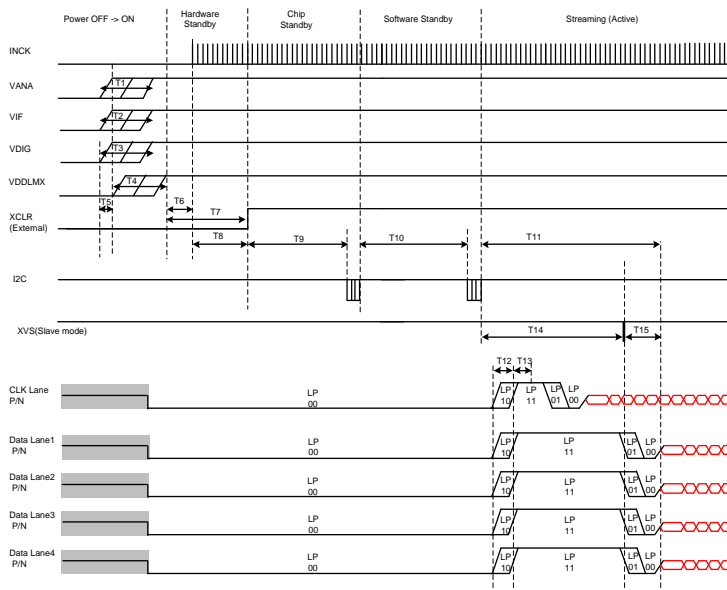Follow the power supply start up sequence below.

Figure 55 Startup Sequence with I2C Serial Communication (External Reset/Slave Mode)

* Presence of INCK during Power Off is acceptable despite of above chart.

Table 44 Startup Sequence Timing Constraints (I2C Serial Communication Mode with External Reset/Slave Mode)

Item	Label	Min.	Max.	Unit	Comment
VANA rising – VANA ON	T1	VANA, VIF, VDIG may rise in any order. VANA, VIF, VDDLMX may rise in any order.		us	
VIF rising – VIF ON	T2			us	
VDIG rising – VDIG ON	T3			us	
VDDLMX rising – VDDLMX ON	T4			us	
VDIG rising – VDDLMX rising	T5	0	-	us	
VANA, VIF, VDIG and VDDLMX rising - INCK start	T6	0	-	us	Presence of INCK during Power off is acceptable
VANA, VIF, VDIG and VDDLMX rising - XCLR rising	T7	100	-	us	
INCK start – XCLR rising	T8	0	-	us	
INCK start and XCLR rising till CCI Read version ID register wait time	T9	100	-	us	
STANDBY OFF till Send Streaming Command wait time	T10	12	-	ms	
Start of first streaming from Sending Streaming Command.	T11	-	T14 + T15 + Integration time	ms	

Item	Label	Min.	Max.	Unit	Comment
DPHY power up	T12	1	1,1	ms	
DPHY initialize	T13	100	110	us	
XVS falling from Sending Streaming Command.	T14	2.2	-	ms	
Start of first streaming from XVS falling	T15	-	0.6	ms	

Note) XCLR needs to be Low until all power supplies complete power-on

7-2-4 Startup Sequence with SPI Slave 4-wire Serial Communication (External Reset/Sensor Master Mode)

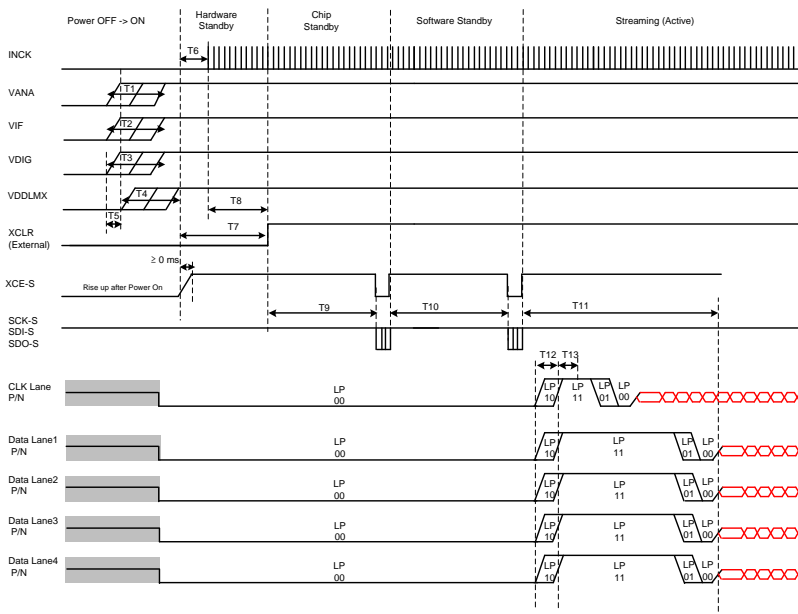Follow the power supply start up sequence below.

Figure 56   Startup Sequence with 2-wire Serial Communication (External Reset/Sensor Master Mode)

* Presence of INCK during Power Off is acceptable despite of above chart.

Table 45 Startup Sequence Timing Constraints (I2C Serial Communication Mode with External Reset/ Sensor Master Mode)

Item	Label	Min.	Max.	Unit	Comment
VANA rising – VANA ON	T1	VANA, VIF, VDIG may rise in any order. VANA, VIF, VDDLMX may rise in any order.		us	
VIF rising – VIF ON	T2			us	
VDIG rising – VDIG ON	T3			us	
VDDLMX rising – VDDLMX ON	T4			us	
VDIG rising – VDDLMX rising	T5	0	-	us	
VANA, VIF, VDIG and VDDLMX rising - INCK start	T6	0	-	us	Presence of INCK during Power off is acceptable
VANA, VIF, VDIG and VDDLMX rising - XCLR rising	T7	100	-	us	
INCK start – XCLR rising	T8	0	-	us	
INCK start and XCLR rising till CCI Read version ID register wait time	T9	100	-	us	
STANDBY OFF till Send Streaming Command wait time	T10	12	-	ms	
Start of first streaming from Sending Streaming Command.	T11	-	2.8ms + Integration time	ms	
DPHY power up	T12	1	1,1	ms	
DPHY initialize	T13	100	110	us	

Note) XCLR needs to be Low until all power supplies complete power-on

7-2-5 Startup Sequence with SPI Slave 4 wire Serial Communication (External Reset/Sensor Slave Mode)

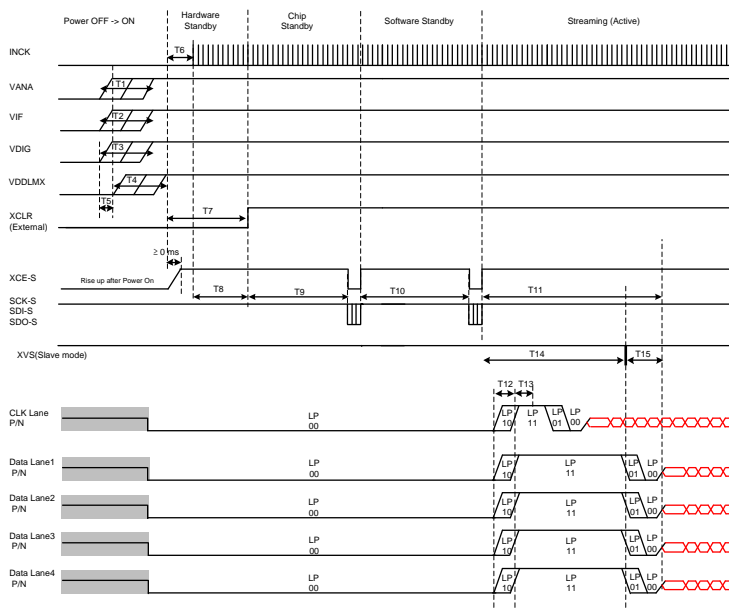Follow the power supply start up sequence below.

Figure 57 Startup Sequence with I2C Serial Communication (External Reset/Slave Mode)

* Presence of INCK during Power Off is acceptable despite of above chart.

Table 46 Startup Sequence Timing Constraints (I2C Serial Communication Mode with External Reset/Slave Mode)

Item	Label	Min.	Max.	Unit	Comment
VANA rising – VANA ON	T1	VANA, VIF, VDIG may rise in any order. VANA, VIF, VDDLMX may rise in any order.		us	
VIF rising – VIF ON	T2			us	
VDIG rising – VDIG ON	T3			us	
VDDLMX rising – VDDLMX ON	T4			us	
VDIG rising – VDDLMX rising	T5	0	-	us	
VANA, VIF, VDIG and VDDLMX rising - INCK start	T6	0	-	us	Presence of INCK during Power off is acceptable
VANA, VIF, VDIG and VDDLMX rising - XCLR rising	T7	100	-	us	
INCK start – XCLR rising	T8	0	-	us	
INCK start and XCLR rising till CCI Read version ID register wait time	T9	100	-	us	
STANDBY OFF till Send Streaming Command wait time	T10	12	-	ms	
Start of first streaming from Sending Streaming Command.	T11	-	T14 + T15 + Integration time	ms	

Item	Label	Min.	Max.	Unit	Comment
DPHY power up	T12	1	1,1	ms	
DPHY initialize	T13	100	110	us	
XVS falling from Sending Streaming Command.	T14	2.2	-	ms	
Start of first streaming from XVS falling	T15	-	0.6	ms	

Note) XCLR needs to be Low until all power supplies complete power-on

7-3   Power Down Sequence with 2-wire Serial Communication (External Reset)

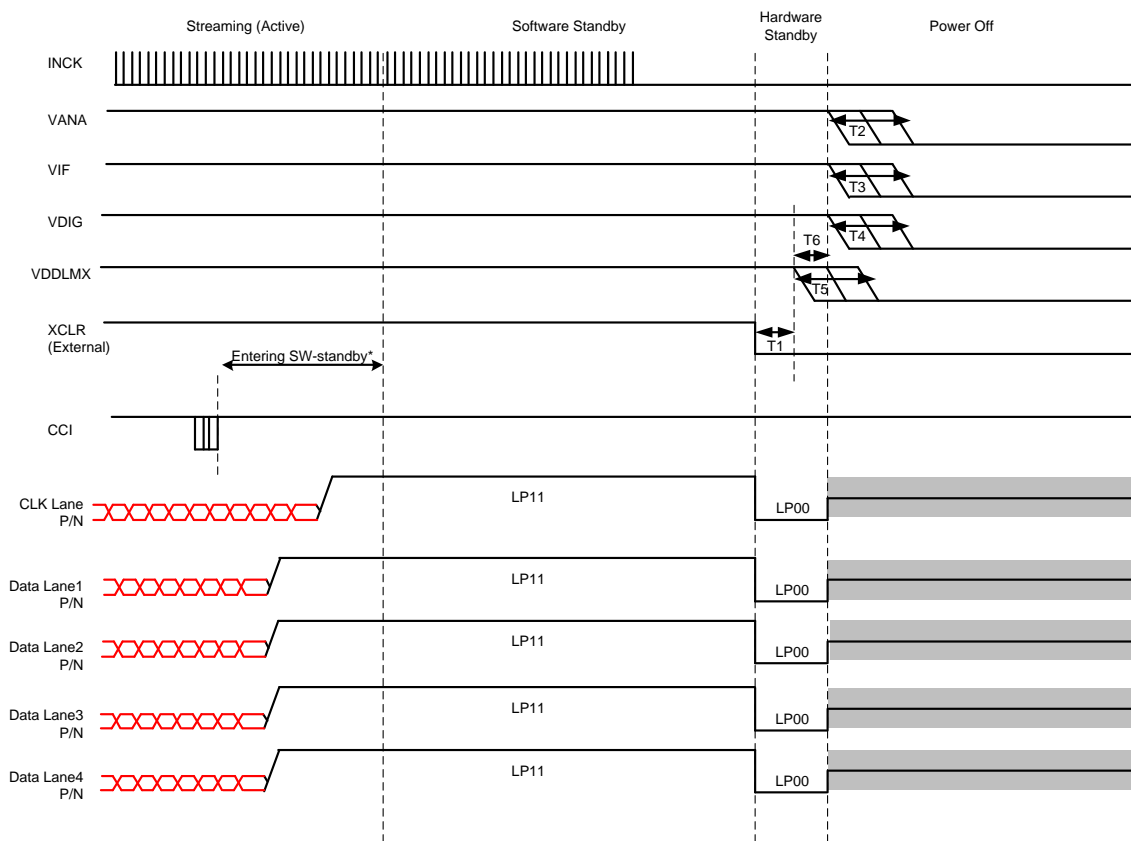Follow the power down sequence below.

Figure 58   Power Down Sequence with 2-wire Serial Communication (External Reset)

Table 47 Power Down Sequence Timing Constraints (2-wire Serial Communication Mode with External Reset)

Item	Label	Min.	Max.	Unit	Comment
XCLR Neg-edge – VDDLMX fall	T1	0	-	us	
VANA ON – VANA fall	T2	VANA, VIF, VDIG may fall in any order. VANA, VIF, VDDLMX may fall in any order.		us	
VIF ON – VIF fall	T3			us	
VDIG ON – VDIG fall	T4			us	
VDDLMX ON – VDDLMX fall	T5			us	
VDDLMX fall – VDIG fall	T6	0	-	us	

7-4   Start Sequence (XCLR – Streaming)

The flow from XCLR rising to the start of streaming is shown below.

1. IMX556 loads automatically the data from OTP. Register access is prohibited during this period.
2. Set the registers for mode operation. [Reg Set (1)]
   For mode operation, some initial settings of registers (GLOBAL_SETTING registers) are necessary. Refer to "Standard Register Setting" for details.
3. Set the register (STANDBY = 0). Then IMX556 transits from Chip-Standby to the Software(SW)-Standby state. [Reg Set (2)]
   Mode operation registers and Global settings can be set after STANDBY = 0 sending also.
   When using Master mode, TMASTER register must be sent after STANDBY = 0 sending. Refer to "6-6-6 Master, Slave".
4. Set the register (MODE_SEL = 1) and the state is shift to Streaming state. [Reg Set (3)]
5. After WakeUp in front of Streaming state, the frame operation is started. And the pixel data and embedded data are output from the MIPI.
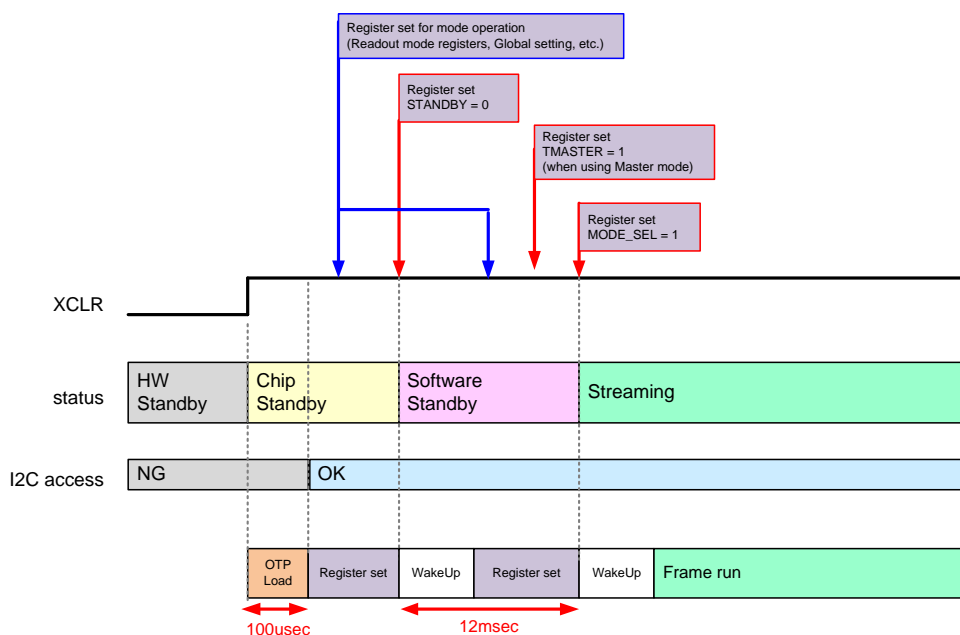

Figure 59 Start Sequence

Table 48 Register Table for Start Sequence

Address	Bit	Register Name	Description
0x1000	[0]	STANDBY	0: Chip Standby - Off 1: Chip Standby
0x1001	[0]	MODE_SEL	Mode Select 0: Software Standby 1: Streaming

7-5 Standby Sequence (Streaming – SW Standby)

The transition flow from the streaming state to SW-standby state is shown below.
1. the register setting is sent (MODE_SEL = 0) during streaming
2. After all frame data is output, the state is shift from Streaming to SW-Standby.
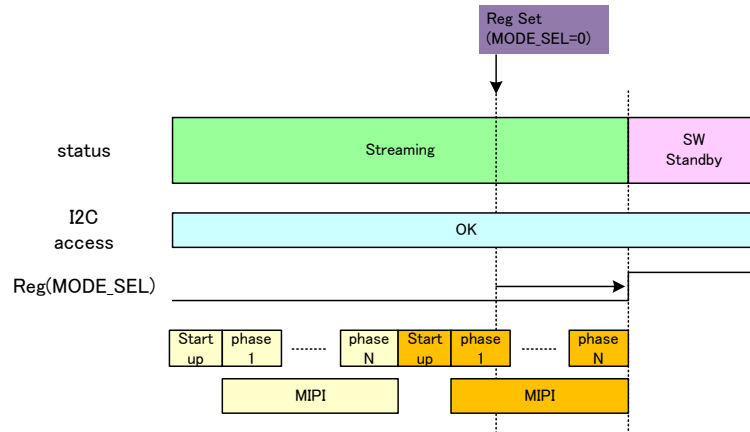

Figure 60 Standby Sequence

8.   Other Functions

8-1   Sub-LVDS /CMOS Select for Illumination Signal

The illumination signal interface can be chosen Sub-LVDS and CMOS.

Table 49 Register Setting for Sub-LVDS/CMOS Select

Address	Bit	Register Name	Description
0x10e2	[0]	LVDS_EN	Sub-LVDS/CMOS select for illumination signal 0: CMOS (LEDP) 1: Sub-LVDS (LEDP: positive, LEDN: negative)

8-2   Test pattern Output (types of test patterns)

This sensor can output test patterns by using a built-in pattern generator.

Table 50 Register Setting for Test Pattern Generator

Address	Bit	Register Name	Description
0x1405	[0]	TESTIMG_PAT_NUM[8]	display test pattern
0x1406	[7:0]	TESTIMG_PAT_NUM[7:0]	004h: PN9(*1) Others: forbidden
0x1407	[0]	TESTIMG_PAT_EN	test pattern enable 0h: Off 1h: On

*1 PN9 is one of Pseudo Random Binary Sequence. The other name is PRBS9.
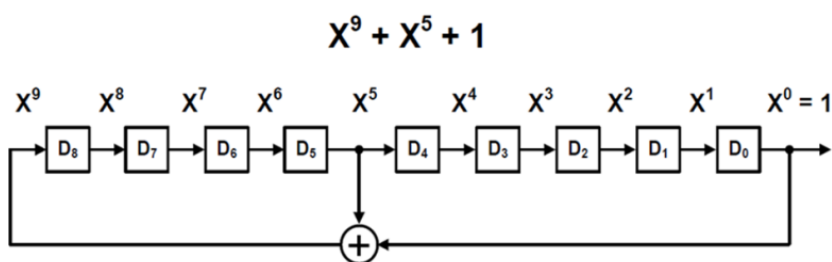
$$X^9 + X^5 + 1$$

Figure 61 PN9 Linear Feedback Shift Registers

8-3 LEDEN

LEDEN output is enable signal for LED driver which in case of needed as below timing. Signal is turned high from start of Reset Sequence and turned low from the end of Integration. This pulse cannot be controlled independently.
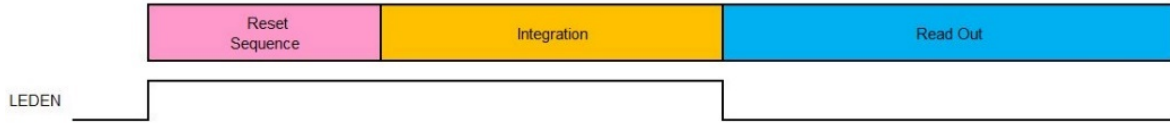

Figure 62 LEDEN

Table 51 LEDEN Setting

|	Address	Bit	Register Name	Setting Value
I2C register	0x21c4	[7:0]	LDD_TIM_EN[7:0]	LEDEN enable 0h: LEDEN disable FFh : LEDEN enable

9. Electrical Characteristics

The Electrical Characteristics of the IMX556 is shown below.

9-1 DC Characteristics

Table 52 DC Characteristics

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	VDDHCM VDDHAN VDDHSN VDDHCP VDDSUB	VANA		2.6	2.7	2.8	V
	VDDMIO VDDMIF VDDHSR	VIF		1.7	1.8	1.9	V
	VDDLSC VDDLPL VDDLCN VDDLIF	VDIG		1.1	1.2	1.3	V
	VDDLMX	VDDLMX		1.1	1.2	1.3	V
Digital Input Voltage	LEDFB LEDEN INCK XCLR POREN SLASEL XCES SDIM TENABLE CMODE GPIO XVS	VIH		0.8*VIF	-	-	V
		VIL		-	-	0.2*VIF	V
Digital Output Voltage	LEDP LEDN LEDEN SDOS SCKM SDIM SDOM XCEM1 XCEM2 GPIO XVS	VOH	I=-2.0mA	VIF-0.2	-	-	V
		VOL	I=2.0mA	-	-	0.2.	V
Sub-LVDS Output	LEDP,LEDN	VCM		VIF/2-0.1	VIF/2	VIF/2+0.1	V
		VOD	Termination resistance: 100ohm	100	150	220	mV

74
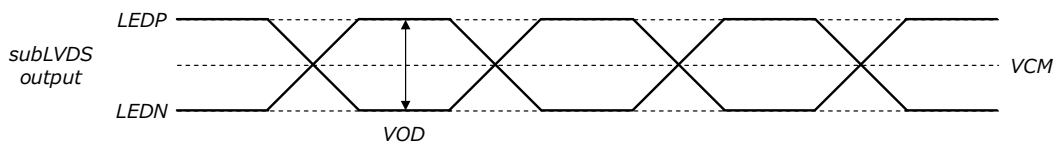
9-2   AC Characteristics

9-2-1   Master Clock Waveform Diagram

9-2-1-1   INCK Square Waveform Input Specifications

Input specifications are shown below when square-wave signal is input directly into the external pin INCK.
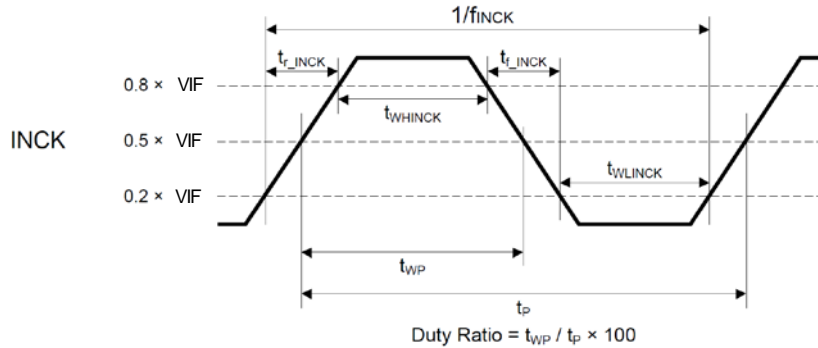

Figure 63   Master Clock Square Waveform Input Diagram

Table 53 Master Clock Square Waveform Input Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
INCK clock frequency	f_{INCK}	8	8, 16, 32	32	MHz
INCK low level width	t_{WLINCK}	10			ns
INCK high level width	t_{WHINCK}	10			ns
INCK Duty (Defined as 0.5 x VIF)	Duty Ratio	45	50	55	%
INCK Tr	t_{r_INCK}			5	ns
INCK Tf	t_{f_INCK}			5	ns

9-2-1-2   INCK Sine Waveform Input Specifications

IMX556 does not support the "AC coupled connection". Therefore, there is no description of AC characteristics.

9-2-2   I2C Serial Communication Block Characteristics

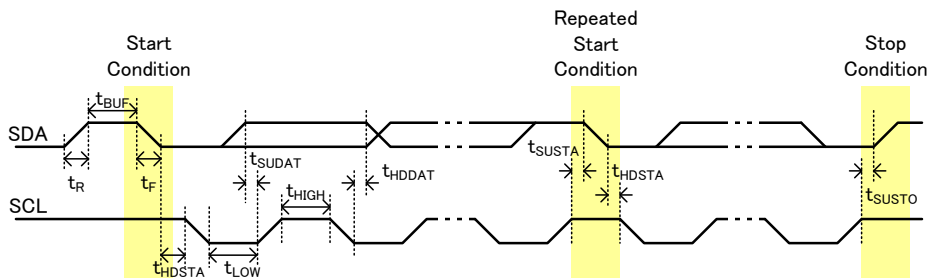I2C serial communication characteristics are shown below.

Figure 64   I2C Serial Communication Block Specification

Table 54 I2C Serial Communication Block Specification

Parameter	Symbol	Conditions	Min.	Max.	Unit
Low level input voltage	V_{IL}		-0.3	$0.3V_{IF}$	V
High level input voltage	V_{IH}		$0.7V_{IF}$	$VIFmax + 0.5$	V
Low level output voltage	V_{OL}	VIF < 2 V, Sink 3 mA	0	$0.2V_{IF}$	V
Output fall time	t_{of}	Load 10 pF – 400 pF, 0.7 VIF→0.3 VIF	6	250	ns
Input current	I_I	0.1 VIF→0.9 VIF	-10	10	uA
SDA I/O capacitance	$C_{I/O}$			10	pF
SCL Input capacitance	C_I			10	pF

Table 55 I2C Serial Communication Block AC Specification

| Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	0	400	kHz
Rise time (SDA and SCL)	t_R	20	300	ns
Fall time (SDA and SCL)	t_F	6	300	ns
Hold time (start condition)	t_{HDSTA}	0.6	—	us
Setup time (rep.-start condition)	t_{SUSTA}	0.6	—	us
Setup time (stop condition)	t_{SUSTO}	0.6	—	us
Data setup time	t_{SUDAT}	100	—	ns
Data hold time	t_{HDDAT}	0	0.9	us
Bus free time between Stop and Start condition	t_{BUF}	1.3		us
Low period of the SCL clock	t_{LOW}	1.3		us
High period of the SCL clock	t_{HIGH}	0.6		us

9-2-3 SPI 4-Wire Serial Communication
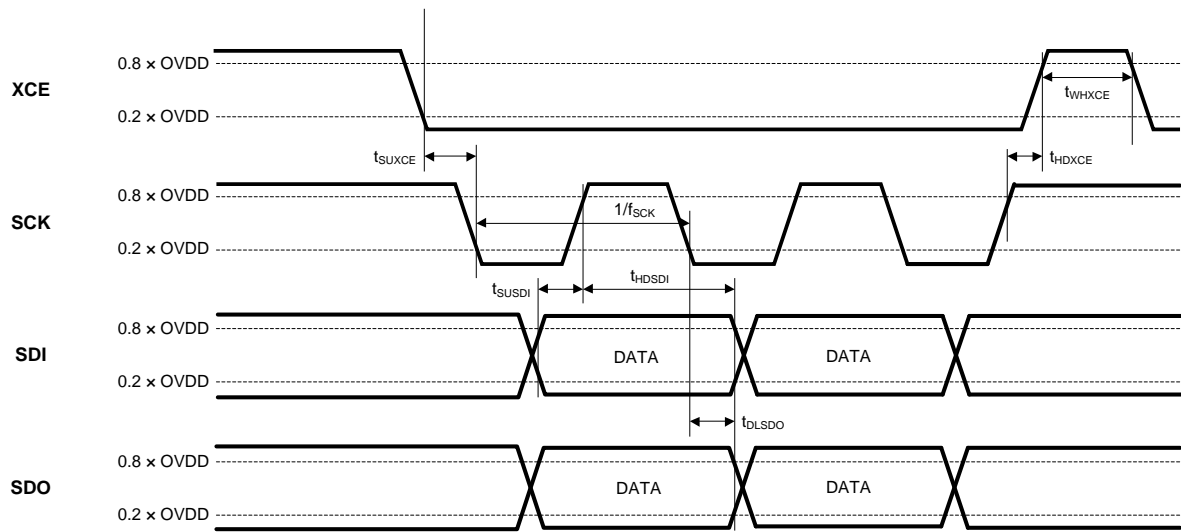
Figure 65 SPI 4-wire Serial Communication Specification

Table 56 SPI 4-wire Serial Communication Waveform Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCK clock frequency	f_{SCK}	—	—	30	MHz	Under Operation
		—	—	INCK/2	MHz	During Standby
XCE input setup time	t_{SUXCE}	5	—	—	ns	
XCE input hold time	t_{HDXCE}	5	—	—	ns	
XCE High level pulse width	t_{WHXCE}	20	—	—	ns	
SDI input setup time	t_{SUSDI}	5	—	—	ns	
SDI input hold time	t_{HDSDI}	5	—	—	ns	
SDO output delay time	t_{DLSDO}	0	—	20	ns	Output load capacitance: 20 pF

9-2-4 Current Consumption

Table 57 Current Consumption

Item			Typ.(*1)	Max.(*2)	Unit
Full Pixel 4phase/frame 30fps@depth 1ms@Integration time/phase Fmod 100MHz Output: A-B	Analog Current	IANA	9.0	53	mA
	Digital Current	IDIG	60	170	mA
	Mix Current	ILMX	240	3900	mA
	I/O Current	IIF	1.7	2	mA
HW/SW Stand-by	Analog Current	IANA	0.54	2.4	mA
	Digital Current	IDIG	0.55	60	mA
	Mix Current	ILMX	0.37	9	mA
	I/O Current	IIF	27	62	uA

*1. VANA=2.7V, VDIG/VDDLMX=1.2V, VIF=1.8V, Ta=25℃
*2. VANA=2.8V, VDIG/VDDLMX=1.3V, VIF=1.9V, Tj=-10 to 60℃

10.   Sensor Characteristics

10-1 Sensor Characteristics

Table 58 Sensor Characteristics

(120fps/1phase, VANA=2.7V, VDIG=1.2V, VDDLMX=1.2V, VIF=1.8V, Tj=60℃)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement Method	Remarks
Dark signal	Vdt			3	LSB	11-3-1	
DC contrast	Cmod	65	-	-	%	11-3-2	
Saturation signal	Vsat	1023			LSB	11-3-3	

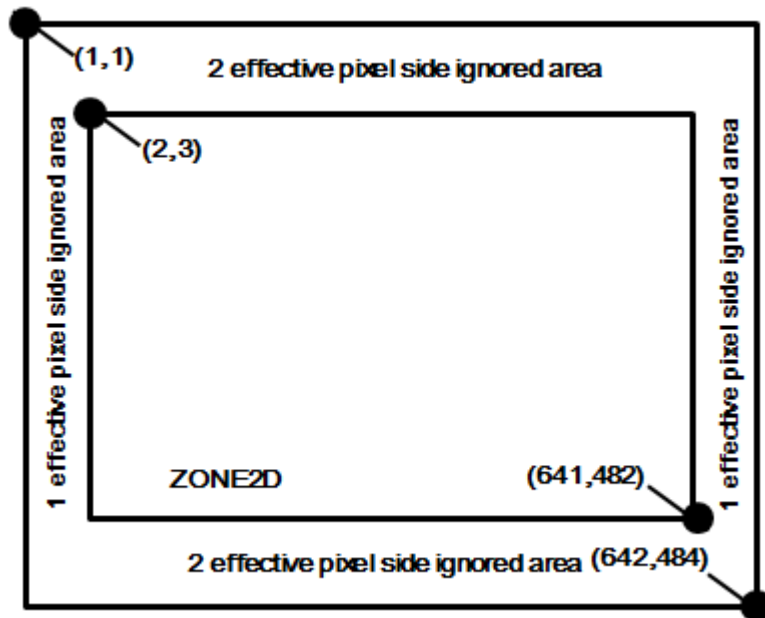### 10-2 Zone Definition used for specifying sensor characteristics

Figure 66 Zone Definition Diagram

Note: These applied mode A, B, A-B, A+B. A&B is applied for each tap separately

"ZONE2D" area is guaranteed the pixel performance.

11. Measurement Method for Sensor Characteristics

11-1 Measurement Conditions

The device operation conditions are at the typical values of the bias.

Table 59 Measurement Conditions

Supply voltage	VANA = 2.7 V, VDIG = 1.2 V, VDDLMX = 1.2 V, VIF = 1.8 V

11-2 Definition of Standard Imaging Conditions

Use light source with IR wavelength 940nm as a subject. The luminous intensity to the sensor receiving surface is adjusted to the signal level shown in each measurement item by the light source output, lens aperture or integration time control by the electronic shutter.

11-3 Measurement Method

11-3-1 Dark Signal

Measure the output difference between the signal output (Va)@6ms integration time and the signal output (Vb)@1ms integration time at the device junction temperature of 60°C and the device in the light-obstructed state, and calculate the signal output at 5 [ms] integration time by them using the following formula. Then, this is Vdt [LSB] normalized with 1ms integration time.

$$Vdt = (Va - Vb) / 5 \text{ [LSB]}$$

11-3-2 DC Contrast

Set the measurement condition to the standard imaging condition III. After adjusting the luminous intensity so that the average value of signal outputs is 520 [LSB]. Measure the number of electrons collected at proper position for each of Tap-A (Q1) and Tap-B(Q2), and substitute the values into the following formula for each case of Tap-A (Q1) and Tap-B (Q2).

$$Cmod = (Q1 - Q2) / (Q1 + Q2)$$

11-3-3 Saturation Signal

Set the measurement condition to the standard imaging condition. After adjusting the luminous Intensity to 12 times the intensity with the average value of signal outputs, 388 [LSB] without Dark offset, measure the average value of the pixel signal outputs.

12. CRA Characteristics of Recommended Lens

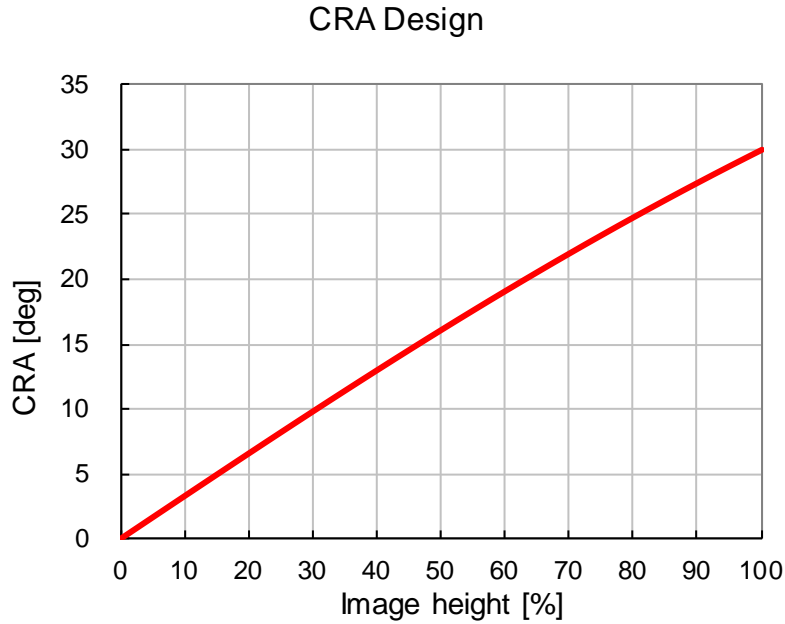The following figure and table shows the target CRA (chief ray angle) of this sensor.

CRA Design

Figure 67 Target CRA

Table 60 Target CRA (values)

Image Height		Target CRA
[%]	[mm]	[deg.]
0.0	0.00	0.0
10.0	0.40	3.3
20.0	0.80	6.6
30.0	1.20	9.8
40.0	1.60	13.0
50.0	2.00	16.1
60.0	2.40	19.1
70.0	2.80	22.0
80.0	3.20	24.8
90.0	3.60	27.5
100.0	4.00	30.0

13. Spot Pixel Specification

13-1 Spot Pixel

Table 61 Spot Pixel Specifications

(VANA = 2.7 V, VDIG = 1.2 V, VIF = 1.8 V, Tj = 60 ˚C)

Type of distortion	Level Note 1)	Maximum distorted pixels in each zone			Remarks
		Zone 2D	Ineffective OB	Effective OB	
Black or white pixels at high light	30% ≦ D	6144	No evaluation criteria applied		
White pixels in the dark	268LSB≦D		No evaluation criteria applied		1msec integration time
Continuous Black or white pixels at high light	30% ≦ D	467	No evaluation criteria applied		
Continuous White pixels in the dark	268LSB≦D		No evaluation criteria applied		1msec integration time

Note) 1. D...Spot pixel level.
2. Continuous pixels in the horizontal or vertical direction are NG.
3. The above chart (hereinafter referred to as the "Spot Pixel Specifications") is the standard only for sorting image sensor products in this specification book (hereinafter referred to as the "PRODUCTS") before shipment from a manufacturing factory. Sony Semiconductor Solutions Corporation and its distributors (collectively hereinafter referred to as the "Seller") disclaim and will not assume any liability even if actual number of distorted pixels of the PRODUCTS delivered to you exceeds the maximum number set forth in the Spot Pixel Specifications. You are solely liable for any claim, damage or liability arising from or in connection with such distorted pixels. If the Seller separately has its own product warranty program for the PRODUCTS (the "Program"), the conditions in this specification book shall prevail over the Program and the Seller shall not assume any liability under the Program to the extent there is contradiction.

13-2 Single Defect Pixel

The following figure shows spot defect pixel. One pixel has two storage nodes and can output both through MIPI if register set to Dual Data output mode. Either A or B or both are counted as 1 defect. Defects are either under "Black or white pixels at high light" or "White pixels in the dark".
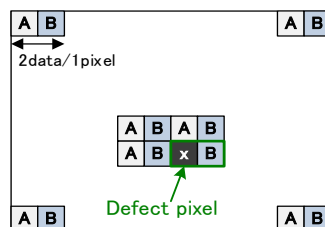

Figure 68   Spot Defect Pixel

13-2-1 Black or White Pixels at High Light

After adjusting the average value of the pixel signal output to 520 LSB, measure the local dip point (black pixel at high light, VXB) and peak point (white pixel at high light, VXK) in the pixel A/B signal output Vx (x = A/B), and substitute the values into the following formula.

$$D_K(\text{White Pixel level}) = (V_{XK}/\overline{V_X}) \times 100[\%]$$

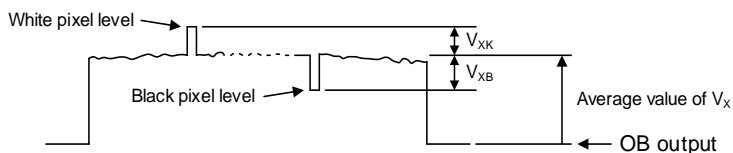$$D_B(\text{Black Pixel level}) = (V_{XB}/\overline{V_X}) \times 100[\%]$$

Figure 69 Measurement Method for Spot Pixels

13-2-2 White Pixels in the Dark

Set the device to a dark setting and measure the local peak point of the signal output waveform using the average value of the dark signal output as a reference.

14. Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, particle radiation such as cosmic rays etc. may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".)
Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Semiconductor Solutions Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Semiconductor Solutions Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 ˚C)	Annual number of occurrence
5.6 mV or higher	18 pcs
10.0 mV or higher	10 pcs
24.0 mV or higher	4 pcs
50.0 mV or higher	2 pcs
72.0 mV or higher	1 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

Material_No.03-0.0.10

15. Note on Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
   Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
   If dust or other is stuck to a glass surface, blow it off with an air blower.
   (For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Recommended temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (- 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C
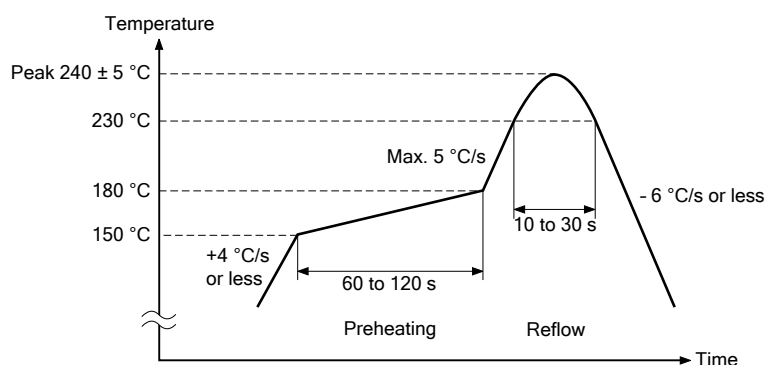
(2) Reflow conditions
  (a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.
  (b) Perform the reflow soldering only one time.
  (c) Finish reflow soldering within 72 h after unsealing the degassed packing.
      Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.
  (d) Perform re-baking only one time under the condition at 125 °C for 24 h.
  (e) Note that condensation on glass or discoloration on resin interfaces may occur if the actual temperature and time exceed the conditions mentioned above.
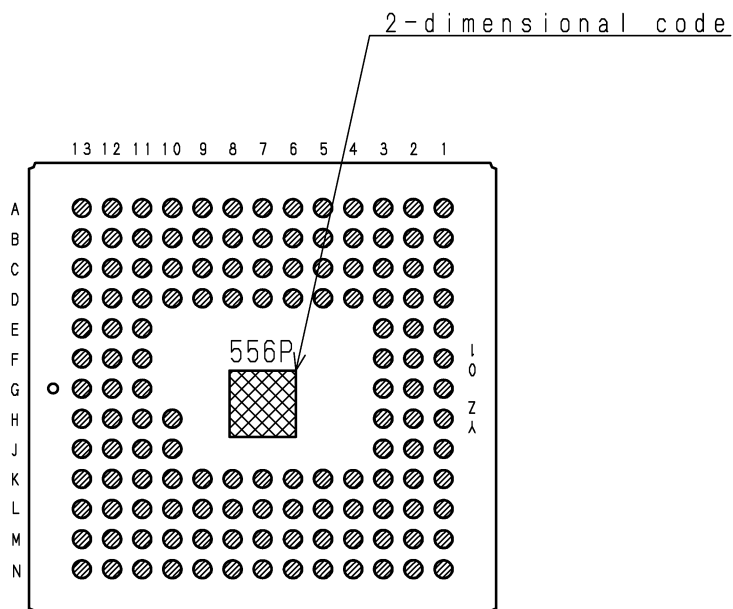
(3) Others
  (a) Carry out evaluation for the solder joint reliability in your company.
  (b) After the reflow, the paste residue of protective tape may remain around the seal glass.
      (The paste residue of protective tape should be ignored except remarkable one.)
  (c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others
  (1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
  (2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
  (3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
  (4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
  (5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

Material_No.14-0.0.9
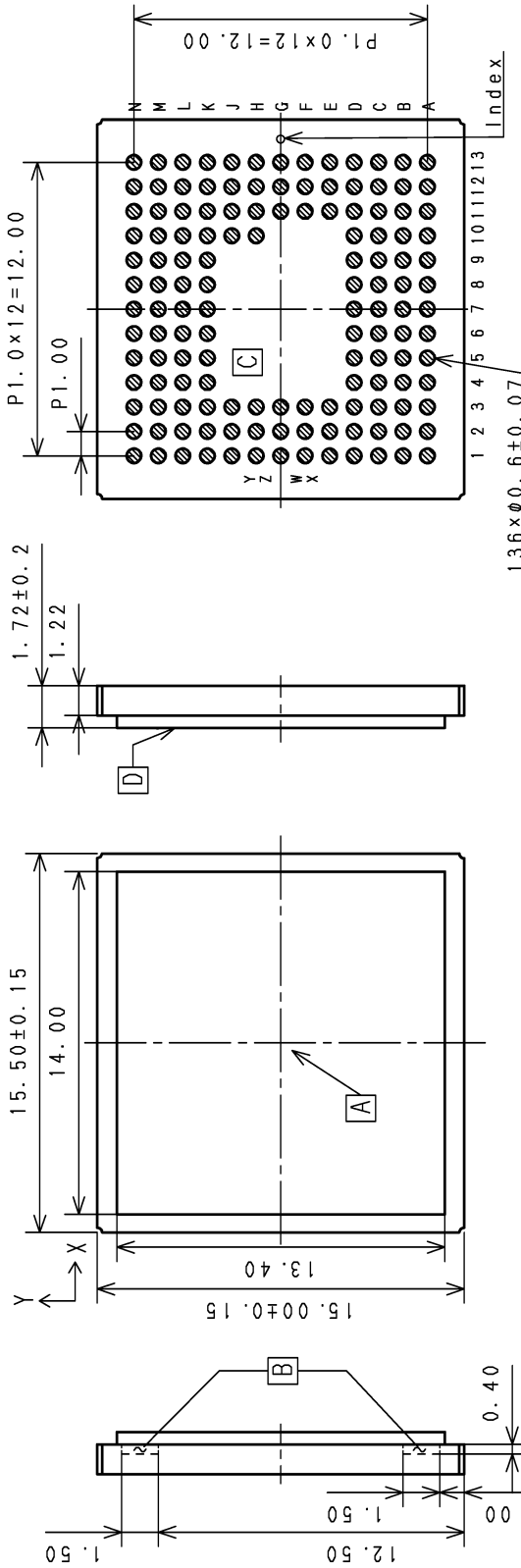
16. Marking

2-dimensional code

```
      13 12 11 10  9  8  7  6  5  4  3  2  1
   A   ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘
   B   ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘
   C   ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘
   D   ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘
   E   ⊘ ⊘ ⊘                 ⊘ ⊘ ⊘
   F   ⊘ ⊘ ⊘      556P        ⊘ ⊘ ⊘    I 0
   G ○ ⊘ ⊘ ⊘      ▨▨         ⊘ ⊘ ⊘
   H   ⊘ ⊘ ⊘ ⊘    ▨▨         ⊘ ⊘ ⊘ ⊘  Z Y
   J   ⊘ ⊘ ⊘ ⊘                ⊘ ⊘ ⊘
   K   ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘
   L   ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘
   M   ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘
   N   ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘ ⊘
```

Note:Following characters enter into "Y",and"Z".(No Au coat)

Y:In English upper case character,One character
Z:Number,single number

SONY

17. Package Information

Unit: mm

136pin-LGA

1) "A" is the center of the effective image area
2) The two points "B" of the package are the horizontal reference
   The point "B'" of the package is the vertical reference
3) The bottom "C" of the package is the height reference
4) Base level "S" is a virtual flat surface calculated at three points (A1,N1,N13)
   of back side terminal
5) The center of the effective image area relative to "B" and "B'" is
   (X,Y) = (7.444, 7.035) ± 0.225mm
6) The rotation angle of the effective image area relative to "X" and "Y" is ±1°
7) The height from the bottom "C" to the effective image area is 0.62 ± 0.1 mm
   The height from the top of cover glass "D" to the effective image area is 1.1 ± 0.15mm
8) The tilt of the effective image area relative to the bottom "C" is less than 0.05mm
9) The thickness of the cover glass is 0.5mm, and the refractive index is 1.5
10) As for standard for resin overflow in package outside,
    it shall be accepted up to outermost line tolerance of package
11) One character of alphabet or number shall be placed from W to Z part
    (Plating pretermission)
12) General tolerance : ± 0.2mm

PACKAGE STRUCTURE	
PACKAGE MATERIAL	Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	
PACKAGE WEIGHT(Typ.)	1.0g
DRAWING NUMBER	AS-B114(E)

88