USB 2.0 Video

PC Camera Controller

SN9C2809EJG

Datasheet

Version: v0.02

For the latest data sheet, please visit www.sunnywale.com

Revision	Date	Description
0.01	2020-06-17	Draft Release
0.02	2020-07-13	1. Modify section2.4 ISP max resolution.

Table of Contents

1 General Description

The SN9C2809 is a high resolution webcam controller. Besides improved image quality, this generation of ISP supports wide dynamic range (WDR) and vertical lens distortion correction (VLDC) to bring better visual experiences. It not only brings less noise image for human eye but also makes the analysis work in machine-vision easier. For modern high resolution and AI applications, SN9C2809 would be a higher performance and cost effective choice.

Besides video ISP, SN9C2809 also supports UAC 1.0 specification which records audio form microphone input. Programmable audio sampling frequency from 8KHz to 48KHz and resolution of 8/16 bit with mono or stereo.

The major functions of SN9C2809 include controlling the CMOS sensor, receiving the image data, converting it to video stream, and then sending data to the host via USB. It's compliant with USB 2.0 High-Speed (HS) and USB Video Class (UVC) 1.1/1.5 over ISO or Bulk in transfer. Compliance with the public standards makes SN9C2809 easy to be integrated into various fields of applications that need high quality video like high resolution tablet built-in camera, camcorder, surveillance, video conference and machine vision (AI).

SN9C2809 supports both parallel and MIPI-CSI2 1/2/4-lane CMOS sensor interfaces and the performance of ISP is up to 3840x2160@25fps or up to 1920x1080@60fps. The high performance Motion-JPEG engine and bit rate controller provides various compression ratios to meet bandwidth requirement. This system is controlled by the embedded micro-controller with the built-in statistics of AE / AWB. The flexible architecture includes the mask ROM, internal RAM and external serial-flash which can store the customized codes and parameters.

There are 3 built-in regulators and no needs of external oscillator, these features make it able to further save BOM and PCB area. The SN9C2809 is the best choice for the compact modern electronic product design.

2 Features

2.1 System

- Single 3.3v power supply
- Extreme low power consumption, < 30mA when standby and < 0.5mA when suspend (Power consumption of sensor is not included)
- Built-in Clock Synthesizer for performance and power saving
- Support external oscillator input with 12MHz frequency
- Built-in PLL for internal clock generation
- Using external serial flash to store customized code and data
- No external RAM needed
- 2 sets of selectable 1.0/1.2/1.5/1.85/2.0/2.85/3.0/3.3 V internal LDO to supply CMOS sensor analog and IO power
- QFN package of 68-pins

2.2 USB Controller

- USB 2.0 high-speed and full-speed compatible
- USB Video Class 1.1 / 1.5 compliant
- USB Audio Class 1.0 compliant
- USB 2.0 HS/FS compatible and auto switch
- USB FS mode and USB disconnection are programmable
- USB Low Power Management Sleep State with RTD3
- 6 endpoints: 1 CONTROL pipe, 2 Interrupt IN , 1 Bulk IN (Video stream) and 2 Isochronous-IN (MJPEG/YUY2 video stream, and audio stream)
- 6 alternate settings for Video Streaming Interface

2.3 Sensor Interface

2.3.1 Parallel Interface

- Support up to 3M (2304x1296) 8/10-bit parallel CMOS sensor
- Support image data type: Y8, YUV422 (YUY2) 8-bits, and RAW8/10 (Bayer-Pattern)
- Output MCLK: 120MHz based output clock request for CMOS sensor silicon
- Up to 192MHz pixel clock is acceptable
- Support industrial standard 2-wire serial interface to control sensor

2.3.2 MIPI CSI-2 RX Interface

- MIPI-CSI2 with D-PHY: 1 clock lane and 4 data lane which can be configured to 1/2/4-lane
- Support up to 8M (3840x2160) MIPI CSI-2 CMOS sensor
- Support image data type: YUV422 (YUY2) 8-bits, and RAW8/10 (Bayer-Pattern)
- Output MCLK: 120MHz based output clock request for CMOS sensor silicon
- Data rate up to 1Gbps/Lane
- MIPI protocol complies to MIPI Camera Serial Interface 1.0 specification Camera Serial Interface 2 v1.0 (CSI-2)
- Support industrial standard 2-wire serial interface to control sensor

2.4 Color Processing

- Resolution support up to 8M pixels (3840x2160)
- ISP clock up to 240MHz
- Frame rate up to 8M@25fps or FHD@60fps
- AE histogram statistics
- AWB window statistics
- AF edge window statistics
- On-the fly defect-pixel cancellation
- Lens shading compensation for R/G/B channel
- Color interpolation Low pass filter
- Individual digital color gain control for R/Gr/Gb/B channels
- Individual digital color gain control for Y/Cb/Cr channels
- Pixel offset (optical black) compensation for R/Gr/Gb/B channels
- Programmable gamma table for RGB channels
- Programmable color conversion matrix for R/G/B input
- Configurable noise reduction
- De-color aliasing in Edge
- Configurable edge enhancement
- Programmable gamma table for Y channel
- Configurable windowing function after processed image
- Programmable hue and saturation
- Auto Gamma for backlight preview
- Auto 50Hz/60Hz frequency switch
- Auto de-flicker
- Wide Dynamic Range (WDR)
- Vertical lens distortion correction (VLDC)

2.5 Scaling Engine

- Scale down only on Y/Cb/Cr format
- With LPF to eliminate artifact (Satisfy Microsoft Lync unify under max. scaling down ratio which is 1280->160 pixels)
- Max scaling down path is from 3840x2160 to 320x240

2.6 Line OSD

- Displays Up to 4 Rows x 24 Characters with independent start position
- Character Size HxV: 16x16, 16x24
- Line zoom (x1, x2, x3, x4 to x8 for both X and Y coordinates)
- Character with transparency and other 3 color choices.
- 64 different user definable characters can be stored in RAM.
- Start address is 16-pixel alignment to output image window
- With precise accumulator to account the timer of OSD

2.7 JPEG Encoder

- Built-in JPEG encoder support USB Video Class MJPEG payload
- JPEG YUV422 baseline format
- 128 bytes quantization tables for Y and C provide programmable compression ratio
- Support frame level bite rate control mechanism

2.8 Video / Still Image

- UVC output video / still image format:
  - USB Video Class Uncompressed YUY2 payload (16bits/pixel)
  - USB Video Class MJPG payload
  - Still Image capture is able to support UVC still image capture method 1 & 2
- Video streaming up to 8M@25fps or FHD@60fps at USB2.0 high-speed mode

2.9 Frame Rate

- Frame rate considering USB bandwidth limitation

- Under the conditions that USB 2.0 ISO throughput=24MB/s, USB2.0 Bulk throughput=35MB/s, and JPEG compression ratio = 18:1. The supported resolution list is listed in Table 2.9-1.

Resolution	Frame rate					
	Y8		YUV422		JPEG	
	UVC ISO	UVC BULK	UVC ISO	UVC BULK	UVC ISO	UVC BULK
3840x2160 (8M)	1	1	1	1	25	25
3264x2448 (8M)	1	1	1	1	25	25
3264x1836 (6M)	1	5	1	1	25 (*1)	25 (*1)
2592x1944 (5M)	1	5	1	1	25 (*1)	25 (*1)
2688x1520 (4M)	5	5	1	1	25 (*1)	25 (*1)
2560x1440 (3M)	5	5	1	1	25 (*1)	25 (*1)
2304x1296 (3M)	5	10	1	5	25 (*1)	25 (*1)
2048x1536 (3M)	5	10	1	5	25 (*1)	25 (*1)
1920x1080 (2M)	10	15	5	5	60	60
1600x1200	10	15	5	5	60	60
1280x720	25	35	10	15	60	60
800x600	50	60	25	35	60	60
640x480	60	60	35	55	60	60
640x400	60	60	45	60	60	60
640x360	60	60	50	60	60	60
352x288	60	60	60	60	60	60
320x240	60	60	60	60	60	60

Table 2.9-1 Supported list of frame rate

- Frame rate considering sensor characteristic
  - The maximum frame rate is limited by how many fps that sensor can output under acceptable maximum pixel clock
  - (*1) In order to keep the same view angle. Higher frame rates are available if not keep the full screen view angle.

2.10 Audio codec

- Support Stereo Sigma Delta ADC
- ADC resolution: 24bit, SNR=100dB
- The adjusted Mic bias: VMID*1.83/2.2/2.38/2.57/3.12/3.3
- Microphone PreAmp:
  - Boost gain -> 0/+20dB/+40dB/50dB

- PGA gain -> -12dB ~ 35.25dB
- Step = 0.75dB

- Mute attenuation : -85dB
- Zero Crossing Update gain
- Anti-aliasing filter
- Support 8/16-bit resolution
- Support stereo 11.025K/ 32K/ 44.1K/ 48KHz sampling rate

2.11 GPIO

- 4 GPIOs are predefined as following functions including LED control, serial flash write protect, sensor LDO and reset/power_down control
- 4 GPIO is reserved for customized application.

2.12 Micro Controller and USB Device Features

- Built-in 8032 micro controller with 6K bytes data memory, and CPU clock rate is up to 120MHz
- Load extended F/W from external serial flash.
- Load VID/PID, manufacturer, product and serial number string from external serial flash.
- Load UVC parameter definition from external serial flash.
- F/W is upgradeable from PC
- Force USB at FS mode / Force USB disconnect
- Watch dog supported

2.13 Pre-Defined for USB Video Class

- Brightness control (UVC defined)
- Contrast control (UVC defined)
- Hue control (UVC defined)
- Saturation control (UVC defined)
- Sharpness control (UVC defined)
- Gamma control (UVC defined)
- White Balance Temperature (UVC defined)
- Backlight Compensation (UVC defined)
- Gain (UVC defined)

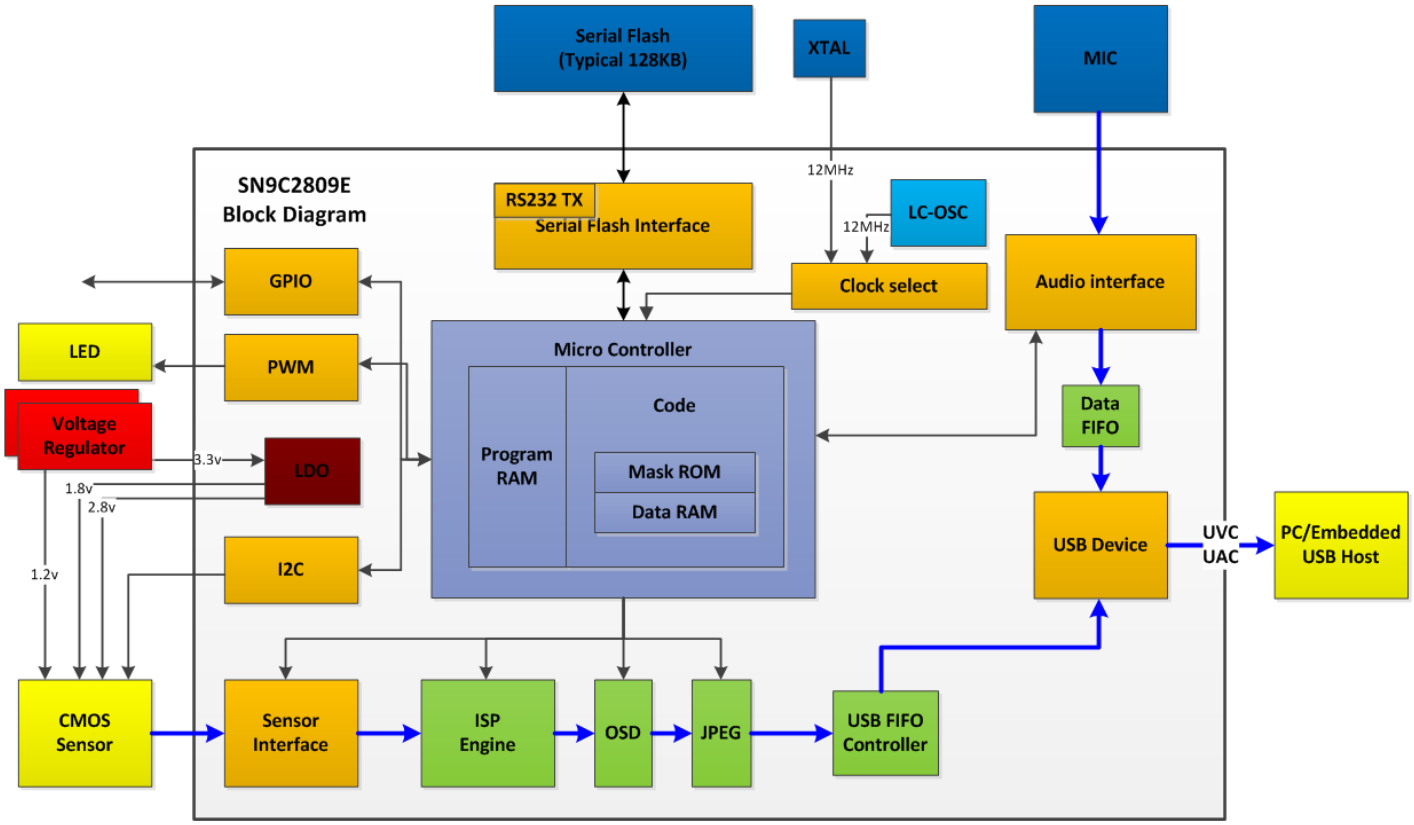
- Power Line Frequency (UVC defined)
- White Balance Temperature, Auto (UVC defined)
- Auto-Exposure Mode (UVC defined)
- Auto-Exposure Priority (UVC defined)
- Exposure Time(Absolute), (UVC defined)
- LED indicator on video streaming
- UVC Extension unit support

2.14 Platform Support

- Microsoft Window 7 32 & 64 bit, Microsoft Window 8/8.1 32 & 64 bit, Microsoft Window 10 32 & 64 bit
- Linux with UVC driver (open source available at http://linux-uvc.berlios.de/)

3 Function Block Diagram

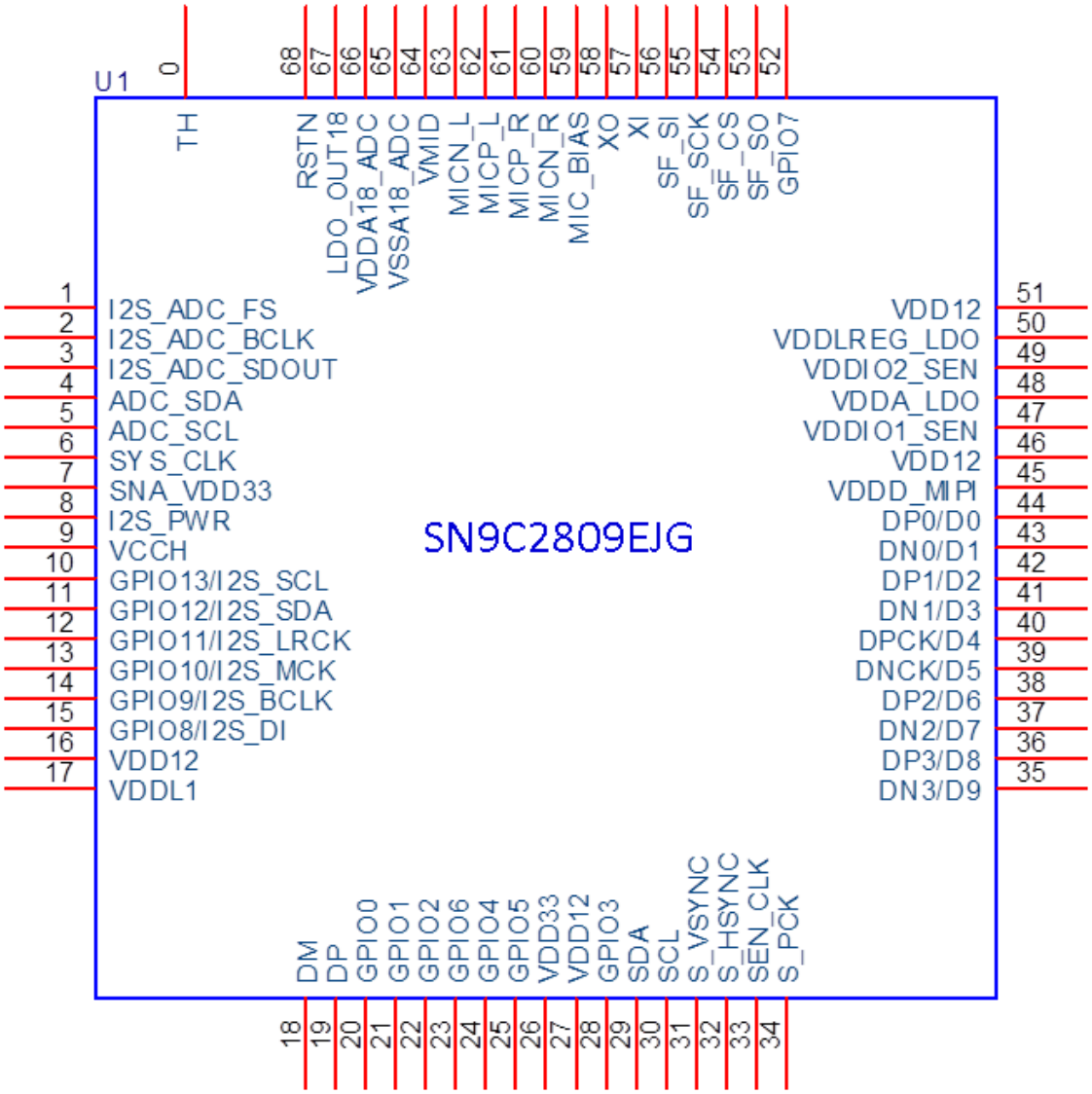
3.1 Block Diagram



4 Pin Assignment

4.1 SN9C2809EJG – 68 pins QFN

4.1.1Pin-out Diagram



4.1.2Pin Description

Pin No.	Pin Name	Description
1	I2S_ADC_FS	I2S_ADC_FS
2	I2S_ADC_BCLK	I2S_ADC_BCLK
3	I2S_ADC_SDOUT	I2S_ADC_SDOUT
4	ADC_SDA	ADC_SDA
5	ADC_SCL	ADC_SCL

6	SYS_CLK	Audio ADC 12Mhz system clock source.
7	SNA_VDD33	Audio codec power.
8	I2S_PWR	I2S power selector. Default 3.3V.
9	VCCH	LC 3.3V & RDL to USB 3.3V for its power supply.
10	I2S_SCL	I2C clock for I2S, or GPIO13
11	I2S_SDA	I2C data for I2S, or GPIO12
12	I2S_LRCK	I2S_LRLK, or GPIO11
13	I2S_MCK	I2S_MCK, GPIO10
14	I2S_BCLK	I2S_BCLK, or GPIO9
15	I2S_DI	I2S_DI, or GPIO8
16	VDD12	DSP core power.
17	VDDL1	USB 1.2V
18	DM	USB D-.
19	DP	USB D+.
20	GPIO0	General purpose I/O. Default for LED control.
21	GPIO1	General purpose I/O. Default for SPI serial flash write protect control.
22	GPIO2	General purpose I/O. Default for sensor LDO enable control.
23	GPIO6	General purpose I/O.
24	GPIO4	General purpose I/O.
25	GPIO5	General purpose I/O.
26	VDD33	DSP system power.
27	VDD12	DSP core power.
28	GPIO3	General purpose I/O. Default is 1.8V power domain and used for sensor power down or reset control.
29	SDA	I2C data for sensor.
30	SCL	I2C clock for sensor.
31	S_VSYNC	Sensor vertical sync.
32	S_HSYNC	Sensor horizontal sync.
33	SEN_CLK	Sensor clock.
34	S_PCK	Sensor pixel clock.
35	DN3 / D9	MIPI sensor data lane 3 negative signal or Parallel D9.
36	DP3 / D8	MIPI sensor data lane 3 positive signal or Parallel D8.
37	DN2 / D7	MIPI sensor data lane 2 negative signal or Parallel D7.
38	DP2 / D6	MIPI sensor data lane 2 positive signal or Parallel D6.
39	DNCK / D5	MIPI sensor clock lane negative signal or Parallel D5.
40	DPCK / D4	MIPI sensor clock lane positive signal or Parallel D4.
41	DN1 / D3	MIPI sensor data lane 1 negative signal or Parallel D3.
42	DP1 / D2	MIPI sensor data lane 1 positive signal or Parallel D2.
43	DN0 / D1	MIPI sensor data lane 0 negative signal or Parallel D1.
44	DP0 / D0	MIPI sensor data lane 0 positive signal or Parallel D0.
45	VDDD_MIPI	MIPI 1.2V.
46	VDD12	DSP core power.
47	VDDIO1_SEN	Internal LDO output for sensor I/O power supply. Default 1.8V.
48	VDDA_LDO	Internal LDO input, 3.3V.
49	VDDIO2_SEN	Internal LDO output for sensor analog power supply. Default 2.8V.
50	VDDLREG_LDO	Internal LDO output for LC & USB & MIPI 1.2V power supply.
51	VDD12	DSP core power.

52	GPIO7	General purpose I/O.
53	SF_SO	SPI data out to serial flash.
54	SF_CS	SPI chip select to serial flash.
55	SF_SCK	SPI clock to serial flash.
56	SF_SI	SPI data in from serial flash.
57	XI	12MHz crystal input.
58	XO	12MHz crystal output.
59	MIC_BIAS	Microphone bias circuit power supply
60	MICN_R	Microphone right channel negative input
61	MICP_R	Microphone right channel positive input.
62	MICP_L	Microphone left channel positive input.
63	MICN_L	Microphone left channel negative input.
64	VMID	ADC VMID pin.
65	VSSA18_ADC	Negative power supply for 1.8V ADC.
66	VDDA18_ADC	Positive power supply for 1.8V ADC.
67	LDO_OUT18	Audio codec LDO output 1.8V.
68	RSTN	Audio codec reset pin.

5 Electrical Characteristics

5.1 DC operating Condition

5.1.1 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Ranges	VDD12	-0.12 ~ 1.32	V
	VDDL1, VDDD_MIPI	-0.12 ~ 1.32	V
	VDDIO_SEN18	-0.3 ~ 3.6	V
	VDD33	-0.3 ~ 3.6	V
	SNA_VDD33	-0.3 ~ 3.6	V
Input Voltage Ranges	Vin	-0.3 ~ VDD33 + 0.3	V
Output Voltage Ranges	Vout	-0.3 ~ VDD33 + 0.3	V
Operating Temperature Ranges	Commercial Ta.	-20 ~ 70	℃
Storage Temperature Ranges	Tstg	-40 ~ 125	℃

5.1.2 Recommended Operating Conditions

System	Parameter	Min	Normal	Max	Unit
VDD12	Power Supply	1.18(*2)	1.25(*2)	1.32	V
VDDL1, VDDD_MIPI	Power Supply	1.18	1.25	1.32	V
VDDIO_SEN18	Power Supply	1.6	1.8	3.6	V
VDD33	Power Supply	3.0	3.3	3.6	V
SNA_VDD33	Power Supply	3.0	3.3	3.6	V
Vin	Input voltage	3.0	3.3	3.6	V
Supply Current Consumed from VDD33 (*1)	Current Supply		45	55	mA
Supply Current Consumed from VDD12	Current Supply		210	230	mA
Suspend Current Consumed from VDD33	Current Supply			500	uA

- (*1) CMOS sensor power consumption is not included)
- (*2) This value to be determined.

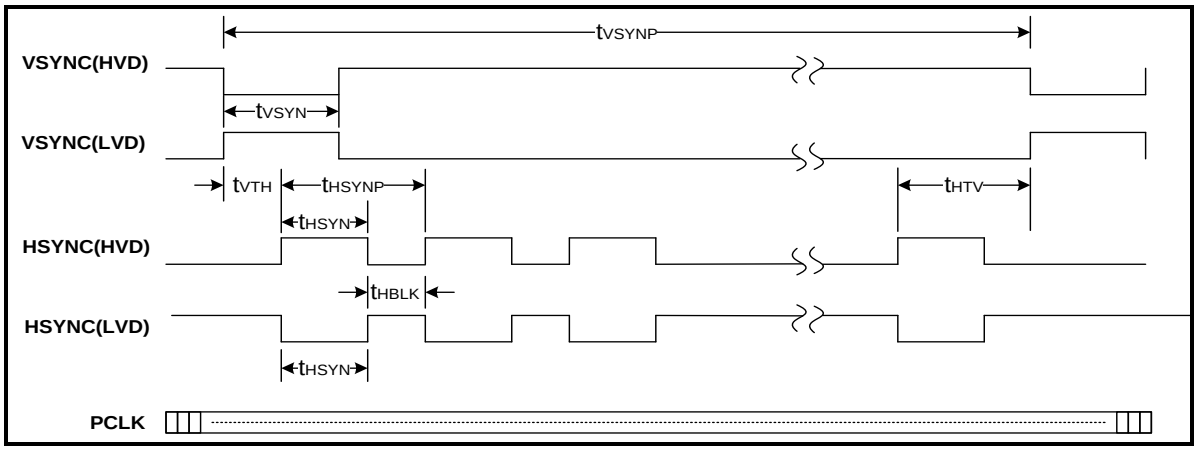
5.1.3 DC Electrical Characteristics

(Under Recommended Operating Conditions and VDD33=3.0 ~ 3.6V, VDDIO_SEN18=1.62 ~ 3.6V, Ta= -20 to +70 °C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vil (VDD33)	Input low voltage	CMOS	-0.3		0.2*VDD33	V
Vih(VDD33)	Input high voltage	CMOS	0.8*VDD33		VDD33+0.3	V
Vil (VDDIO_SEN18)	Input low voltage	CMOS	-0.3		0.2*VDDIO_SEN18	V
Vih(VDDIO_SEN18)	Input high voltage	CMOS	0.8*VDDIO_SEN18		VDDIO_SEN18+0.3	V
Iil	Input low current	no pull-up or pull-down	-1		1	µA
Iih	Input high current	no pull-up or pull-down	-1		1	µA
Ioz	Tri-state leakage current		-1		1	µA
Vol	Output Low voltage	Iol=4mA / 8mA			0.4	V
Voh	Output high voltage	Ioh=4mA / 8mA	2.4			V
Bias voltage	Microphone bias voltage	Vmicbias		VMID*2.56(default) VMID=LDO18/2		V
Bias current source	Microphone bias current	Imicbias		3		mA
Cin	Input capacitance			10		pF
Cout	Output capacitance			10		pF
Cbid	Bi-directional buffer Capacitance			10		pF
Rpu	Pull-up resistor			70K		©
Rpd	Pull-down resistor			70K		©

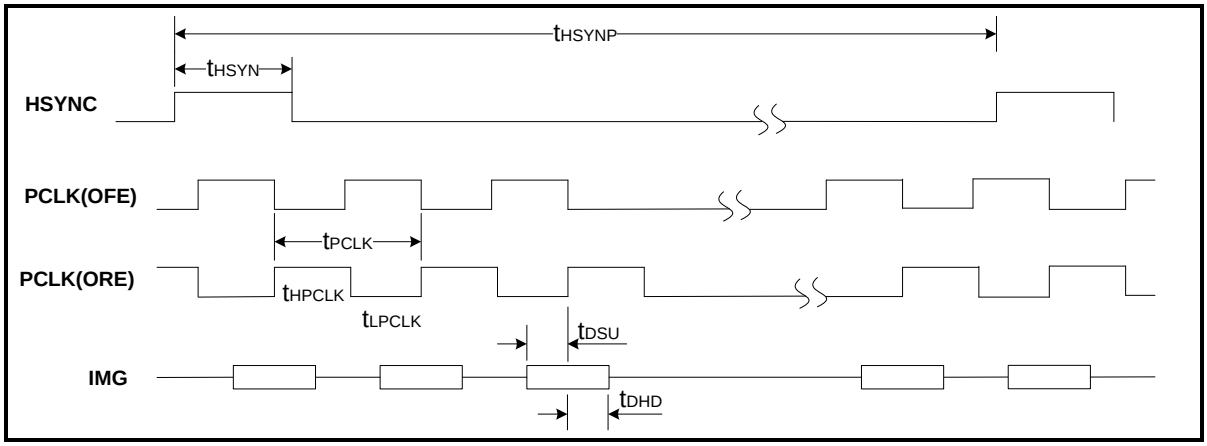
5.2 AC operating Condition

5.2.1Parallel Sensor Interface



Parameter	Symbol	Min.	Typ.	Max.	Unit
VSYNC pulse width	tVSYNC	tPCLK	-	-	ns
VSYNC to HSYNC	tVTH	tPCLK	-	-	ns
HSYNC pulse width	tHSYN	tPCLK	-	-	ns
Blank time between two HSYNC	tHBLK	tPCLK	-	-	ns
HSYNC to VSYNC	tHTV	tHSYNP			ns
Note: tSENCK is period of internal clock for sensor post processing. tHSYNP is period of Hsync, tVSYNP is period of Vsync. HVD (High Valid), LVD (Low Valid).					

- SYNC_MODE = 1: (PCLK is free run)



Parameter	Symbol	Min.	Typ.	Max.	Unit
HSYNC pulse width	tHSYN	tPCLK	-	-	ns
PCLK Low Pulse Width	tLPCLK	2.0	-	-	ns
PCLK High Pulse Width	tHPCLK	2.0	-	-	ns
Frequency of pixel clock	fPCLK	-	-	96	MHz
Image data setup time	tDSU	2.0	-	-	ns
Image data hold time	tDHD	2.0	-	-	ns
Note: tSENCK is period of internal clock for sensor post processing ORE (On Rising Edge) means the timing act on rising edge OFE (On Falling Edge) means the timing act on falling edge					

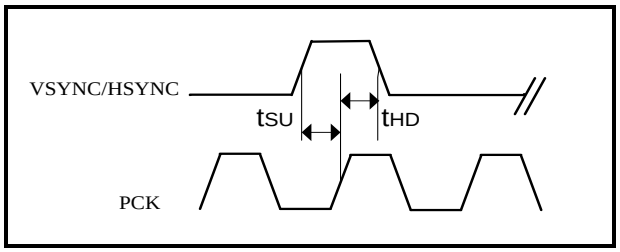
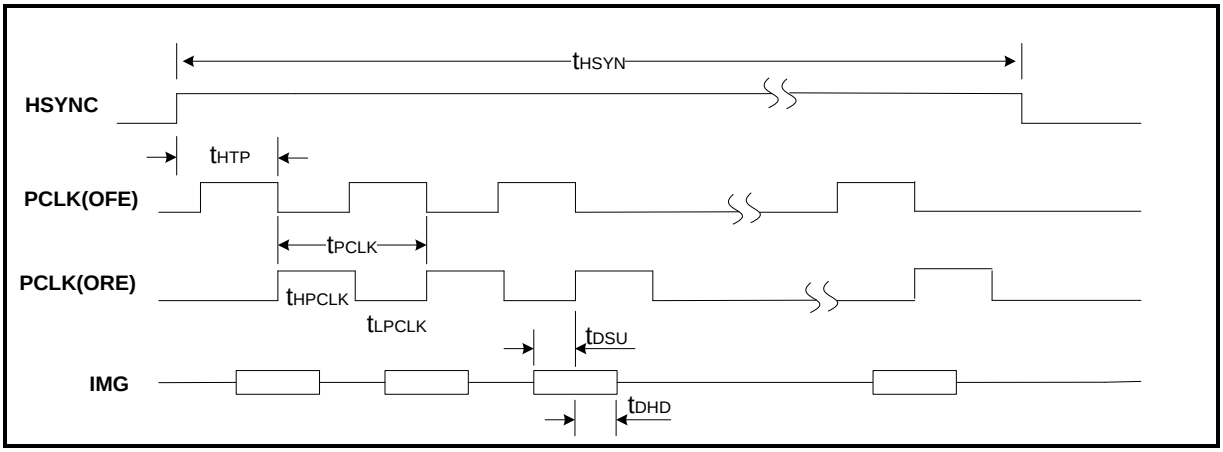


Figure 5.2.1-1 VSYNC/HSYNC setup/hold time

Parameter	Symbol	Min.	Typ.	Max.	Unit
VSYNC / HSYNC setup time	tSU	2	-	-	ns
VSYNC / HSYNC hold time	tHD	2	-	-	ns

■ SYNC_MODE = 0: (PCLK is output only when hsync active)



Parameter	Symbol	Min.	Typ.	Max.	Unit
HSYNC pulse width	tHSYN	HSIZE * tPCLK	-	-	ns
HSYNC to PCLK	tHTP	tSENCK	-	-	
PCLK Low Pulse Width	tLPCLK	2.0	-	-	ns
PCLK High Pulse Width	tHPCLK	2.0	-	-	ns
Frequency of pixel clock	fPCLK	-	-	96	MHz
Image data setup time	tDSU	2.0	-	-	ns
Image data hold time	tDHD	2.0	-	-	ns
Note: tSENCK is period of internal clock for sensor post processing ORE (On Rising Edge) means the timing act on rising edge OFE (On Falling Edge) means the timing act on falling edge HSIZE represents total valid PCLK number per horizontal line					

5.2.2MIPI RX Electrical Characteristics

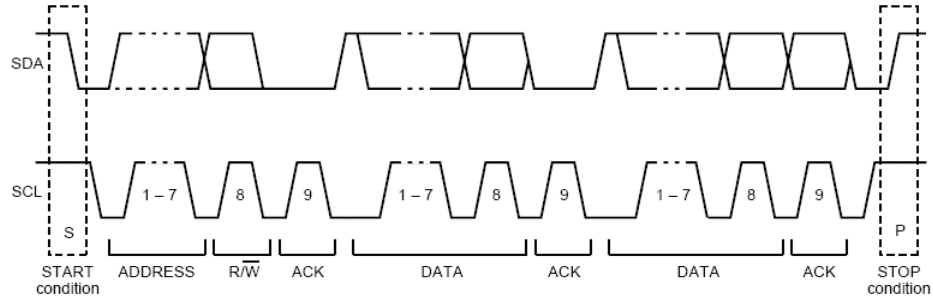
- Low power mode electrical characteristics

Symbol	Parameter	Min	Typ.	Max	Unit
VIH	Logic 1 input voltage	880			mV
VIL	Logic 0 input voltage, not in ULP state			550	mV
VHYST	Input hysteresis	25			mV

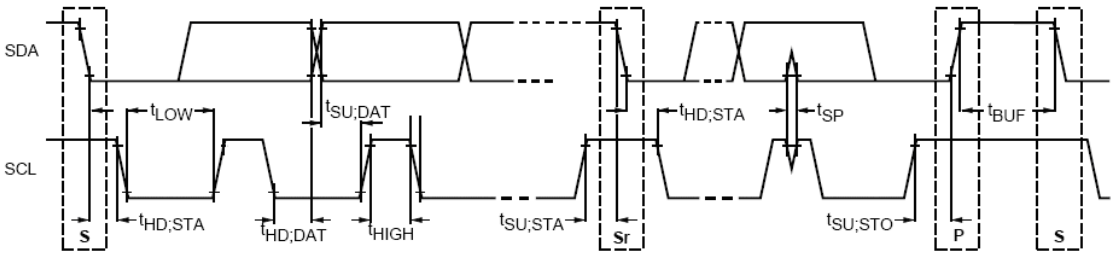
- High speed mode electrical characteristics

Symbol	Parameter	Min	Typ.	Max	Unit
VCMRX(DC)	Common mode voltage		200		mV
VID	Differential input voltage		200		mV
ZID	Differential input impedance	80		125	©

5.2.3 I2C Control Interface



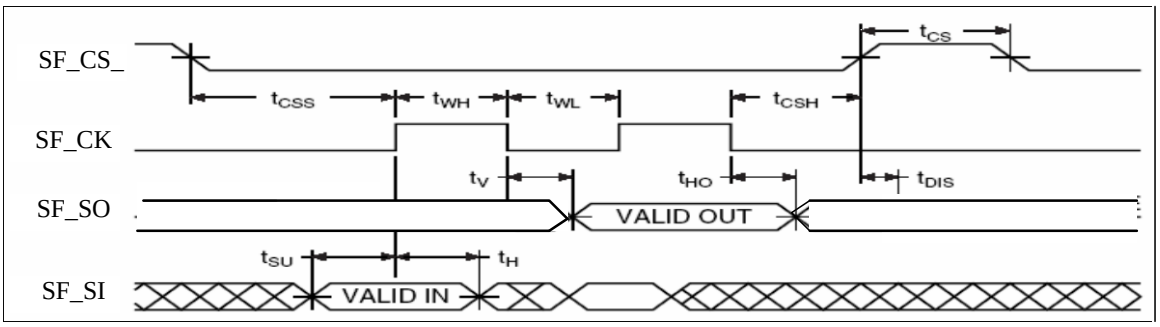
A complete data transfer.



Definition of timing for F/S-mode devices on the I²C-bus.

Parameter	Symbol	Standard mode			Fast mode			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	-	98.7	-	-	394.7	-	kHz
Hold time START condition	$t_{HD;STA}$	-	5067	-	-	1267	-	ns
LOW period of the SCL clock	t_{LOW}	-	5067	-	-	1267	-	ns
HIGH period of the SCL clock	$t_{HD;STA}$	-	5067	-	-	1267	-	ns
Setup time for a repeated START condition	$t_{SU;STA}$	-	5067	-	-	1267	-	ns
Data hold time: Write Data hold time: Read	$t_{HD:DAT}$ $t_{HD:DAT}$	- 35	2533 -	- -	- 35	633 -	- -	ns ns
Data setup time: Write Data setup time: Read	$t_{SU:DAT}$ $t_{SU:DAT}$	- 600	2533 -	- -	- 600	633 -	- -	ns ns
Setup time for STOP condition	$t_{SU:STO}$	-	5066	-	-	1267	-	ns
Bus free time between a STOP and START condition	t_{BUF}	4.8	-	-	1.4	-	-	us

5.2.4 Serial Flash Interface



When f_{SCK} = 60 Mhz

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	-	60	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	136		-	ns
SF_CK Edge to Chip Select High	t_{CSH}	32		-	ns
Chip High period	t_{CS}	120		-	ns
Clock high period	t_{WH}	8	-	-	ns
Clock low period	t_{WL}	8	-	-	ns
Input Data setup time	t_{SU}	6	-	-	ns
Input Data hold time	t_{H}	106	-	-	ns
Output Data Valid time @ CL=20pF	t_{V}	-	-	5	ns
Output Data Hold time @ CL=20pF	t_{HO}	0	-	-	ns

When f_{SCK} = 24 Mhz

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	-	24	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	36		-	ns
SF_CK Edge to Chip Select High	t_{CSH}	36		-	ns
Chip High period	t_{CS}	41.67		-	ns
Clock high period	t_{WH}	20.83	-	-	ns
Clock low period	t_{WL}	20.83	-	-	ns
Input Data setup time	t_{SU}	10	-	-	ns
Input Data hold time	t_{H}	10	-	-	ns
Output Data Valid time @ CL=20pF	t_{V}	-	-	5	ns
Output Data Hold time @ CL=20pF	t_{HO}	36	-	-	ns

5.3 Temperature

5.3.1Storage Temperature

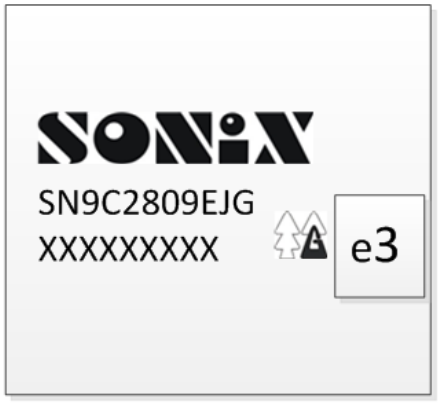
From -40℃ to +125℃

5.3.2Operation Temperature

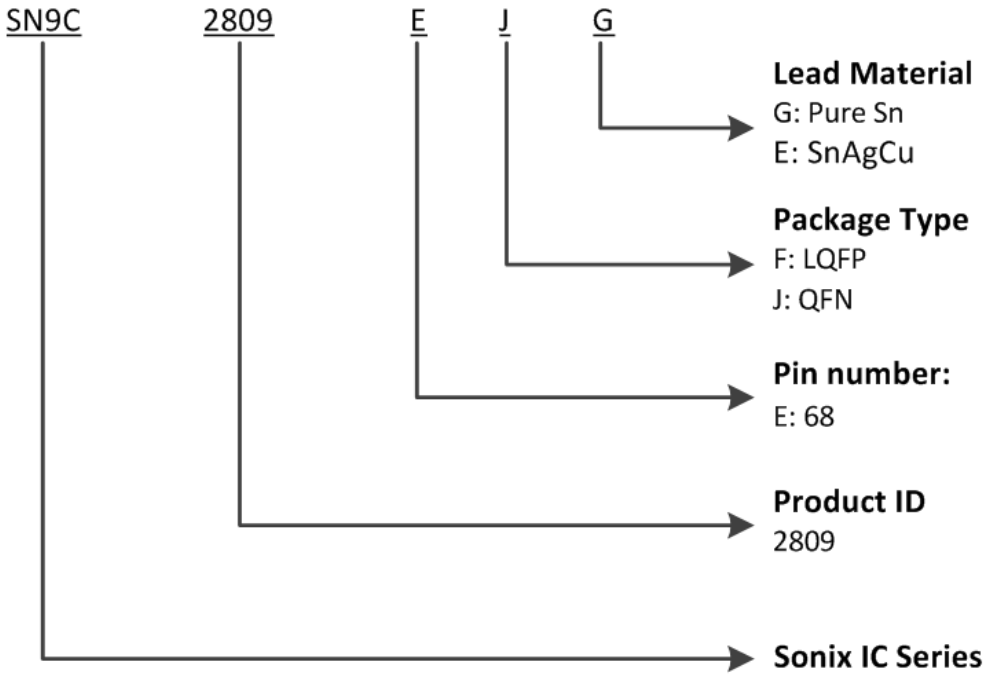
Max. Junction Temp (℃)	Max. Lead Temp.	Ta (℃)	θja (℃/W)
125	+390℃±10℃, 5sec	-20 ~ 70	52.5

6 Package Information

6.1 Nomenclature

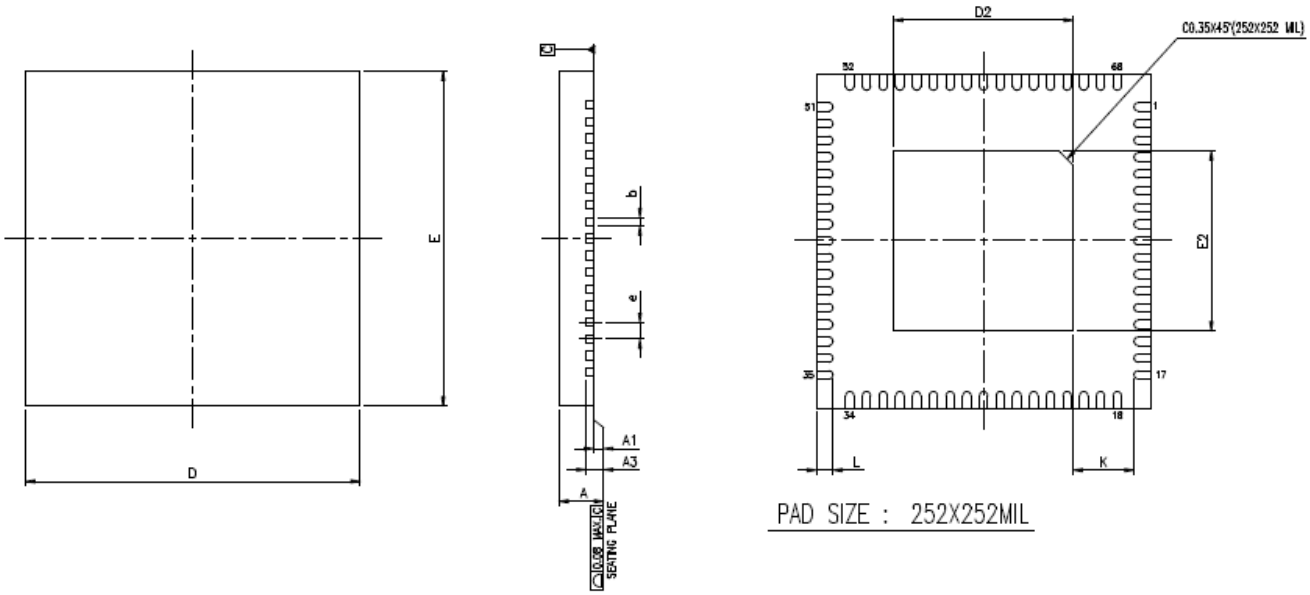


LOGO
Product ID
DATECODE + (SONIX) + e3 (Eco-friendly Products)



6.2 QFN 68 Pins

(8x8x0.8mm / Pitch：0.4)



SYMBOLS	Dimension in mm		
	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.15	0.20	0.25
D	8.00 BSC		
E	8.00 BSC		
e	0.40 BSC		
D2	6.10	6.20	6.30
E2	6.10	6.20	6.30
L	0.35	0.40	0.45
K	0.20	-	-

Notes：

CONTROLLING DIMENSION：MILLIMETER (mm)

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