OmniVision

datasheet

PRODUCT SPECIFICATION

1/2.9" b&w CMOS 2 megapixel (1600 x 1300) image sensor
with OmniPixel®3-GS technology

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OG02B1B

b&w CMOS 2 megapixel (1600 x 1300) image sensor with OmniPixel®3-GS technology

datasheet (CSP)
PRODUCT SPECIFICATION

version 2.02
october 2019

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applications

- augmented and virtual reality
- drones
- 3D imaging
- machine vision
- industrial bar code scanning
- industrial automation

ordering information

- **OG02B1B-A75A** (b&w, lead-free)
  75-pin CSP

features

- 3 µm x 3 µm pixel with OmniPixel®3-GS technology
- automatic black level calibration (ABLC)
- programmable controls for frame rate, mirror and flip, cropping and windowing
- support output formats: 8/10-bit RAW
- fast mode switching
- supports 2x2 monochrome binning
- two-lane MIPI serial output interface
- DVP parallel output interface
- supports horizontal and vertical 2:1 monochrome subsampling
- support for image sizes: 1600 x 1300, 1280 x 720, 640 x 480
- embedded 128 bytes of one-time programmable (OTP) memory
- two on-chip phase lock loops (PLLs)
- LED PWM
- temperature sensor
- built-in strobe control

key specifications (typical)

- **active array size:** 1600 x 1300
- **power supply:**
  analog: 2.8V (nominal)
  core: 1.2V (nominal)
  I/O: 1.8V (nominal)
- **power requirements:**
  active: 190 mW
  XSHUTDOWN: <25 µA
- **temperature range:**
  operating: -30°C to 85°C junction temperature (see **table 8-2**)
  stable image: 0°C to 50°C junction temperature (see **table 8-2**)
- **output interface:** 2-lane MIPI serial output and DVP parallel output
- **output formats:** 10-bit RAW
- **lens size:** 1/2.9"
- **input clock frequency:** 6~27 MHz
- **lens chief ray angle:** 15° linear
- **max S/N ratio:** 37.4 dB
- **dynamic range:** 68 dB
- **maximum image transfer rate:**
  1600 x 1300: 60 fps
- **sensitivity:**
  114Ke$^-$/(µW.cm^{-2}.sec) @ 850 nm
  54Ke$^-$/(µW.cm^{-2}.sec) @ 940 nm
- **minimum exposure time:** 1 row period
- **maximum exposure time:** frame length - 12 row periods, where frame length is set by registers {0x380E, 0x380F}
- **pixel size:** 3 µm x 3 µm
- **image area:** 4857.696 µm x 3955.896 µm
- **package dimensions:** 7219 µm x 6157 µm (see **section 9** for details)

note Maximum integration time of dark current depends on read out speed (e.g., for 60 fps, max dark current is around 1e$^-$ at 50°C).

note OmniVision recommends CSP packages use underfill as a part of camera assembly process.

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1 application system

1.1 overview

The OG02B1B image sensor is a low voltage, high performance, 1/2.9-inch, monochrome, CMOS, image sensor that provides the functionality of a 2 megapixel (1600x1300) camera using OmniPixel®3-GS technology. The OG02B1B provides full-frame, sub-sampled, cropped, or windowed 8/10-bit images via the control of the Serial Camera Control Bus (SCCB) interface.

The OG02B1B has an image array capable of operating at up to 60 frames per second (fps) in 10-bit, 2 megapixel resolution with complete user control over image quality, formatting, and output data transfer.

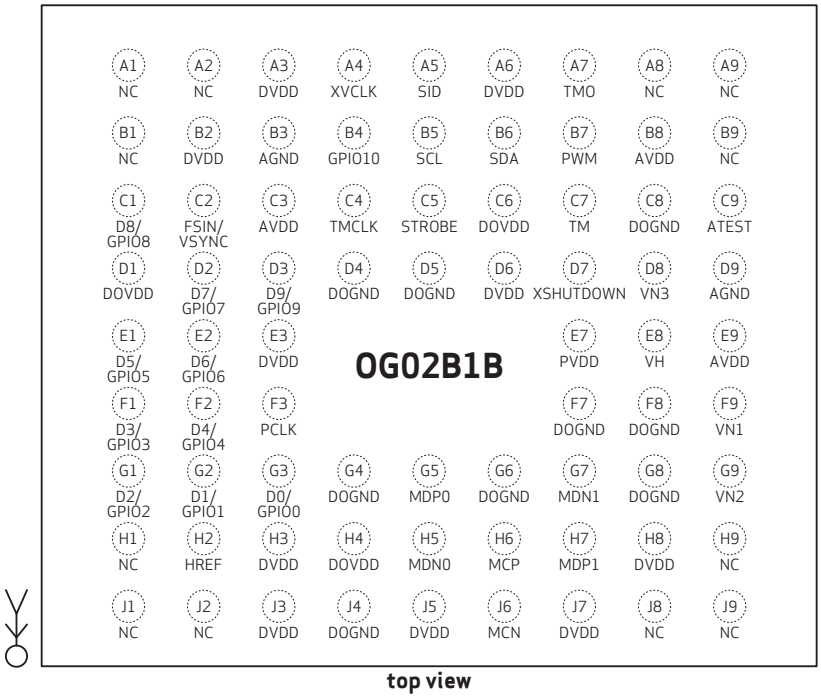
In addition, OmniVision image sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable image.

For customized information purposes, the OG02B1B includes 128 bytes of one-time programmable (OTP) memory. The OG02B1B has a one/two-lane MIPI interface and parallel DVP interface.

1.2 signal description and pin assignment

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OG02B1B image sensor. The package information is shown in **section 9**.

figure 1-1 pin diagram



top view

table 1-1 signal descriptions (sheet 1 of 4)

pin number	signal name	pin type	description
A1	NC	–	no connect
A2	NC	–	no connect
A3	DVDD	power	power for digital circuit
A4	**XVCLK**	input	system input clock
A5	**SID**	input	chip ID selection
A6	DVDD	power	power for digital circuit
A7	**TMO**	output	test mode output

table 1-1 signal descriptions (sheet 2 of 4)

pin number	signal name	pin type	description
A8	NC	–	no connect
A9	NC	–	no connect
B1	NC	–	no connect
B2	DVDD	power	power for digital circuit
B3	AGND	ground	ground for analog circuit
B4	**GPIO10**	I/O	general purpose I/O 10
B5	**SCL**	input	SCCB input clock
B6	**SDA**	I/O	SCCB data
B7	**PWM**	I/O	PWM output
B8	AVDD	power	power for analog circuit
B9	NC	–	no connect
C1	**D8/GPIO8**	I/O	DVP output data 8 / general purpose I/O 8
C2	**FSIN/VSYNC**	I/O	frame sync input / vertical sync output
C3	AVDD	power	power for analog circuit
C4	**TMCLK**	input	test mode clock
C5	**STROBE**	I/O	strobe output
C6	DOVDD	power	power for I/O circuit
C7	**TM**	input	test mode (active high with internal pull down resistor)
C8	DOGND	ground	ground for I/O
C9	ATEST	reference	analog test
D1	DOVDD	power	power for I/O circuit
D2	**D7/GPIO7**	I/O	DVP output data 7 / general purpose I/O 7
D3	**D9/GPIO9**	I/O	DVP output data 9 / general purpose I/O 9
D4	DOGND	ground	ground for I/O
D5	DOGND	ground	ground for I/O
D6	DVDD	power	power for digital circuit
D7	**XSHUTDOWN**	input	reset and power down (active low)
D8	VN3	reference	internal analog reference
D9	AGND	ground	ground for analog circuit
E1	**D5/GPIO5**	I/O	DVP output data 5 / general purpose I/O 5

table 1-1 signal descriptions (sheet 3 of 4)

pin number	signal name	pin type	description
E2	**D6/GPIO6**	I/O	DVP output data 6 / general purpose I/O 6
E3	DVDD	power	power for digital circuit
E7	PVDD	power	power for PLL
E8	VH	reference	internal analog reference
E9	AVDD	power	power for analog circuit
F1	**D3/GPIO3**	I/O	DVP output data 3 / general purpose I/O 3
F2	**D4/GPIO4**	I/O	DVP output data 4 / general purpose I/O 4
F3	**PCLK**	I/O	DVP output clock
F7	DOGND	ground	ground for I/O
F8	DOGND	ground	ground for I/O
F9	VN1	reference	internal analog reference
G1	**D2/GPIO2**	I/O	DVP output data 2 / general purpose I/O 2
G2	**D1/GPIO1**	I/O	DVP output data 1 / general purpose I/O 1
G3	**D0/GPIO0**	I/O	DVP output data 0 / general purpose I/O 0
G4	DOGND	ground	ground for I/O
G5	**MDP0**	output	MIPI TX data lane 0 positive output
G6	DOGND	ground	ground for I/O
G7	**MDN1**	output	MIPI TX data lane 1 negative output
G8	DOGND	ground	ground for I/O
G9	VN2	reference	internal analog reference
H1	NC	–	no connect
H2	**HREF**	I/O	DVP HREF output
H3	DVDD	power	power for digital circuit
H4	DOVDD	power	power for I/O circuit
H5	**MDN0**	output	MIPI TX data lane 0 negative output
H6	**MCP**	output	MIPI TX clock lane positive output
H7	**MDP1**	output	MIPI TX data lane 1 positive output
H8	DVDD	power	power for digital circuit
H9	NC	–	no connect
J1	NC	–	no connect

table 1-1 signal descriptions (sheet 4 of 4)

pin number	signal name	pin type	description
J2	NC	–	no connect
J3	DVDD	power	power for digital circuit
J4	DOGND	ground	ground for I/O
J5	DVDD	power	power for digital circuit
J6	**MCN**	output	MIPI TX clock lane negative output
J7	DVDD	power	power for digital circuit
J8	NC	–	no connect
J9	NC	–	no connect

table 1-2 configuration under various conditions (sheet 1 of 2)

pin number	signal name	XSHUTDOWN[a]	after XSHUTDOWN release[b]	software standby[c]
A4	XVCLK	input	input	input
A5	SID	input	input	input
A7	TMO	high-z	output	output by default
B4	GPIO10	high-z	high-z by default	high-z by default (configurable)
B5	SCL	input	input	input
B6	SDA	high-z	input/open drain	input/open drain
B7	PWM	high-z	output	output by default (configurable)
C1	D8/GPIO8	high-z	high-z by default	high-z by default (configurable)
C2	FSIN/VSYNC	high-z	high-z by default	high-z by default (configurable)
C4	TMCLK	input	input	input
C5	STROBE	high-z	high-z by default	high-z by default (configurable)
C7	TM	input	input	input
D2	D7/GPIO7	high-z	high-z by default	high-z by default (configurable)

table 1-2 configuration under various conditions (sheet 2 of 2)

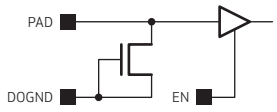
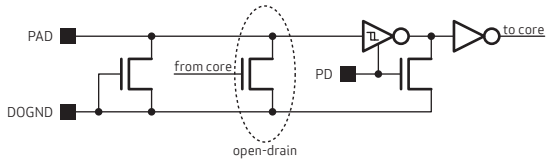
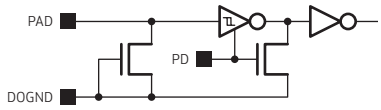
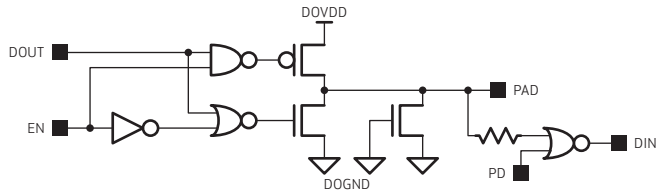
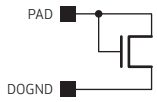
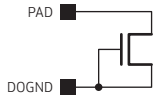
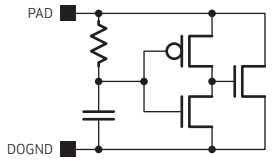
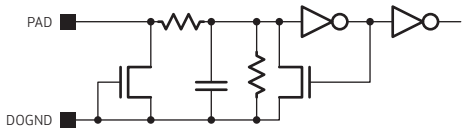
pin number	signal name	XSHUTDOWN[a]	after XSHUTDOWN release[b]	software standby[c]
D3	D9/GPIO9	high-z	high-z by default	high-z by default (configurable)
D7	XSHUTDOWN	input	input	input
E1	D5/GPIO5	high-z	high-z by default	high-z by default (configurable)
E2	D6/GPIO6	high-z	high-z by default	high-z by default (configurable)
F1	D3/GPIO3	high-z	high-z by default	high-z by default (configurable)
F2	D4/GPIO4	high-z	high-z by default	high-z by default (configurable)
F3	PCLK	high-z	high-z by default	high-z by default (configurable)
G1	D2/GPIO2	high-z	high-z by default	high-z by default (configurable)
G2	D1/GPIO1	high-z	high-z by default	high-z by default (configurable)
G3	D0/GPIO0	high-z	high-z by default	high-z by default (configurable)
G5	MDP0	high-z	high by default	high by default (configurable)
G7	MDN1	high-z	high by default	high by default (configurable)
H2	HREF	high-z	high-z by default	high-z by default (configurable)
H5	MDN0	high-z	high by default	high by default (configurable)
H6	MCP	high-z	high by default	high by default (configurable)
H7	MDP1	high-z	high by default	high by default (configurable)
J6	MCN	high-z	high by default	high by default (configurable)

a. XSHUTDOWN = 0

b. XSHUTDOWN = 1

c. XSHUTDOWN = 1, standby initiated by register

table 1-3 pad symbol and equivalent circuit

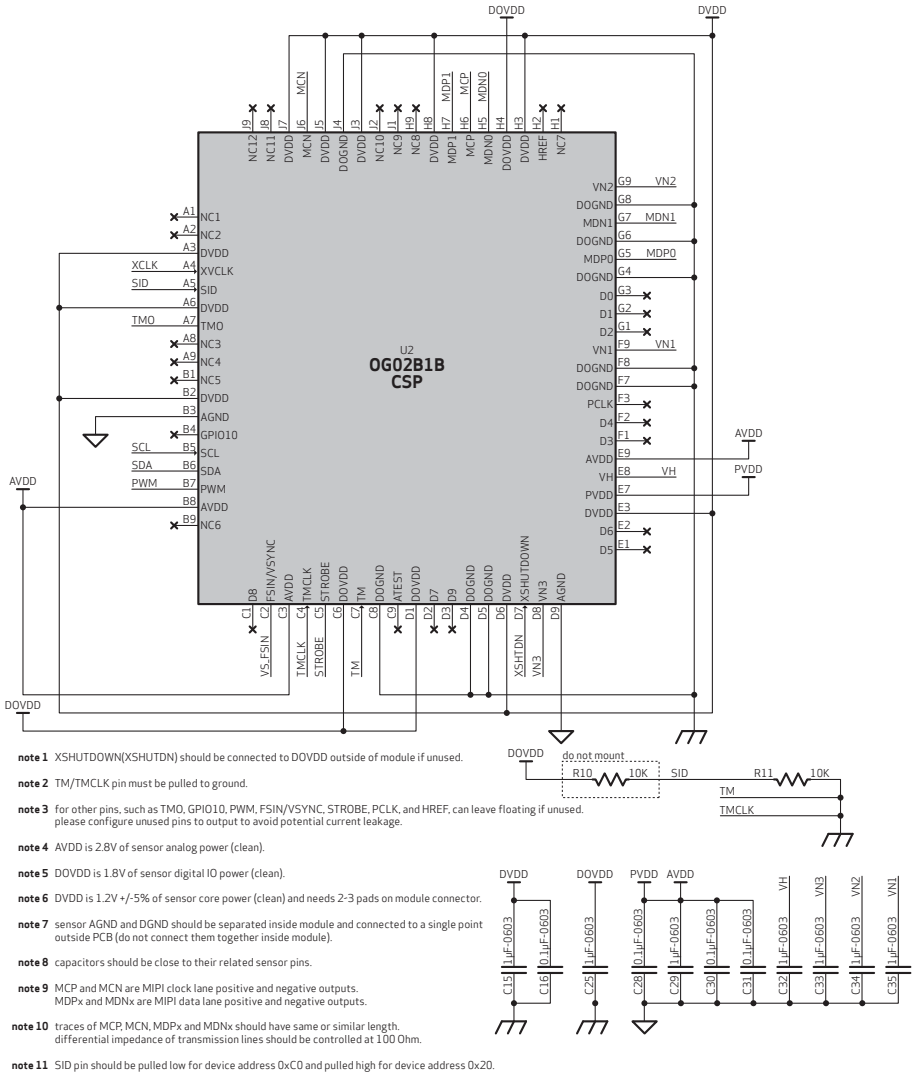
symbol	equivalent circuit
XVCLK, TMCLK	
SDA, TMO	
SCL	
FSIN/VSYNC, STROBE, PWM, D/GPIO[9:0], GPIO10, PCLK, HREF	
VN1, VN2, VN3	
MDP0, MDN0, MDP1, MDN1, MCP, MCN, AGND, DOGND, VH	
AVDD, DVDD, DOVDD, PVDD	
TM, XSHUTDOWN, SID	

1.3 reference design

figure 1-2 shows the power supply and signal connection of the OG02B1B when using MIPI interface. The SCCB ID is defined by the voltage level of the SID pin at power up and after hardware reset (XSHUTDOWN pin low). When the SID pin is pulled down, the SCCB ID is "C0" by default, or defined by register 0x0109. When it is pulled high, the SCCB ID is 0x20 or defined by register 0x0107.

Analog supply is 2.8V. I/O pad power (DOVDD) is 1.8V. Core logic operates on 1.2V (DVDD). The OG02B1B must use external power de-coupling capacitors to reduce noise. The recommended capacitance is 1µF. At power up, the power supplies should ramp up in 50 µs or more to avoid in-rush current during ramp-up.

figure 1-2 OG02B1B MIPI reference design schematic



note 1 XSHUTDOWN(XSHUTDN) should be connected to DOVDD outside of module if unused.

note 2 TM/TMCLK pin must be pulled to ground.

note 3 for other pins, such as TMO, GPIO10, PWM, FSIN/VSYNC, STROBE, PCLK, and HREF, can leave floating if unused. please configure unused pins to output to avoid potential current leakage.

note 4 AVDD is 2.8V of sensor analog power (clean).

note 5 DOVDD is 1.8V of sensor digital IO power (clean).

note 6 DVDD is 1.2V +/-5% of sensor core power (clean) and needs 2-3 pads on module connector.

note 7 sensor AGND and DGND should be separated inside module and connected to a single point outside PCB (do not connect them together inside module).

note 8 capacitors should be close to their related sensor pins.

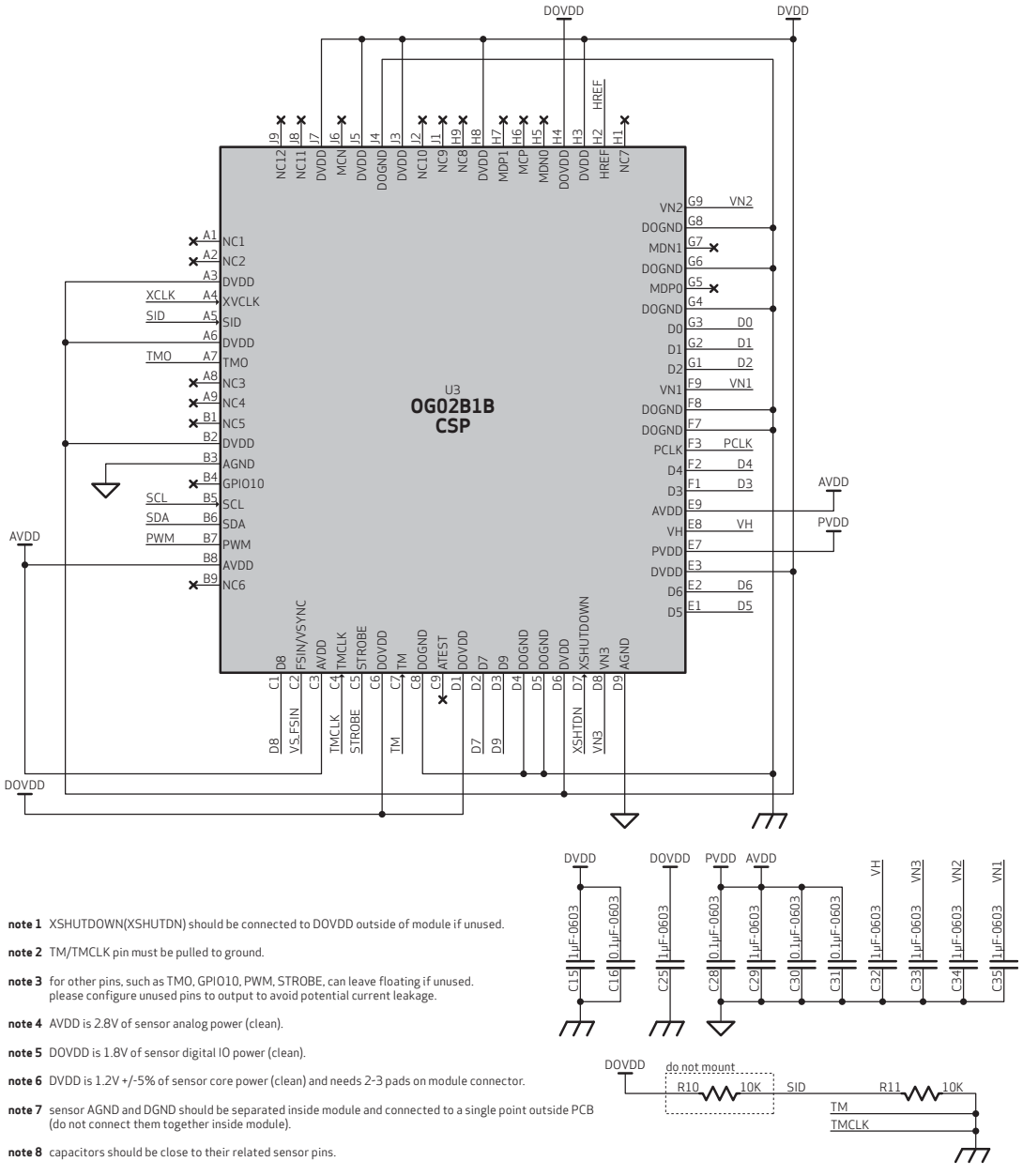
note 9 MCP and MCN are MIPI clock lane positive and negative outputs. MDPx and MDNx are MIPI data lane positive and negative outputs.

note 10 traces of MCP, MCN, MDPx and MDNx should have same or similar length. differential impedance of transmission lines should be controlled at 100 Ohm.

note 11 SID pin should be pulled low for device address 0xC0 and pulled high for device address 0x20.

figure 1-3 shows the power supply signal connections of the OG02B1B when using the DVP interface.

figure 1-3 OG02B1B DVP reference design schematic



note 1 XSHUTDOWN(XSHUTDN) should be connected to DOVDD outside of module if unused.

note 2 TM/TMCLK pin must be pulled to ground.

note 3 for other pins, such as TMO, GPIO10, PWM, STROBE, can leave floating if unused. please configure unused pins to output to avoid potential current leakage.

note 4 AVDD is 2.8V of sensor analog power (clean).

note 5 DOVDD is 1.8V of sensor digital IO power (clean).

note 6 DVDD is 1.2V +/-5% of sensor core power (clean) and needs 2-3 pads on module connector.

note 7 sensor AGND and DGND should be separated inside module and connected to a single point outside PCB (do not connect them together inside module).

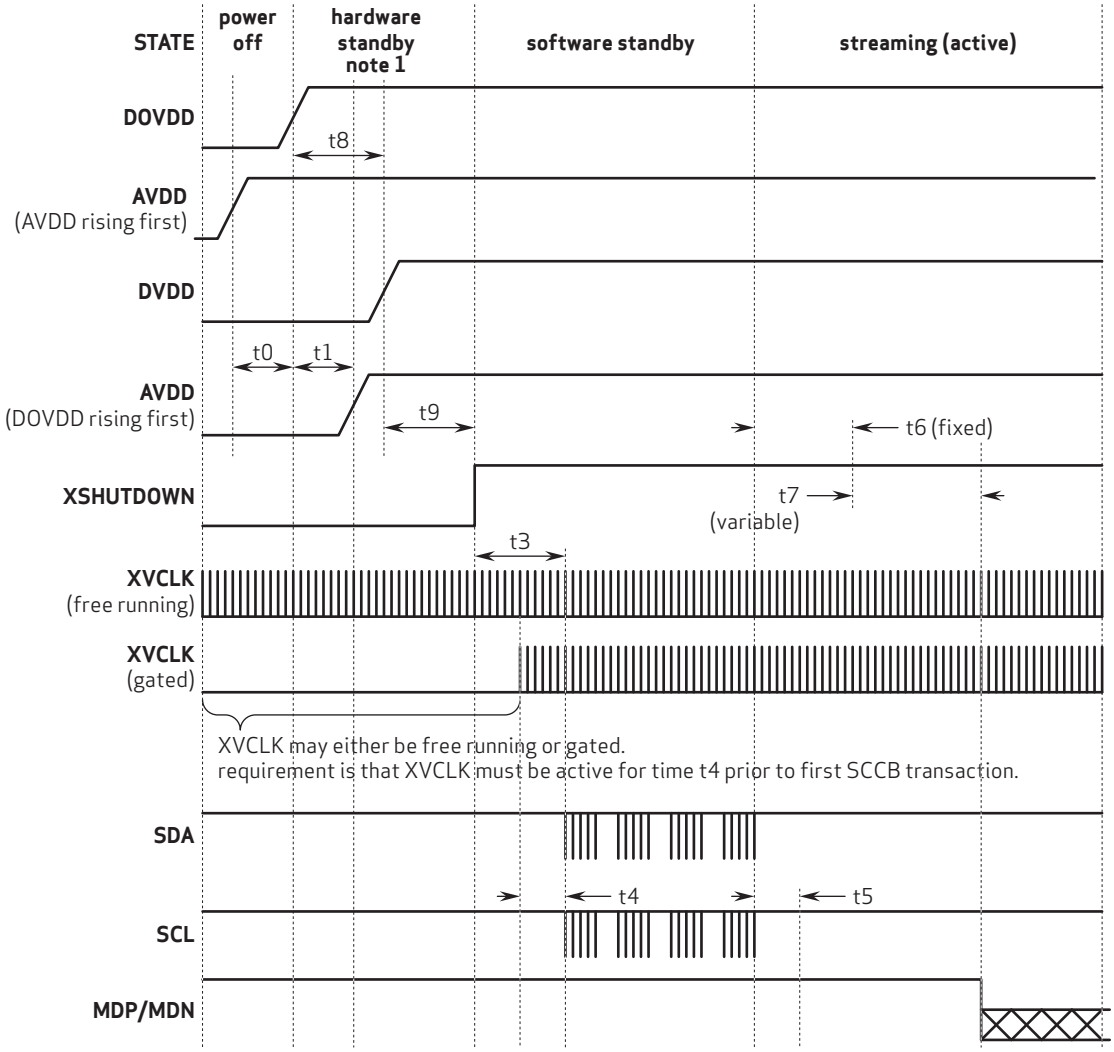
note 8 capacitors should be close to their related sensor pins.

note 9 SID pin should be pulled low for device address 0xC0 and pulled high for device address 0x20.

1.4 power management

1.4.1 power up sequence

figure 1-4 power up sequence



note 1 with low power consumption

table 1-4 power up sequence timing constraints

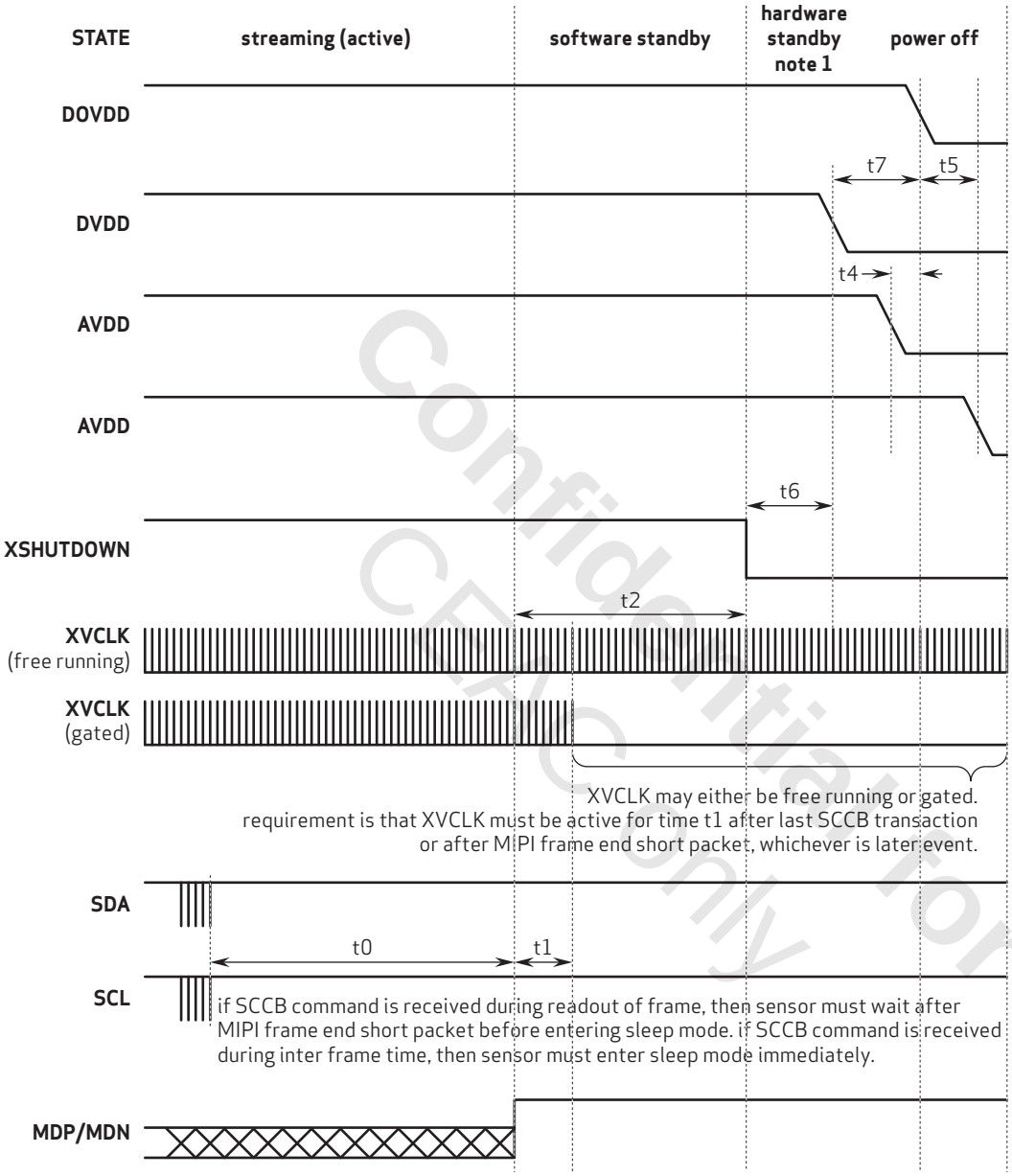
constraint	label	min	max	unit
AVDD rising – DOVDD rising	t0	0	∞	ms
DOVDD rising – AVDD rising	t1			ms
AVDD or DOVDD rising, whichever is last – XSHUTDOWN rising	t2	1		ms
XSHUTDOWN rising – first SCCB transaction	t3	65536		XVCLK cycles
minimum number of XVCLK cycles prior to first SCCB transaction	t4	65536		XVCLK cycles
PLL start up/lock time	t5		0.2	ms
entering streaming mode – first frame start sequence (fixed part)	t6	16388		XVCLK cycles
entering streaming mode – first frame start sequence (variable part)	t7	delay is exposure time value		row period
DOVDD to external DVD rising	t8	0		ms
DOVDD rising to XSHUTDOWN rising	t9	0		ms

1.4.2 power down sequence

The digital and analog supply voltages can be powered down in any order (e.g., DOVDD, then AVDD or AVDD, then DOVDD). Similar to the power-up sequence, the XVCLK input clock may be either gated or continuous. If the SCCB command to exit streaming is received while a frame of MIPI data is being output, then the sensor must wait to the MIPI frame end code before entering software standby mode.

If the SCCB command to exit streaming mode is received during the inter frame time, then the sensor will enter software standby mode immediately.

figure 1-5 power down sequence



note 1 with low power consumption

table 1-5 power down sequence timing constraints

constraint	label	min	max	unit
enter software standby SCCB command device in software standby mode	t0	when a frame of MIPI data is output, wait for MIPI end code before entering software for standby; otherwise, enter software standby mode immediately		
minimum of XVCLK cycles after last SCCB transaction or MIPI frame end	t1	512		XVCLK cycles
last SCCB transaction or MIPI frame end, XSHUTDOWN falling	t2	512		XVCLK cycles
XSHUTDOWN falling - AVDD falling or DOVDD falling whichever is first	t3	0.0		ms
AVDD falling - DOVDD falling	t4	AVDD and DOVDD may fall in any order, falling separation can vary from 0 ns to infinity		ms
DOVDD falling - AVDD falling	t5			ms
XSHUTDOWN falling - DVDD falling	t6	0		ms
DVDD falling to DOVDD falling	t7	0		ms

1.5 reset

The OG02B1B sensor includes a XSHUTDOWN pin (pin **D7**) that forces a complete hardware reset when it is pulled low (GND). The OG02B1B clears all registers and resets them to their default values when a hardware reset occurs.

1.5.1 power ON reset generation

The OG02B1B has a power on reset that is generated after the core power becomes stable.

1.6 hardware and software standby

Two suspend modes are available for the OG02B1B:

- hardware standby – dropping any power source (AVDD/DOVDD/DVDD) or if XSHUTDOWN pin is tied to low, will initiate hardware standby mode
- software standby – executing a software power down (register bit 0x0100[0]) through the SCCB interface suspends internal circuit activity, but does not halt the device clock. All register content is maintained in standby mode.

figure 1-6 standby sequence

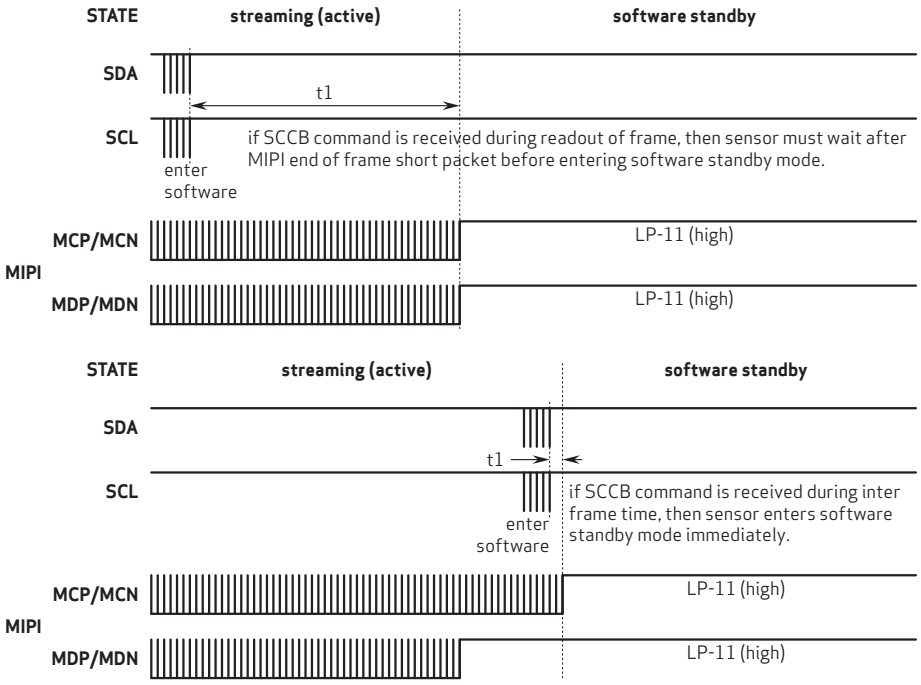


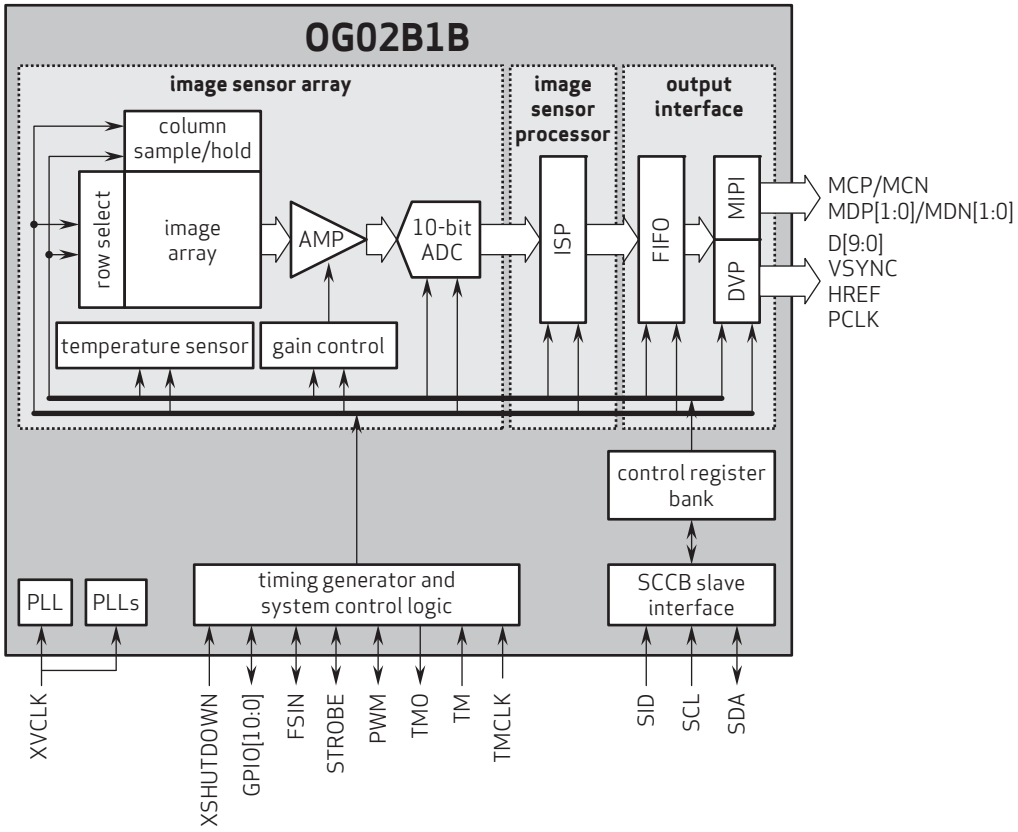
table 1-6 hardware and software standby description

mode	description
hardware standby with XSHUTDOWN	1. enabled by pulling XSHUTDOWN pad low 2. power down all blocks 3. register values are reset to default values 4. no SCCB communication 5. minimum power consumption
software standby	1. default mode after power on reset 2. power down all blocks except SCCB 3. register values are maintained 4. SCCB communication is available 5. low power consumption 6. GPIO can be configured as high/low/tri-state

2 sensor architecture

figure 2-1 shows the top level block diagram of the OG02B1B sensor.

figure 2-1 OG02B1B block diagram



The image sensor core generates streaming pixel data at a constant frame rate.The timing generator outputs signals to access the image array. The entire pixel array is reset at the same point of time. After the exposure time has elapsed, the pixels stop gathering light and store the collected charge in a storage node. The charge then reads out row by row. During readout, the accumulated charge is converted to a voltage signal in the pixel. This signal is then amplified and converted to a digital signal by the analog-to-digital converter (ADC). Dark current and circuit offsets are compensated by the black level correction circuit (BLC). The correction is implemented purely in the digital domain. Dark current increases exponentially with temperature and the BLC can be configured to automatically re-trigger with changes in junction temperature, in addition to changes in gain. A temperature sensor is integrated in the image sensor core.

The image is formatted and output through the digital video port (DVP) interface or the MIPI interface. Two on-chip phase lock loops (PLLs) generate the required clock signals for all blocks from the XVCLK input clock. The timing generator generates the control signals for the pixel array to reset the PD at the beginning of the exposure, to stop the exposure

by reading out the accumulated charge, and also to generate the required control timing for the readout amplifier and ADC. In DVP mode, the horizontal synchronization reference (HREF), vertical synchronization (VSYNC), and pixel clock (PCLK) signals are also generated so the backend processor can receive the image data.

All functional blocks are controlled by registers. The host controller can program and read back through the SCCB interface.

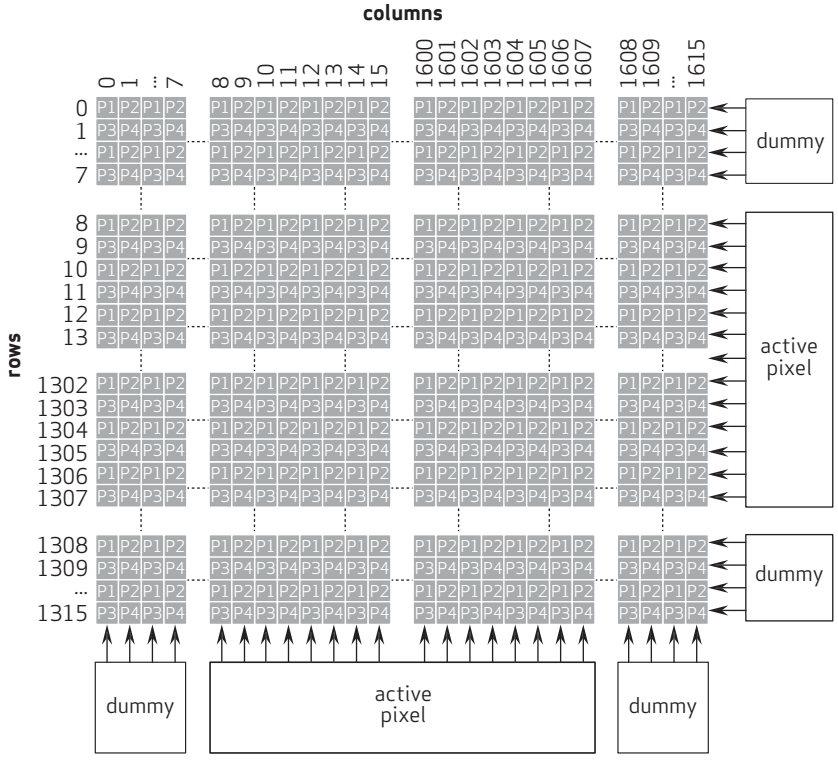
3 image sensor core

3.1 pixel array structure

The OG02B1B sensor has an image array of 1616 columns by 1316 rows (2,126,656 pixels). **figure 3-1** shows a cross-section of the image sensor array.

Of the 2,126,656 pixels, 2,080,000 (1600x1300) are active pixels and can be output. The other pixels are used for black level calibration and interpolation.

figure 3-1 sensor array layout



3.2 subsampling

There are two subsampling modes in the OG02B1B: binning and skipping. Both are acceptable methods of reducing output resolution while maintaining the field of view. Binning is usually preferred as it increases the pixel's signal-to-noise ratio. When the binning function is ON, voltage levels of a pair of the same pixels (e.g., P1 and P1 pixels, or P2 and P2 pixels) are averaged. In skipping mode (binning function is OFF), alternate pixels, which are not output, are merely skipped. The OG02B1B supports 2x2 binning. **figure 3-2** illustrates 2x2 binning, where the voltage levels of two horizontal (2x1) pixels, which are the same, such as P3 and P3 pixels are averaged.

figure 3-2 example of 2x2 binning

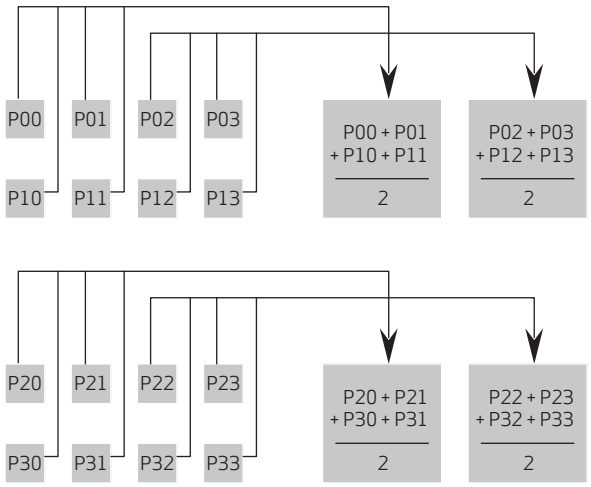


figure 3-3 example of 2:1 skipping

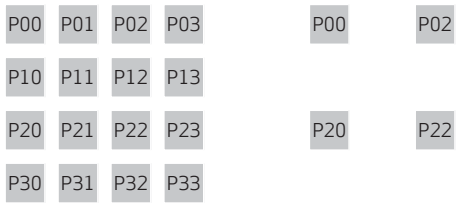


figure 3-4 example of 4:1 skipping

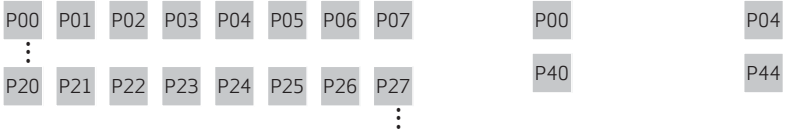


table 3-1 binning-related registers

address	register name	default value	R/W	description
0x3814	TIMING_X_INC	0x11	RW	Bit[7:4]: x_odd_inc Bit[3:0]: x_even_inc
0x3815	TIMING_Y_INC	0x11	RW	Bit[7:4]: y_odd_inc Bit[3:0]: y_even_inc
0x3820	TIMING_FORMAT1	0x00	RW	Bit[1]: Vertical binning
0x3821	TIMING_FORMAT2	0x00	RW	Bit[0]: Horizontal binning

3.3 manual exposure and gain control

Exposure time control is set by registers {0x3501, 0x3502}. Maximum exposure time is frame length - 12 row periods, where frame length is set by registers {0x380E, 0x380F}. Minimum exposure time is 1 row period.

Analog gain control is set by registers {0x3508, 0x3509}. 1x analog gain is set by setting register 0x3508=0x01 and register 0x3509=0x00.

Digital gain control is set by registers {0x350A, 0x350B, 0x350C}. 1x digital gain is set by setting register 0x350A=0x01, register 0x350B=0x00, and register 0x350C=0x00.

The OG02B1B also supports sub row exposure control, which is when the setting needs to change between sub row exposure and normal exposure. Use registers {0x3506, 0x3507} to control the sub row exposure. The range is 0~HTS-0x10.

```
@@ Sub Row Exposure
C0 3501 00
C0 3502 00
C0 3506 00
C0 3507 00;[0,HTS - 0x10]
C0 379B 00
C0 382C 0A
C0 382D 98
C0 3882 04
C0 3883 EB
C0 38A6 01
C0 38A7 86

@@ Back to normal
C0 3501 05
C0 3502 B6
C0 3506 00
C0 3507 00
C0 379B 01
C0 382C 0A
C0 382D 98
```

```
C0 3882 02

C0 3883 6C

C0 38A6 00

C0 38A7 01
```

table 3-2 manual exposure and gain control registers

address	register name	default value	R/W	description
0x3501	EXPO	0x05	RW	Bit[7:0]: Exposure[15:8]
0x3502	EXPO	0xA0	RW	Bit[7:0]: Exposure[7:0]
0x3503	AEC MANUAL	0xA8	RW	Bit[6]: Digital gain delay option 0: Delay 2 frames 1: Delay 1 frame Bit[4]: Gain delay option 0: Delay 2 frames 1: Delay 1 frame
0x3506	EXPO FINE	0x00	RW	Bit[7:0]: Fine exposure[15:8]
0x3507	EXPO FINE	0x00	RW	Bit[7:0]: Fine exposure[7:0]
0x3508	GAIN COARSE	0x01	RW	Bit[4:0]: Coarse real gain
0x3509	GAIN FINE	0x00	RW	Bit[7:4]: Fine real gain
0x350A	DIGIGAIN COARSE	0x01	RW	Bit[3:0]: Coarse digital gain
0x350B	DIGIGAIN FINE	0x00	RW	Bit[7:0]: Digital fine gain[9:2] 4.10 format
0x350C	DIGIGAIN FINE	0x00	RW	Bit[7:6]: Digital fine gain[1:0] 4.10 format

3.4 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines. These lines are used as reference for black level calibration.

The black level calibration (BLC) function is used to set the pixel output of a complete black object to a programmable pedestal value in all kinds of lightning conditions. Due to circuit offset and pixel dark current, the pixel output level of a black object is normally non-zero. The OG02B1B calibrates the black level of the active pixel by subtracting the true optical black pixel output.

The target BLC pedestal value is set by registers {0x4002, 0x4003}. The pedestal values are 10-bit values. The ISP will subtract the pedestal value early in the signal processing path.

table 3-3 BLC control functions (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x9F	RW	Bit[0]: BLC enable 0: Disable 1: Enable
0x4000	BLC_CTRL_00	0xCF	RW	Bit[7:4]: r_off_avg_weight_o Bit[3]: r_target_adj_dis_o Bit[2]: r_off_cmp_en_o Bit[1]: r_dither_en_o Bit[0]: r_mf_en_o
0x4001	BLC_CTRL_01	0x20	RW	Bit[7:6]: r_hdr_option_o Bit[5]: r_kcoef_man_en_o Bit[4]: r_off_man_en_o Bit[3]: r_zero_in_out_en_o Bit[2]: r_blk_in_out_en_o Bit[1:0]: r_byp_mode_o
0x4002	BLC_AUTO	0x00	RW	Bit[2:0]: Black target level[10:8]
0x4003	BLC_CTRL_03	0x10	RW	Bit[7:0]: Black target level[7:0]
0x4008	BLC_CTRL_08	0x00	RW	Bit[3:0]: r_up_bl_start_o[3:0]
0x4009	BLC_CTRL_09	0x07	RW	Bit[3:0]: r_up_bl_end_o[3:0]
0x400C	BLC_CTRL_0C	0x00	RW	Bit[3:0]: r_dn_bl_start_o[3:0]
0x400D	BLC_CTRL_0D	0x07	RW	Bit[3:0]: r_dn_bl_end_o[3:0]

table 3-3 BLC control functions (sheet 2 of 2)

address	register name	default value	R/W	description
0x4010	BLC_CTRL_10	0x41	RW	Bit[7]: r_up_off_trig_en_o Bit[6]: r_gain_chg_trig_en_o Bit[5]: r_fmt_chg_trig_en_o Bit[4]: r_rst_trig_en_o Bit[3]: r_man_avg_en_o Bit[2]: r_man_trig_o Bit[1]: r_off_frz_en_o Bit[0]: r_off_always_up_o
0x4011	BLC_CTRL_11	0x7F	RW	Bit[6]: r_off_chg_mf_en_o Bit[5]: r_fmt_chg_mf_en_o Bit[4]: r_gain_chg_mf_en_o Bit[3]: r_rst_mf_mode_o Bit[2]: r_off_chg_mf_mode_o Bit[1]: r_off_chg_mf_mode_o Bit[0]: r_gain_chg_mf_mode_o

3.5 system clock control

The OG02B1B has two on-chip PLLs which generate the system clock from a 6~27 MHz input clock. A programmable clock divider is provided to generate different frequencies for the system.

3.5.1 PLL configuration

PLL settings can only be changed during sensor standby mode. Register 0x0100 is set to 0.

figure 3-5 PLL1 clock diagram

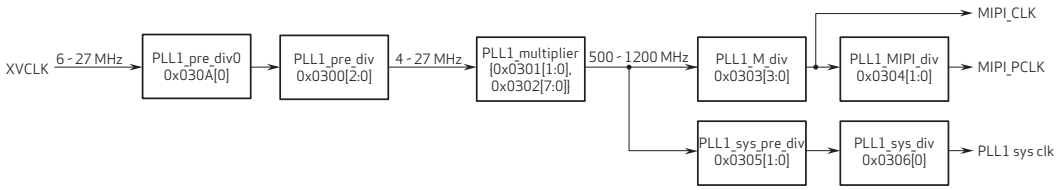
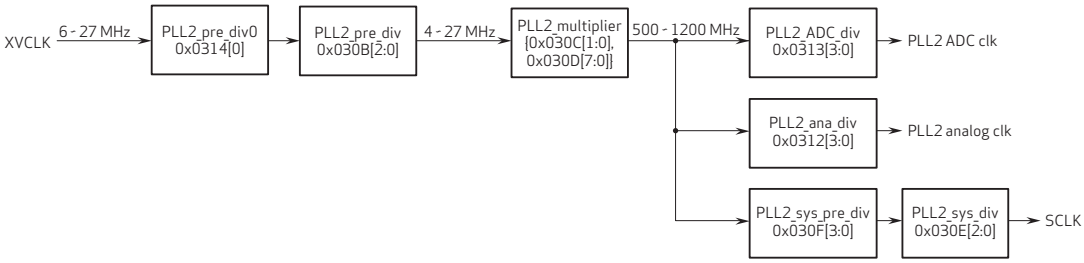


figure 3-6 PLL2 clock diagram



note Contact your local OmniVision FAE for additional assistance on PLL configuration.

table 3-4 PLL control registers (sheet 1 of 2)

function	address	description
PLL1_pre_div0	0x030A	Bit[0]: pll1_predivp 0: /1 1: /2
PLL1_pre_div	0x0300	Bit[2:0]: pll1_prediv 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /4 110: /6 111: /8
PLL1_multiplier	0x0301	Bit[1:0]: pll1_mult[9:8]
PLL1_multiplier	0x0302	Bit[7:0]: pll1_mult[7:0]

table 3-4 PLL control registers (sheet 2 of 2)

function	address	description
PLL1_sys_pre_div	0x0305	Bit[1:0]: pll1_divsp 00: /3 01: /4 10: /5 11: /6
PLL1_sys_div	0x0306	Bit[0]: pll1_divs 0: /1 1: /2
PLL1_M_div	0x0303	Bit[3:0]: pll1_divm
PLL1_MIPI_div	0x0304	Bit[1:0]: pll1_div_mipi 00: /4 01: /5 10: /6 11: /8
PLL2_pre_div0	0x0314	Bit[0]: pll2_predivp 0: /1 1: /2
PLL2_pre_div	0x030B	Bit[2:0]: pll2_prediv 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /4 110: /6 111: /8
PLL2_multiplier	0x030C	Bit[1:0]: pll2_mult[9:8]
PLL2_multiplier	0x030D	Bit[7:0]: pll2_mult[7:0]
PLL2_sys_pre_div	0x030F	Bit[3:0]: pll2_divsp
PLL2_sys_div	0x030E	Bit[2:0]: pll2_divs 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /3.5 110: /4 111: /5
PLL2_ADC_div	0x0313	Bit[3:0]: pll2_div_dac
PLL2_ana_div	0x0312	Bit[3:0]: pll2_div_sa1

table 3-5 sample PLL configuration[a]

name	address	value
PLL1_pre_div0	0x030A[0]	1'h0
PLL1_pre_div	0x0300[2:0]	3'h1
PLL1_multiplier[9:8]	0x0301[1:0]	2'h0
PLL1_multiplier[7:0]	0x0302[7:0]	8'h32
PLL1_sys_pre_div	0x0305[1:0]	2'h2
PLL1_sys_div	0x0306[0]	1'h1
PLL1_M_div	0x0303[3:0]	4'h0
PLL1_MIPI_div	0x0304[1:0]	2'h3
PLL2_pre_div0	0x0314[0]	1'h0
PLL2_pre_div	0x030B[2:0]	3'h4
PLL2_multiplier[9:8]	0x030C[1:0]	2'h0
PLL2_multiplier[7:0]	0x030D[7:0]	8'h5A
PLL2_sys_pre_div	0x030F[3:0]	4'h2
PLL2_sys_div	0x030E[2:0]	3'h4
PLL2_ADC_div	0x0313[3:0]	4'h1
PLL2_ana_div	0x0312[3:0]	4'h8
SYS_CLK		80 MHz
MIPI_PCLK		100 MHz
MIPI_CLK		800 Mbps
XVCLK		24 MHz

a. PLL control for 2 megapixel @ 60 fps with 2-lane, 10-bit output

figure 3-7 clock connection diagram

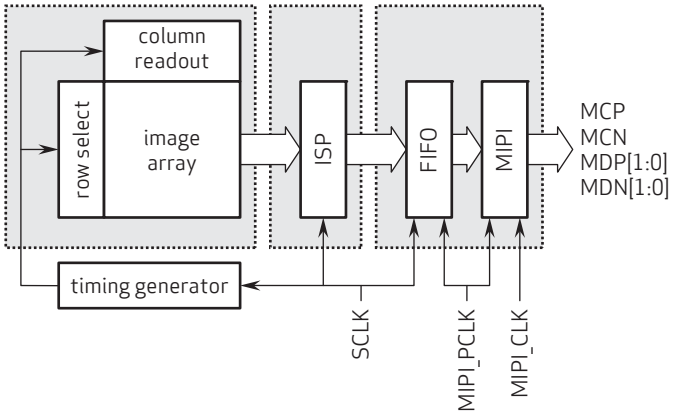


table 3-6 PLL speed limitation

parameter	value
PLL1_multiplier input	4~27 MHz
PLL1_multiplier output	500~1200 MHz
PLL2_multiplier input	4~27 MHz
PLL2_multiplier output	500~1200 MHz
SYS_CLK	up to 80 MHz

3.6 temperature sensor

The OG02B1B is equipped with the on-chip temperature sensor that covers -64° ~ +192°C. It can be controlled through the SCCB interface (see **figure 3-7**).

The temperature value can be read from registers (0x4417, 0x4418). The value of 0x4417 is the integer part of the measured temperature in Celsius degree. The value of 0x4418 is the decimal part of the measured temperature. The valid readout temperature range is from -63.996°C (-3F.FF) to 192°C (C0.00).

If (0x4417, 0x4418) ≤ 0xC000, the temperature is positive, JT(°C) = (0x4417, 0x4418)/256. If (0x4417, 0x4418) > 0xC000, the temperature is negative, JT(°C) = - ({0x4417, 0x4418} - 0xC000)/256.

table 3-7 temperature control registers

address	register name	default value	R/W	description
0x4407	TPM CTRL 07	0x31	RW	Bit[3]: TPM power down
0x4417	TPM2 INTEGER	–	R	Bit[7:0]: Integer part of temperature value
0x4418	TPM2 DECIMAL	–	R	Bit[7:0]: Decimal part of temperature value

3.7 LED PWM

The LED PWM driver is used to turn on an LED indicator light when the camera is transmitting image data. The driver uses pad clock input from 6~27 MHz and drives LED to be active when the OG02B1B image sensor is outputting image data. The output frequency of LED PWM driver can be adjusted by LED_FREQ_DIV_CYCLE from 1k to 100kHz and the duty cycle of the output can be adjusted from 0~100% by setting the DUTY_CYCLE_REG register from 0~65535. Minimum duty cycle can also be limited by register LED_DUTY_CYCLE_LOW.

The following parameter setting is stored in OTP memory:

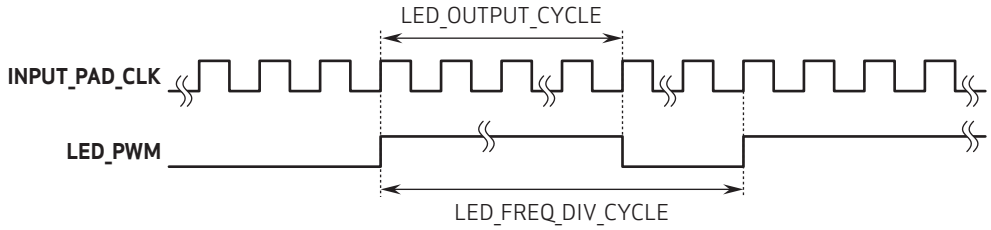
- LED_DUTY_CYCLE_LOW: (16-bit) minimum duty cycle output
- LED_FREQ_DIV_CYCLE: (16-bit) LED driver output frequency divider

The LED PWM output is calculated as follows:

- LED_FREQ = INPUT_PAD_CLK_FREQ / LED_FREQ_DIV_CYCLE
- LED_OUTPUT_CYCLE = LED_FREQ_DIV_CYCLE × DUTY_CYCLE_REG / 65535

LED_PWM pin is a dedicated output pin and can only be tri-state in XSHUTDOWN mode for security. The pin will drive low in software standby (sleep) and hardware standby (power down) mode.

figure 3-8 LED PWM output timing




```
@@ LED PWM example setting

C0 3006 04 04; bit operation, set 3006[2]=1

C0 3910 10 ;div_reg

C0 3911 00 ;div_reg

C0 3912 80 ;duty_reg, %

C0 3913 00 ;duty_reg, %

C0 3914 10 ;led_duty_cycle_low_reg, %

C0 3915 00 ;led_duty_cycle_low_reg, %

C0 391C 01 ;led_pwm_ctrl0.[4] [0]duty_chg_en. dft:'h00
```

table 3-8 LED PWM registers

address	register name	default value	R/W	description
0x3912	DUTY CYCLE REG	0x08	RW	Bit[7:0]: Desirable duty cycle from 0~100% for LED_PWM output[15:8] Range: 0~65535
0x3913	LED_PWM_REG03	0x00	RW	Bit[7:0]: Desirable duty cycle from 0~100% for LED_PWM output[7:0] Range: 0~65535

table 3-9 non-volatile memory map table (OTP)

OTP address	description
0x3D0A	Bit[7:0]: LED_FREQ_DIV_CYCLE[15:8]
0x3D0B	Bit[7:0]: LED_FREQ_DIV_CYCLE[7:0]
0x3D08	Bit[7:0]: LED_DUTY_CYCLE_LOW[15:8]
0x3D09	Bit[7:0]: LED_DUTY_CYCLE_LOW[7:0]

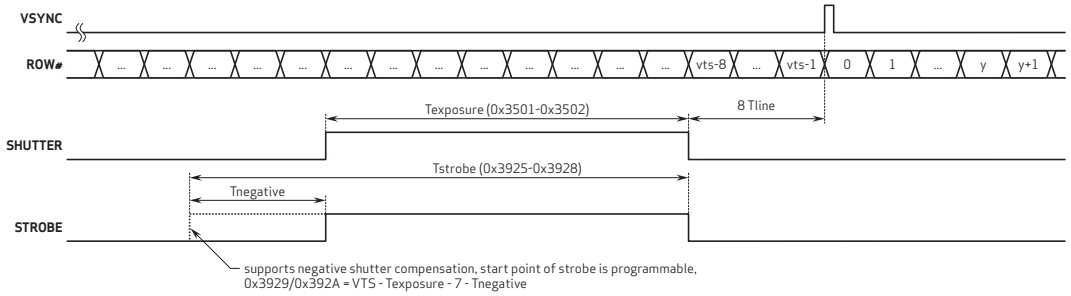
3.8 strobe

Strobe facilitates implementation of a flashlight. It generates a pulse with a reference starting point at the time when the pixel array starts integration. It also supports negative strobe control.

It is necessary to program the strobe width and negative shutter compensation every time during exposure time update for the OG02B1B.

The integration end point to SOF is fixed to 8 Tlines. The start point of strobe is programmable, which is {0x3929, 0x392A} = VTS - Texposure - 7 - Tnegative.

figure 3-9 strobe timing diagram




```
@@ Strobe Control example setting

C0 3006 08 08 ; bit operation, set 0x3006[3]=1

C0 3004 02 02 ; bit operation, set 0x3004[1]=1

C0 3007 02

C0 301C 20 20 ;enable clock for group write

C0 3020 20 20 ;strobe logic always on

C0 3025 02

C0 382C 0A

C0 382D F8

C0 3920 FF

C0 3921 00

C0 3923 00 ; delay

C0 3924 00 ;

C0 3925 00 ; width

C0 3926 00
```

```
C0 3927 00

C0 3928 80

C0 392B 00

C0 392C 00

C0 392D 03 ; suggest set same as HTS

C0 392E A8

C0 392F 0B

C0 38B3 07

C0 3885 07

C0 382B 3A

C0 3670 68

;Below need program every time during exposure update

;Exp = 1, Gain = 1x

C0 3208 00

C0 3501 00 ; exp

C0 3502 01

C0 3508 01 ; gain

C0 3509 00

C0 3927 00 ; strobe width

C0 3928 01

C0 3929 05 ; strobe start point is VTS - Texposure - 7 - Tnegative,

C0 392A 80 ; here VTS = 0x588, Texposure = 1, if Tnegative = 0, then R3929/2A = 0x580

C0 3208 10

C0 3208 A0
```

table 3-10 strobe control registers

address	register name	default value	R/W	description
0x3921	PWM_CTRL_21	0x00	RW	Bit[7]: Shift direction Bit[6:0]: strobe_frame_shift[30:24]
0x3922	PWM_CTRL_22	0x00	RW	Bit[7:0]: strobe_frame_shift[23:16]
0x3923	PWM_CTRL_23	0x00	RW	Bit[7:0]: strobe_frame_shift[15:8]
0x3924	PWM_CTRL_24	0x05	RW	Bit[7:0]: strobe_frame_shift[7:0]
0x3925	PWM_CTRL_25	0x00	RW	Bit[7:0]: strobe_frame_span[31:24]
0x3926	PWM_CTRL_26	0x00	RW	Bit[7:0]: strobe_frame_span[23:16]
0x3927	PWM_CTRL_27	0x00	RW	Bit[7:0]: strobe_frame_span[15:8]
0x3928	PWM_CTRL_28	0x1A	RW	Bit[7:0]: strobe_frame_span[7:0]
0x3929	PWM_CTRL_29	0x01	RW	Bit[7:0]: r_strobe_row_st[15:8]
0x392A	PWM_CTRL_2A	0xB4	RW	Bit[7:0]: r_strobe_row_st[7:0]
0x392B	PWM_CTRL_2B	0x00	RW	Bit[7:0]: r_strobe_cs_st[15:8]
0x392C	PWM_CTRL_2C	0x10	RW	Bit[7:0]: r_strobe_cs_st[7:0]
0x392D	PWM_CTRL_2D	0x05	RW	Bit[7:0]: step_onerow_man[15:8]
0x392E	PWM_CTRL_2E	0xF2	RW	Bit[7:0]: step_onerow_man[7:0]
0x392F	PWM_CTRL_2F	0x40	RW	Bit[7]: r_strobe_frm_pwen Bit[6]: r_strobe_frm_pwst Bit[5]: r_strobe_pol Bit[4]: r_strobe_step_pix Bit[3]: r_step_onerow_precision_man Bit[2:0]: r_strobe_st_opt

3.9 low power modes

The OG02B1B sensor supports three low power modes:

- low frame rate streaming mode
- internal trigger snapshot mode
- external trigger snapshot mode

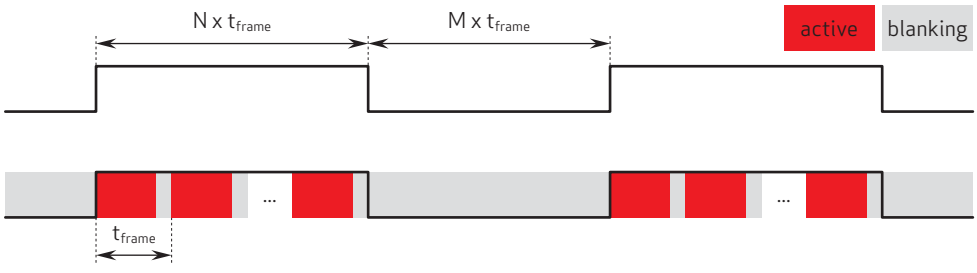
table 3-11 low power mode control registers

register	description
0x4F00	Power Control Options 0x00: Normal mode 0x01: Low power mode
0x3030	Low Power Mode Control Bit[4]: Low frame rate streaming mode (i.e., repeating the sequence of streaming {0x303F} frames and then sleeping {0x302C, 0x302F} lines) Bit[2]: External trigger snapshot mode A rising edge on FSIN pin wakes the sensor up and streams out {0x303F} frames Others: For debug only
0x303F	Number of Active Frames
{0x302C, 0x320F}	Number of Lines of Sleep Period
0x3023	Bit[1]: MIPI power down enable during sleep period 0: Disable for low power streaming mode

3.9.1 low frame rate mode

In low frame rate mode, the OG02B1B sensor streams N frames, idles for M frames, and then repeats. The power consumption of the OG02B1B sensor is close to N/(N+M) of the current in full speed streaming mode but the maximum integration time is limited to about t_{Frame} - $40t_{Row}$.

figure 3-10 low frame rate mode timing

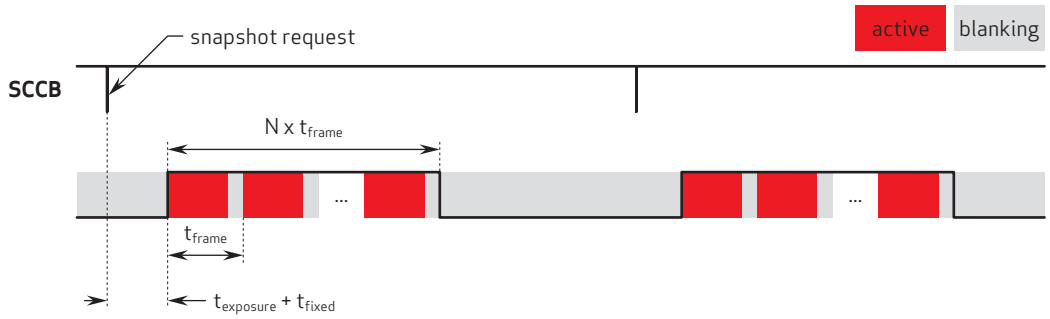


```
@@ Low frame rate streaming mode example setting

C0 303F 01 ;r_frame_on_num. (active frames after wake-up)

C0 31FF 00 ;Change to Clockless SCCB

C0 0100 00

;low frame rate streaming mode, switch between sleep <=> active certain frames

C0 3030 10

C0 3030 90
```

3.9.2 snapshot mode

In snapshot mode, the OG02B1B streams N frames upon request through the SCCB and then stays idle until the next request (see **figure 3-11**).

figure 3-11 snapshot mode timing

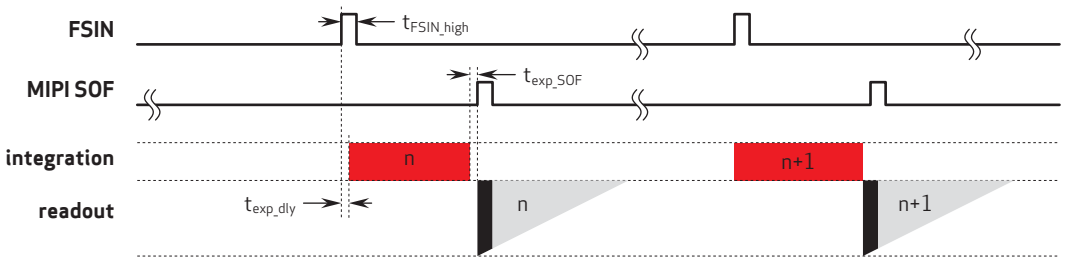



```
@@ Snapshot mode example setting

C0 303F 01 ;r_frame_on_num. (active frames after wake-up)

C0 31FF 00 Change to Clockless SCCB

C0 0100 00

;register to wake => active certain frames => sleep

C0 3030 10

C0 3030 80
```

3.9.3 external trigger snapshot mode

Upon the rising edge of FSIN pulse, the sensor wakes up from sleep mode, starts integration, reads out and sends out number (set by 0x303F) of frames. The sensor then returns back to sleep mode (see **figure 3-12**).

figure 3-12 external snapshot mode timing



FSIN pulse width, t_{FSIN_High}, should be no shorter than 5 input clock cycles. The wake up sequence takes 16388 input clock cycles, and then the pixel array is reset. The integration starts when the pixel reset finish, the interval from FSIN rising to integration, t_{Exp_Dly}, equals to $16388 \times t_{XVCLK} + 11 \times t_{Row}$. The frame start short packet is sent out about 10 row periods after integration finish.

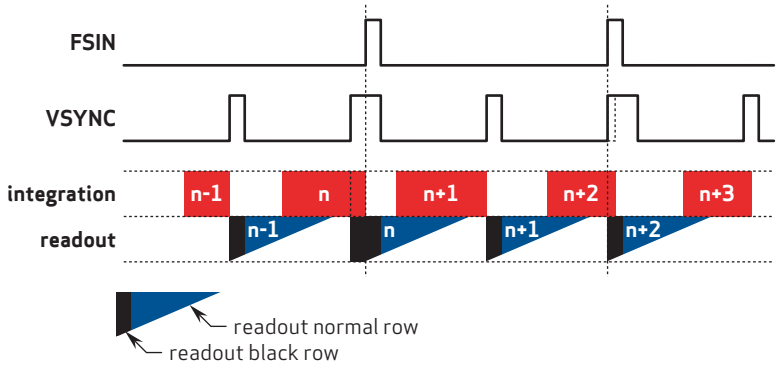
```
@ external trigger snapshot mode example setting

C0 3006 00 02 ;disable FSIN output, bit operation, set 0x3006[1]=0

C0 303F 01 ;r_frame_on_num. (active frames after wake-up)

C0 31FF 00 ;Change to Clockless SCCB

C0 0100 00

;FSIN trigger wake => active certain frames => sleep

C0 3030 10

C0 3030 84
```

3.10 FSIN

3.10.1 frame sync

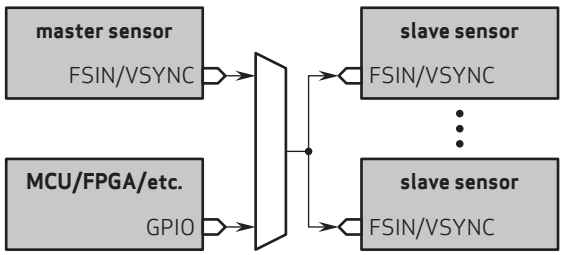
Frame sync input (FSIN) is designed to synchronize video frame timing for a multi-camera system. Upon FSIN rising edge, the sensor will reset read out timing to align the frame start to FSIN. FSIN will not change anything that has already happened (e.g., the start point of the integration of frame n and frame n+2 in **figure 3-13**). The integration time (end point of integration) of these frames will be slightly modified by FSIN.

figure 3-13 FSIN timing



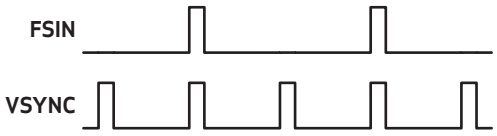
FSIN signal can be generated from a master sensor or any device that is capable of generating a pixel cycle accurate periodic signal.

figure 3-14 FSIN/VSYNC connection between sensors



FSIN period must be integer multiple of the sensor frame period and the tolerance is no more than half row period.

figure 3-15 FSIN/VSYNC timing




```
;Frame sync mode example setting

@@ master

C0 3006 02 02 ;enable FSIN output, bit operation, set 0x3006[1]=1

C0 3823 00

@@ slave (OG02B)

C0 3006 00 02 ;disable FSIN output, bit operation, set 0x3006[1]=0

C0 38B3 07

C0 3885 07

C0 382B 5A

C0 3670 68

C0 3823 30   ;//[5] ext_vs_en ;//[4] r_init_man_en

C0 3824 00   ;//sclk -> cs counter reset value at vs_ext

C0 3825 08   ;//set it to 8

C0 3826 05   ;//sclk -> r counter reset value at vs_ext

C0 3827 BE   ;//vts = 'h5C2 as default, set r counter to vts-4
```

3.10.2 frame sync in DVP mode

The OG02B1B FSIN and VSYNC share the same pin. In DVP mode, the backend chip still needs VSYNC from the sensor. The FSIN pin cannot change, while VSYNC can output from other pins, such as PWM. Here is an example setting to output VSYNC from the PWM pin.

```
;VSYNC from PWM pin

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

; function VSYNC

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

#define VSYNC_OUT

#ifdef VSYNC_OUT

    r3006 =  r3006 | 04 ;[2]io_pwm_oen (PWM PAD as output for VSYNC)

    r3006 =  r3006 & fd ;[1]io_fsin_oen (FSIN PAD as input for master-slave sync/lpm
trigger)

    r3667 = r3667 | 60 ;[6:4]pad_share_pwm_o

    r3667 = r3667 & EF ;[6:4]pad_share_pwm_o

    r3816 = 00

    r3817 = 01 ;vsync_st

    r3818 = 00

    r3819 = 05 ;vsync_ed

#endif
```

3.11 group hold

The group write function is for updating a group of registers at a guaranteed timing, so that they take effect starting from the same frame. The sensor latches critical parameters (e.g., exposure time, gain etc.) at the beginning of each frame. All values are guaranteed to be programmed to the target registers prior to the next latching point after the group write launching command.

The sensor can store up to six groups of registers in its buffer. The total buffer size is 1536 bytes. The buffer size for each group is programmable. The start address of these six groups are set by registers {0x3200[3:0], 4'h0} ~ {0x3204[6:0], 4'h0}, respectively. The default size for group 0 ~ group 3 is 128 bytes. Group 4 is 256 bytes. The remaining bytes are for group 5. The users can adjust the sizes according to their applications. The last two groups are special groups used to specify the list of registers to be sent out in the embedded line.

By default, the sensor shuts down the clock of the group write function block during a long vertical blanking period to save power. To always enable the clock for group write function, register 0x301C[5] should be set to 1.

The group write procedure usually consists of register recording and launching. The register recording is started by writing 4'h0 to register 0x3208[7:4] with the group ID specified in register 0x3208[3:0]. After writing to all intended registers, write 4'h1 to register 0x3208[7:4] with group ID in 0x3208[3:0] to terminate the recording.

The following is an example sequence to program the gain and exposure time using group 0.

```
C0 3208 00

C0 3508 01

C0 3509 00

C0 3501 03

C0 3502 BA

C0 3208 10
```

To program the register settings recorded, write 4'hA to register 0x3208[7:4] with the group ID in register 0x3208[3:0]. The registers will be programmed to the target registers prior to next latching point.

```
C0 3208 A0
```

Group write can be used to switch two to four groups of settings repeatedly. When there are only two groups to switch back and forth, the group period of group 3 and group 4 should be zero. The default sequence is group 0 -> group 1 -> group 2 -> group 3. The two groups of settings should be recorded first. The first setting must be recorded in group 0. The second setting can be recorded in either one of group 1~3. The number of frames for the sensor to stay at each group of setting are set by registers 0x3209~0x320C, respectively. Set register 0x320D[7:4] to 3 and specify the second group ID in register 0x320D[1:0], then launch group 0 by writing 0xA0 to register 0x3208. The sensor will launch group 0, stay for the number of frames specified by register 0x3209, then launch the second group specified by register 0x320D[1:0], and stay for the number of frames for that group, and repeat this sequence until group write function is reset by register 0x301C[1].

```
;Group auto switch example setting
C0 301C F0 ; enable the clock for group write function
C0 3209 05 ; number of frames to stay at group 0
C0 320A 03 ; number of frames to stay at group 1
C0 320B 00 ; set group 2 period to 0
C0 320C 00 ; set group 3 period to 0

; Define group 0
C0 3208 00 ;Group write 0 start
C0 3501 01
C0 3502 20
C0 3509 20
C0 3208 10 ;Group write 0 end

; Define group 1
C0 3208 01 ;Group write 1 start
C0 3501 02
C0 3502 40
C0 3509 40
C0 3208 11 ;Group write 1 end

;Auto mode switch between group0 and group1
;setting to switch
C0 320D 00; disable switch
C0 320D 31; [5]: repeat [4]: context_sw
C0 3208 A0
```

table 3-12 group hold registers

address	register name	default value	R/W	description
0x3200	GROUP ADR0	0x00	RW	Group0 Start Address in SRAM Actual Address is {0x3200[6:0], 4'h0}
0x3201	GROUP ADR1	0x08	RW	Group1 Start Address in SRAM Actual Address is {0x3201[6:0], 4'h0}
0x3202	GROUP ADR2	0x10	RW	Group2 Start Address in SRAM Actual Address is {0x3202[6:0], 4'h0}
0x3203	GROUP ADR3	0x18	RW	Group3 Start Address in SRAM Actual Address is {0x3203[6:0], 4'h0}
0x3204	GROUP ADR4	0x20	RW	SOF Triggered Embedded Line Data Start Address in SRAM Actual Address is {0x3204[6:0], 4'h0}
0x3206	FSIN_GRP	0x10	RW	Bit[4]: fsin_en Bit[1:0]: Start group in FSIN mode
0x3207	COMBINE_LAUNCH _CTRL	–	W	Bit[7:4]: Launch select 0xA: Launch in frame blanking 0xE: Launch immediately 0x6: Launch in horizontal blanking Others: Not used Bit[3]: cmb_launch_grp3 Bit[2]: cmb_launch_grp2 Bit[1]: cmb_launch_grp1 Bit[0]: cmb_launch_grp0
0x3208	GROUP ACCESS	–	W	Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 1010: Group launch 1110: Fast group launch Others: Reserved Bit[3:0]: Group ID 0000: Group bank 0 0001: Group bank 1 0010: Group bank 2 0011: Group bank 3 Others: Reserved
0x3209	GROUP0 PERIOD	0x00	RW	Frame Number to Stay in Group 0
0x320A	GROUP1 PERIOD	0x00	RW	Frame Number to Stay in Group 1
0x320B	GROUP2 PERIOD	0x00	RW	Frame Number to Stay in Group 2
0x320C	GROUP3 PERIOD	0x00	RW	Frame Number to Stay in Group 3
0x320D	GRP SW_CTRL	0x01	RW	Bit[5]: Repeat switch mode Bit[4]: Context switch enable Bit[1:0]: Switch back group

4 image processor

4.1 ISP general controls

table 4-1 ISP top registers

address	register name	default value	R/W	description
0x5000	ISP CTRL 00	0x9F	RW	Bit[7:6]: isp_sof_sel Bit[5]: isp_eof_sel Bit[4]: otp_dpc_en Bit[3]: dpc_en Bit[2]: dpc_buf_en Bit[1]: awbg_en Bit[0]: blc_en
0x5001	ISP CTRL 01	0x20	RW	Bit[5]: ptdp_en Bit[4]: latch_en Bit[3]: r_size_man Bit[2]: r_pre_isp_raw_en Bit[1]: bypass_isp1 Bit[0]: bypass_isp0

4.2 mirror and flip

The OG02B1B provides mirror and flip readout modes, which respectively reverse the sensor data readout order horizontally and vertically (see **figure 4-1**).

figure 4-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

table 4-2 mirror and flip registers

address	register name	default value	R/W	description
0x3820	IMAGE_ ORIENTATION	0x00	RW	Timing Control Register Bit[6]: vflip_blc Bit[2]: Vertical flip enable 0: Normal 1: Vertical flip
0x3821	IMAGE_ ORIENTATION	0x00	RW	Timing Control Register Bit[2]: Horizontal mirror enable 0: Normal 1: Horizontal mirror

```
; Mirror_Flip example setting
@@ Mirror_Off_Flip_Off
C0 3820 00 44 ; bit operation, set 0x3820[6][2]=00
C0 3821 00 04 ; bit operation, set 0x3821[2]=0
@@ Mirror_On_Flip_Off
C0 3820 00 44
C0 3821 04 04
@@ Mirror_Off_Flip_On
C0 3820 44 44
C0 3821 00 04
@@ Mirror_On_Flip_On
C0 3820 44 44
C0 3821 04 04
```

4.3 image windowing

An image windowing area is defined by four parameters, horizontal start (HS), horizontal end (HE), vertical start (VS), and vertical end (VE). By properly setting the parameters, any portion within the sensor array size can output as a visible area. Windowing is achieved by simply masking off the pixels outside of the window; thus, the timing is not affected.

figure 4-2 image windowing

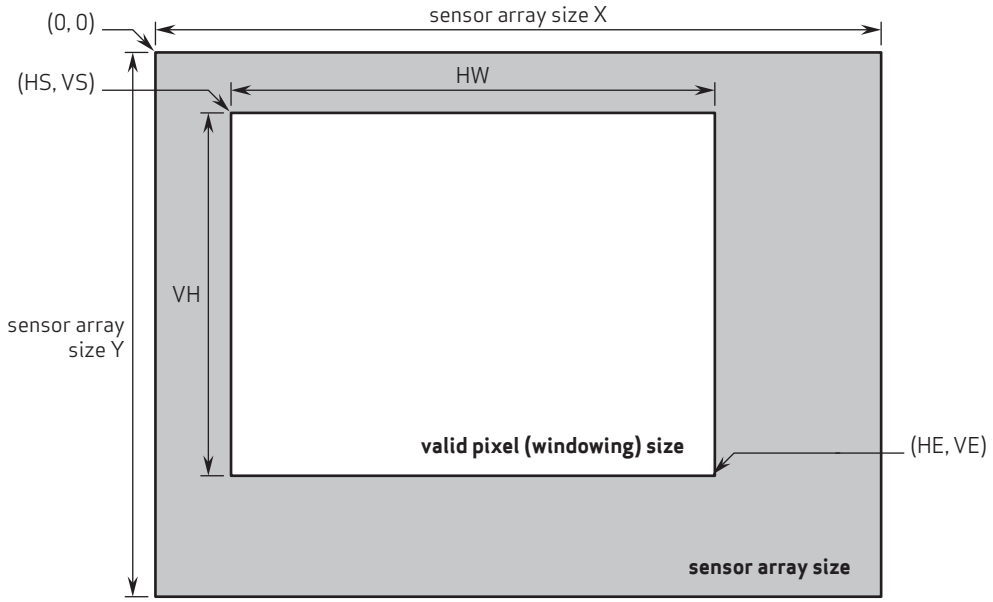


table 4-3 image windowing control functions

function	register	R/W	description
horizontal start	{0x3800, 0x3801}	RW	HS[9:8] = 0x3800 HS[7:0] = 0x3801
vertical start	{0x3802, 0x3803}	RW	VS[9:8] = 0x3802 VS[7:0] = 0x3803
horizontal end	{0x3804, 0x3805}	RW	HE[9:8] = 0x3804 HE[7:0] = 0x3805
vertical end	{0x3806, 0x3807}	RW	VE[9:8] = 0x3806 VE[7:0] = 0x3807

4.4 test pattern

For testing purposes, the OG02B1B offers two test patterns:

4.4.1 general test pattern bar

figure 4-3 test pattern

table 4-4 general test pattern bar selection control

function	register	default value	R/W	description
general test pattern bar	0x5E00	0x00	RW	Bit[7]: Test pattern bar enable

4.4.2 solid color test pattern

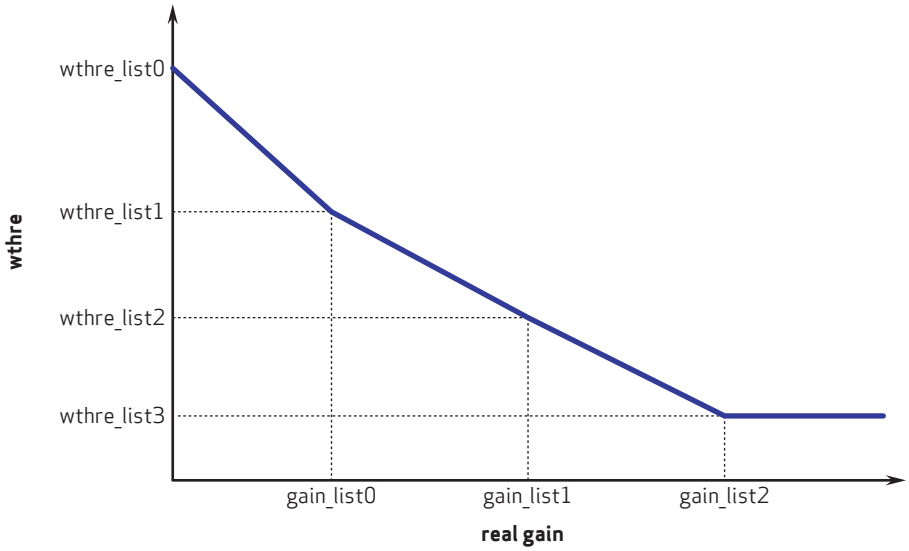
table 4-5 solid color test pattern control

function	register	default value	R/W	description
solid test pattern	0x4320	0x80	RW	Bit[7:6]: Pixel order 00: P3P4/P1P2 01: P4P3/P2P1 10: P1P2/P3P4 11: P2P1/P4P3 Bit[1]: Solid test pattern enable 0: Solid test pattern OFF 1: Solid test pattern enable
solid pattern P1	0x4322	0x00	RW	Bit[1:0]: solid_testpattern_P1[9:8]
solid pattern P1	0x4323	0x00	RW	Bit[7:0]: solid_testpattern_P1[7:0]
solid pattern P2	0x4324	0x00	RW	Bit[1:0]: solid_testpattern_P2[9:8]
solid pattern P2	0x4325	0x00	RW	Bit[7:0]: solid_testpattern_P2[7:0]
solid pattern P4	0x4326	0x00	RW	Bit[1:0]: solid_testpattern_P4[9:8]
solid pattern P4	0x4327	0x00	RW	Bit[7:0]: solid_testpattern_P4[7:0]
solid pattern P3	0x4328	0x00	RW	Bit[1:0]: solid_testpattern_P3[9:8]
solid pattern P3	0x4329	0x00	RW	Bit[7:0]: solid_testpattern_P3[7:0]

4.5 defective pixel cancellation (DPC)

The DPC function detects defect pixels/clusters by using a programmable threshold. The threshold can be set manually by registers or automatically calculated based on analog gain. Refer to figure **figure 4-4** for details.

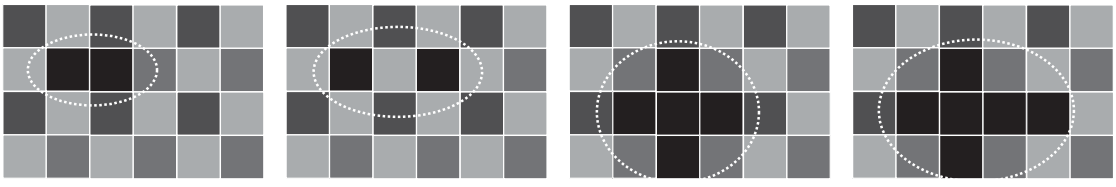
figure 4-4 threshold gain curve



note Bthre = Wthre * (8+thre_ratio)/8

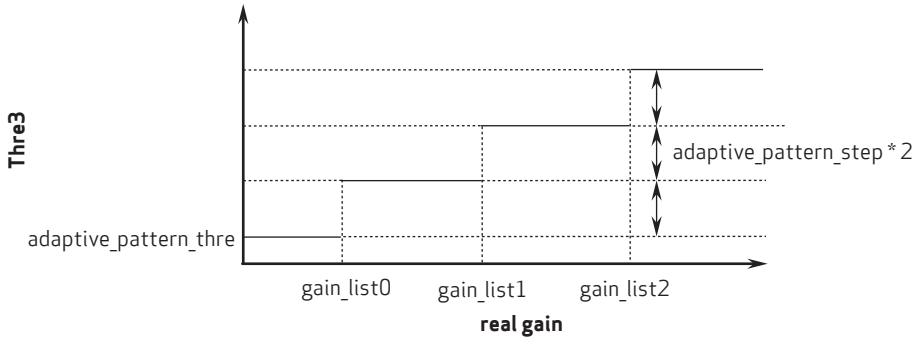
The DPC can correct single defect pixel, couplet, cross type and tail type cluster (refer to **table 4-6** for the enable/disable controls for each type of defect). **figure 4-5** shows the sample defect pattern of couplet, cross and tail cluster defect.

figure 4-5 defect pattern examples



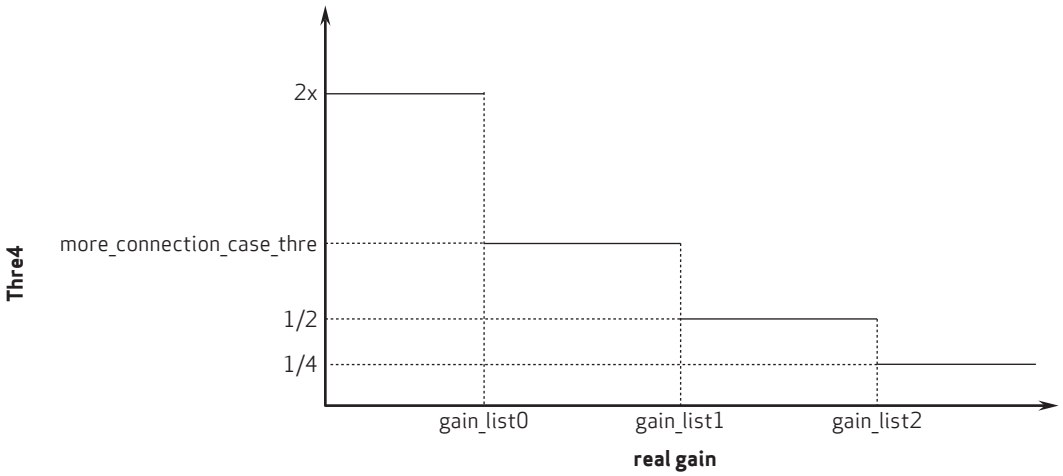
different color plane couplet | same color plane couplet | cross type cluster | tail type cluster

figure 4-6 adaptive thresholds



If there are two similar defective pixels not far from each other, they cannot be recovered. To resolve this, the DPC algorithm will only search for similar patterns in high frequency regions. When the difference between minimum and maximum values are below the adaptive threshold, the current pixel is considered located in a high frequency region. Smaller threshold values will retain more image details.

figure 4-7 connected case thresholds



When detecting the same or different channel connected defect pixels, the difference between the central pixel and surrounding normal pixels must be below this threshold. Compared to a single white or black pixel, these clusters will further degrade the image quality, thus a separate threshold is designed for them. These thresholds are higher than single defect pixel thresholds as connected cases are less common.

table 4-6 DPC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5B00	DPC CTRL00	0x1B	RW	Bit[7]: Tail enable Bit[6]: General tail enable Bit[5]: 3x3 cluster enable Bit[4]: Saturate cross cluster enable Bit[3]: Cross cluster enable Bit[2]: Manual mode enable Bit[1]: Black pixel correction enable Bit[0]: White pixel correction enable
0x5B01	DPC CTRL01	0x94	RW	Bit[7:6]: VNumList2 Bit[5:4]: VNumList1 Bit[3:2]: VNumList0 Bit[1]: Clip interpg enable Bit[0]: Share buffer enable
0x5B02	DPC CTRL02	0x2E	RW	Bit[5:4]: Pixel order man Bit[3:2]: Edge option Bit[1:0]: VNumList3
0x5B03	DPC CTRL03	0x24	RW	Bit[6:3]: WThresList0 Bit[2:0]: Max VNum
0x5B04	DPC CTRL04	0x12	RW	Bit[7:4]: WThresList2 Bit[3:0]: WThresList1
0x5B05	DPC CTRL05	0x41	RW	Bit[7:4]: BThresRatio Bit[3:0]: WThresList3
0x5B06	DPC CTRL06	0x48	RW	Bit[7:4]: Status threshold Bit[3:0]: More connection case threshold
0x5B07	DPC CTRL07	0x84	RW	Bit[7:4]: Matching threshold Bit[3:0]: Status threshold step
0x5B08	DPC CTRL08	0x40	RW	Bit[7:4]: Adaptive pattern step Bit[3:0]: Adaptive pattern threshold
0x5B09	DPC CTRL09	0x00	RW	Bit[3:0]: Saturate
0x5B0A	DPC CTRL0A	0x03	RW	Bit[7:0]: Gain list0
0x5B0B	DPC CTRL0B	0x0F	RW	Bit[7:0]: Gain list1
0x5B0C	DPC CTRL0C	0x3F	RW	Bit[7:3]: Gain list2
0x5B0D	DPC CTRL0D	0x0F	RW	Bit[7:0]: DPC level list0
0x5B0E	DPC CTRL0E	0xFD	RW	Bit[7:0]: DPC level list1
0x5B0F	DPC CTRL0F	0xF5	RW	Bit[7:0]: DPC level list2
0x5B10	DPC CTRL10	0xF5	RW	Bit[7:0]: DPC level list3
0x5B11	DPC CTRL11	0x02	RW	Bit[1]: Saturate option

table 4-6 DPC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5B14	DPC CTRL14	0x00	RW	Bit[7]: Clock gate disable rec2 Bit[6]: Clock gate disable rec1 Bit[5]: Clock gate disable rec0 Bit[4]: Clock gate disable SRAM Bit[3]: Clock gate disable buffer Bit[2]: Clock gate disable SF Bit[1]: Clock gate disable Bit[0]: Manual pixel order enable
0x5B1E	DPC STAT 1E	–	R	Bit[6:0]: BThre
0x5B1F	DPC STAT 1F	–	R	Bit[4:0]: WThre
0x5B20	DPC STAT 20	–	R	Bit[4:0]: Thre1
0x5B21	DPC STAT 21	–	R	Bit[7:0]: Thre2
0x5B22	DPC STAT 22	–	R	Bit[6:0]: Thre3
0x5B23	DPC STAT 23	–	R	Bit[6:0]: Thre4
0x5B24	DPC STAT 24	–	R	Bit[7:4]: Level Bit[3:0]: PConnected
0x5B25	DPC STAT 25	–	R	Bit[2:0]: VNum
0x5B26	DPC STAT 26	–	R	Bit[7:0]: DPC_version[15:8]
0x5B27	DPC STAT 27	–	R	Bit[7:0]: DPC_version[7:0]

5 image output interface

5.1 mobile industry processor interface (MIPI)

The OG02B1B supports a one/two-lane MIPI transmitter interface with a data transfer rate of up to 800 Mbps per lane.

table 5-1 supported resolution and frame rate

format[a]	resolution	frame rate	methodology	internal pixel clock	MIPI data rate
full resolution	1600x1300	60 fps	full size active	160 MHz	2-lane @ 800 Mbps
720p	1280x720	90 fps	1280x720 cropping	160 MHz	2-lane @ 800 Mbps
VGA	640x480	180 fps	640x480 sub-sampling	160 MHz	2-lane @ 800 Mbps
VGA	640x480	180 fps	640x480 b&w binning	160 MHz	2-lane @ 800 Mbps

a. all formats with minimum dummy columns and rows

figure 5-1 MIPI timing

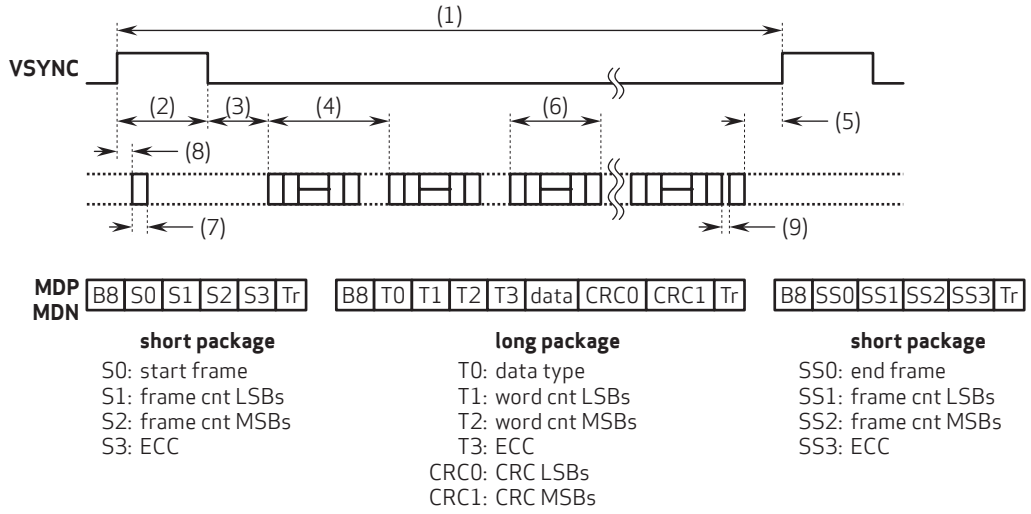


table 5-2 MIPI timing specifications (2-lane mode)

mode	timing
full resolution 1600x1300	(1) 1,333,048 t_{sclk} (2) 1,024 t_{sclk} (3) 36,408 t_{sclk} (4) 904 t_{sclk} (5) 120,448 t_{sclk} (6) 808 t_{sclk} (7) 27 t_{sclk} (8) -171 t_{sclk} (9) 35 t_{sclk}
720p 1280x720	(1) 889,486 t_{sclk} (2) 1,024 t_{sclk} (3) 34,509 t_{sclk} (4) 858 t_{sclk} (5) 236,320 t_{sclk} (6) 668 t_{sclk} (7) 27 t_{sclk} (8) -171 t_{sclk} (9) 35 t_{sclk}
VGA 640x480	(1) 444,592 t_{sclk} (2) 1,024 t_{sclk} (3) 18,367 t_{sclk} (4) 768 t_{sclk} (5) 56,918 t_{sclk} (6) 348 t_{sclk} (7) 27 t_{sclk} (8) -171 t_{sclk} (9) 35 t_{sclk}

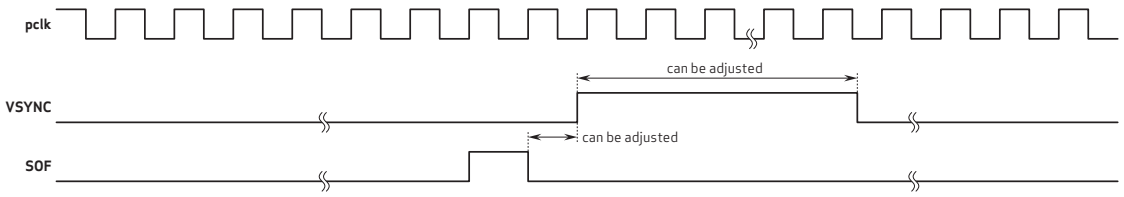
5.1.1 VSYNC timing in MIPI mode

For MIPI output interface, the VSYNC leading edge can be triggered by either the end of frame (EOF) of last frame or start of frame (SOF) of current frame. In both cases, the delay from EOF/SOF to VSYNC leading edge is controlled by registers {0x4314, 0x4315, 0x4316}, and the VSYNC pulse width is controlled by registers {0x4311, 0x4312} in unit of system clock period.

5.1.1.1 VSYNC mode 1

In mode 1, VSYNC is generated by the internal start of frame (SOF) signal (see **figure 5-2**).

figure 5-2 VSYNC timing in mode 1



5.1.1.2 VSYNC mode 2

In mode 2, VSYNC is generated by the internal end of frame (EOF) signal (see **figure 5-3**).

figure 5-3 VSYNC timing in mode 2

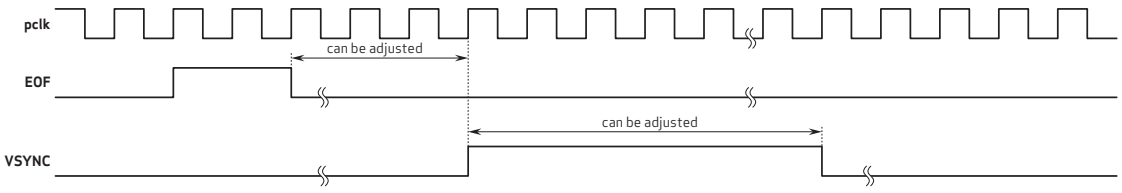


table 5-3 MIPI control registers (sheet 1 of 8)

address	register name	default value	R/W	description
0x4800	MIPI CTRL00	0x04	RW	Bit[7]: r_sc_valid_opt_o 0: Not used 1: MIPI always in high speed mode Bit[5]: gate_sc_en 0: Clock lane is free running 1: Gate clock lane when there is no packet to transmit Bit[4]: line_sync_en 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[2]: pclk_inv_o Bit[1]: first_bit Change clk_lane first bit 0: Output 8'h55 1: Output 8'hAA Bit[0]: LPX_select for pclk domain 0: Auto calculate t_lpx_p, unit pclk2x period 1: Use lpx_p_min

table 5-3 MIPI control registers (sheet 2 of 8)

address	register name	default value	R/W	description
0x4802	MIPI CTRL02	0x00	RW	Bit[7]: hs_prepare_sel 0: Auto calculate T_hs_prepare, unit pclk2x 1: Use hs_prepare_min_o[7:0] Bit[6]: clk_prepare_sel 0: Auto calculate T_clk_prepare, unit pclk2x 1: Use clk_prepare_min_o[7:0] Bit[5]: clk_post_sel 0: Auto calculate T_clk_post, unit pclk2x 1: Use clk_post_min_o[7:0] Bit[4]: clk_trail_sel 0: Auto calculate T_clk_trail, unit pclk2x 1: Use clk_trail_min_o[7:0] Bit[3]: hs_exit_sel 0: Auto calculate T_hs_exit, unit pclk2x 1: Use hs_exit_min_o[7:0] Bit[2]: hs_zero_sel 0: Auto calculate T_hs_zero, unit pclk2x 1: Use hs_zero_min_o[7:0] Bit[1]: hs_trail_sel 0: Auto calculate T_hs_trail, unit pclk2x 1: Use hs_trail_min_o[7:0] Bit[0]: clk_zero_sel 0: Auto calculate T_clk_zero, unit pclk2x 1: Use clk_zero_min_o[7:0]
0x4803	MIPI CTRL03	0x30	RW	Bit[5]: r_crc_1d_en Bit[4]: fifo_rd_spd_ol Bit[3]: manu_offset_o t_period manual offset Bit[2]: r_manu_half2one
0x4805	MIPI CTRL05	0x00	RW	Bit[3]: lpda_retim_manu_o Bit[2]: lpda_retim_sel_o 0: Not used 1: Manual Bit[1]: lpck_retim_manu_o Bit[0]: lpck_retim_sel_o 0: Not used 1: Manual

table 5-3 MIPI control registers (sheet 3 of 8)

address	register name	default value	R/W	description
0x4806	MIPI CTRL06	0x00	RW	Bit[4]: pu_mark_en_o Power up mark1 enable Bit[3]: mipi_remot_rst Bit[2]: mipi_susp Bit[1]: smia_lane_ch_en Bit[0]: tx_lsb_first 0: High bit first 1: Low power transmit low bit first
0x4807	MIPI CTRL07	0x03	RW	Bit[3:0]: sw_t_lpx Ultra low power T_lpx
0x4808	MIPI CTRL08	0x18	RW	Bit[7:0]: wkup_dly Mark1 wakeup delay/2^10
0x4810	FCNT MAX	0xFF	RW	Bit[7:0]: fcnt_max[15:8] Maximum frame counter of frame sync short packet
0x4811	FCNT MAX	0xFF	RW	Bit[7:0]: fcnt_max[7:0] Maximum frame counter of frame sync short packet
0x4813	MIPI CTRL13	0x00	RW	Bit[2]: vc_sel Bit[1:0]: VC ID
0x4814	MIPI CTRL14	0x2A	RW	Bit[6]: lpkt_dt_sel 0: Use mipi_dt 1: Use dt_man_o as long packet data Bit[5:0]: dt_man Manual data type
0x4818	HS ZERO MIN	0x00	RW	Bit[1:0]: hs_zero_min[9:8] Minimum value of hs_zero, unit ns
0x4819	HS ZERO MIN	0x70	RW	Bit[7:0]: hs_zero_min[7:0] Minimum value of hs_zero hs_zero_real = hs_zero_min_o + Tui*ui_hs_zero_min_o
0x481A	HS TRAIL MIN	0x00	RW	Bit[1:0]: hs_trail_min[9:8] Minimum value of hs_trail, unit ns
0x481B	HS TRAIL MIN	0x3C	RW	Bit[7:0]: hs_trail_min[7:0] Minimum value of hs_trail hs_trail_real = hs_trail_min_o + Tui*ui_hs_trail_min_o
0x481C	CLK ZERO MIN	0x01	RW	Bit[1:0]: clk_zero_min[9:8] Minimum value of clk_zero, unit ns

table 5-3 MIPI control registers (sheet 4 of 8)

address	register name	default value	R/W	description
0x481D	CLK ZERO MIN	0x2C	RW	Bit[7:0]: clk_zero_min[7:0] Minimum value of clk_zero clk_zero_real = clk_zero_min_o + Tui*ui_clk_zero_min_o
0x481E	CLK PREPARE MAX	0x5F	RW	Bit[7:0]: clk_prepare_max[7:0] Maximum value of clk_prepare, unit ns
0x481F	CLK PREPARE MIN	0x26	RW	Bit[7:0]: clk_prepare_min[7:0] Minimum value of clk_prepare clk_prepare_real = clk_prepare_min_o + Tui*ui_clk_prepare_min_o
0x4820	CLK POST MIN	0x00	RW	Bit[1:0]: clk_post_min[9:8] Minimum value of clk_post, unit ns
0x4821	CLK POST MIN	0x3C	RW	Bit[7:0]: clk_post_min[7:0] Minimum value of clk_post clk_post_real = clk_post_min_o + Tui*ui_clk_post_min_o
0x4822	CLK TRAIL MIN	0x00	RW	Bit[1:0]: clk_trail_min[9:8] Minimum value of clk_trail, unit ns
0x4823	CLK TRAIL MIN	0x3C	RW	Bit[7:0]: clk_trail_min[7:0] Minimum value of clk_trail clk_trail_real = clk_trail_min_o + Tui*ui_clk_trail_min_o
0x4824	LPX P MIN	0x00	RW	Bit[1:0]: lpx_p_min[9:8] Minimum value of lpx_p, unit ns
0x4825	LPX P MIN	0x32	RW	Bit[7:0]: lpx_p_min[7:0] Minimum value of lpx_p lpx_p_real = lpx_p_min_o + Tui*ui_lpx_p_min_o
0x4826	HS PREPARE MIN	0x32	RW	Bit[7:0]: hs_prepare_min[7:0] Minimum value of hs_prepare, unit ns
0x4827	HS PREPARE MAX	0x55	RW	Bit[7:0]: hs_prepare_max[7:0] Maximum value of hs_prepare hs_prepare_real = hs_prepare_max_o + Tui*ui_hs_prepare_max_o
0x4828	HS EXIT MIN	0x00	RW	Bit[1:0]: hs_exit_min[9:8] Minimum value of hs_exit, unit ns
0x4829	HS EXIT MIN	0x64	RW	Bit[7:0]: hs_exit_min[7:0] Low byte of minimum value of hs_exit hs_exit_real = hs_exit_min_o + Tui*ui_hs_exit_min_o

table 5-3 MIPI control registers (sheet 5 of 8)

address	register name	default value	R/W	description
0x482A	UI HS ZERO MIN	0x06	RW	Bit[5:0]: ui_hs_zero_min[5:0] Minimum UI value of hs_zero, unit UI
0x482B	UI HS TRAIL MIN	0x04	RW	Bit[5:0]: ui_hs_trail_min[5:0] Minimum UI value of hs_trail, unit UI
0x482C	UI CLK ZERO MIN	0x00	RW	Bit[5:0]: ui_clk_zero_min[5:0] Minimum UI value of clk_zero, unit UI
0x482D	UI CLK PREPARE	0x00	RW	Bit[7:4]: ui_clk_prepare_max Maximum UI value of clk_prepare, unit UI Bit[3:0]: ui_clk_prepare_min Minimum UI value of clk_prepare, unit UI
0x482E	UI CLK POST MIN	0x34	RW	Bit[5:0]: ui_clk_post_min[5:0] Minimum UI value of clk_post, unit UI
0x482F	UI CLK TRAIL MIN	0x00	RW	Bit[5:0]: ui_clk_trail_min[5:0] Minimum UI value of clk_trail, unit UI
0x4830	UI LPX P MIN	0x00	RW	Bit[5:0]: ui_lpx_p_min[5:0] Minimum UI value of lpx_p (pclk2x domain), unit UI
0x4831	UI HS PREPARE	0x64	RW	Bit[7:4]: ui_hs_prepare_max Maximum UI value of hs_prepare, unit UI Bit[3:0]: ui_hs_prepare_min Minimum UI value of hs_prepare, unit UI
0x4832	UI HS EXIT MIN	0x00	RW	Bit[5:0]: ui_hs_exit_min[5:0] Minimum UI value of hs_exit, unit UI
0x4833	MIPI PKT STAR SIZE	0x10	RW	Bit[5:0]: r_rdy_mark
0x4837	PCLK PERIOD	0x14	RW	Bit[7:0]: pclk_period[7:0] Period of pclk2x, pclk_div=1, and 1-bit decimal

table 5-3 MIPI control registers (sheet 6 of 8)

address	register name	default value	R/W	description
0x4838	MIPI LP GPIO0	0x00	RW	Bit[7]: lp_sel0 0: Auto generate mipi_lp_dir0_o 1: Use lp_dir_man0 to be mipi_lp_dir0_o Bit[6]: lp_dir_man0 0: Input 1: Output Bit[5]: lp_p0_o Bit[4]: lp_n0_o Bit[3]: lp_sel1 0: Auto generate mipi_lp_dir1_o 1: Use lp_dir_man1 to be mipi_lp_dir1_o Bit[2]: lp_dir_man1 0: Input 1: Output Bit[1]: lp_p1_o Bit[0]: lp_n1_o
0x4839	MIPI LP GPIO1	0x00	RW	Bit[7]: lp_sel2 0: Auto generate mipi_lp_dir2_o 1: Use lp_dir_man2 to be mipi_lp_dir2_o Bit[6]: lp_dir_man2 0: Input 1: Output Bit[5]: lp_p2_o Bit[4]: lp_n2_o Bit[3]: lp_sel3 0: Auto generate mipi_lp_dir3_o 1: Use lp_dir_man3 to be mipi_lp_dir3_o Bit[2]: lp_dir_man3 0: Input 1: Output Bit[1]: lp_p3_o Bit[0]: lp_n3_o
0x483C	MIPI CTRL3C	0x02	RW	Bit[3:0]: t_clk_pre Unit: pclk2x cycle

table 5-3 MIPI control registers (sheet 7 of 8)

address	register name	default value	R/W	description
0x483D	MIPI LP GPIO4	0x00	RW	Bit[7]: lp_ck_sel0 0: Auto generate mipi_ck_lp_dir0_o 1: Use lp_ck_dir_man0 to be mipi_ck_lp_dir0_o Bit[6]: lp_ck_dir_man0 0: Input 1: Output Bit[5]: lp_ck_p0_o Bit[4]: lp_ck_n0_o Bit[3]: lp_ck_sel0 0: Auto generate mipi_ck_lp_dir0_o 1: Use lp_ck_dir_man0 to be mipi_ck_lp_dir0_o Bit[2]: lp_ck_dir_man0 0: Input 1: Output Bit[1]: lp_ck_p0_o Bit[0]: lp_ck_n0_o
0x483E	FCNT RD H	–	R	Fcnt RD H
0x483F	FCNT RD L	–	R	Fcnt RD L
0x484A	SEL MIPI CTRL4A	0x3F	RW	Bit[7:6]: Not used Bit[5]: slp_lp_pon_man_o Set for power up Bit[4]: slp_lp_pon_da Bit[3]: slp_lp_pon_ck Bit[2]: mipi_slp_man_st MIPI bus status manual control enable in sleep mode Bit[1]: clk_lane_state Bit[0]: data_lane_state
0x484B	MIPI OPTION	0x03	RW	Bit[3]: same_skewcal 0: Initial dskew calibration time controlled by 0x4853, periodic skew calibration time controlled by 0x4852 1: Initial and periodic skew calibration have same calibration time Bit[2]: line_st_sel_o 0: Line starts after HREF 1: Line starts after fifo_st Bit[1]: clk_start_sel_o 0: Clock starts after SOF 1: Clock starts after reset Bit[0]: sof_sel_o 0: Frame starts after HREF occurs 1: Frame starts after SOF

table 5-3 MIPI control registers (sheet 8 of 8)

address	register name	default value	R/W	description
0x484C	MIPI CTRL 4C	0x00	RW	Bit[3]: smia_fcnt_i select Bit[2]: prbs_en Bit[1]: hs_test_only Bit[0]: set_frame_cnt_0
0x484D	TEST PATTEN DATA	0xB6	RW	Bit[7:0]: test_patten_data[7:0] Data lane test pattern
0x484E	FE DLY	0x10	RW	Bit[7:0]: r_fe_dly_o Last packet to frame end delay / 2
0x484F	TEST PATTERN CK DATA	0x55	RW	Bit[7:0]: Clock lane test pattern data

5.2 digital video port (DVP)

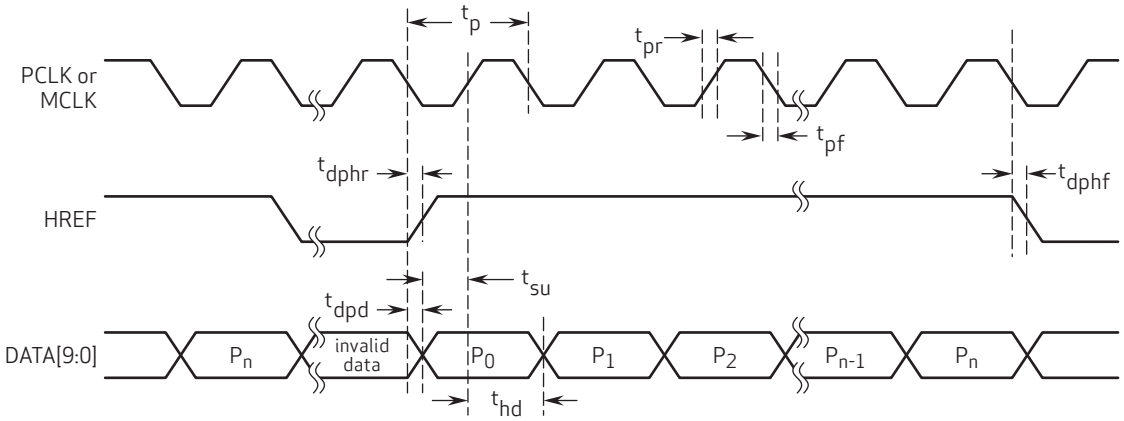
The OG02B1B also supports a DVP interface, which provides 10-bit parallel data output.

table 5-4 supported resolution and frame rate

format[a]	resolution	frame rate	methodology	pixel clock
full resolution	1600x1300	40 fps	full size active	96 MHz

a. all formats with minimum dummy columns and rows

figure 5-4 line/pixel output timing



note n = number of pclks in a line

table 5-5 pixel timing specifications (for PCLK = 96MHz)

symbol	parameter	min	typ	max	unit
t_p	PCLK period[a]		10.416		ns
t_{pr}	PCLK rising time[a]		2		ns
t_{pf}	PCLK falling time[a]		2		ns
t_{dphr}	PCLK negative edge to HREF rising edge	-0.5		-0.7	ns
t_{dphf}	PCLK negative edge to HREF negative edge	-0.2		0.6	ns
t_{dpd}	PCLK negative edge to data output delay	-0.4		1	ns
t_{su}	data bus setup time		4.5		ns
t_{hd}	data bus hold time		4.5		ns

a. PCLK running at 96MHz, C_L = 15pF, and DOVDD = 1.8V

figure 5-5 DVP timing diagram

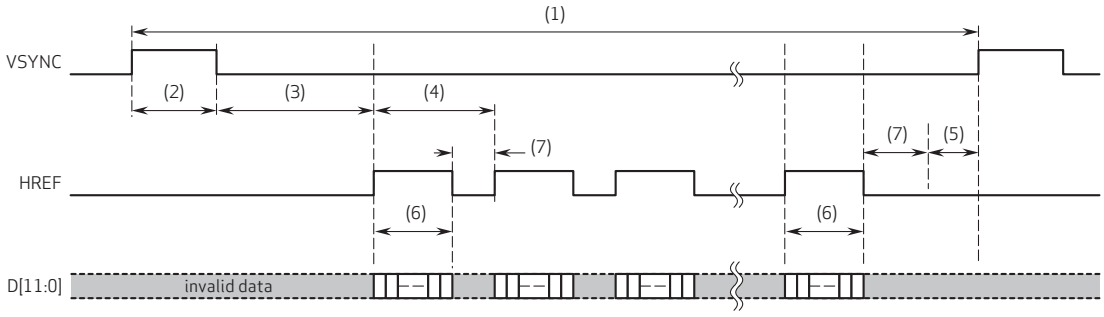


table 5-6 DVP timing specifications

mode	timing
full resolution 1600x1300	(1) v2v: 2,048,688 Tsclk (frame length) (2) v_width: 5,552 Tsclk (3) v2h: 49,684 Tsclk (4) h2h: 1,388 Tsclk (line length) (5) h2v: 189,106 Tsclk (6) h_width: 1,600 Tpclk where Tsclk = 12.5ns/80MHz and Tpclk = 10.416ns/96MHz

note Timing values shown in **table 5-2** may vary depending upon register settings.

table 5-7 DVP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4701	VSYNCOUT_SEL	0x00	RW	Bit[1:0]: VSYNC output select 00: eof_o 01: Output gpo_vsync 10: Output hsync_o 11: eof_o
0x4702	VSYNC_RISE_LNT	0x00	RW	Bit[7:0]: vsync_rise_lnt[15:8] Line counter that controls rising position of VSYNC
0x4703	VSYNC_RISE_LNT	0x02	RW	Bit[7:0]: vsync_rise_lnt[7:0] Line counter that controls rising position of VSYNC
0x4704	VSYNC_FALL_LNT	0x00	RW	Bit[7:0]: vsync_fall_lnt[15:8] Line counter that controls falling position of VSYNC

table 5-7 DVP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4705	VSYNC_FALL_LNT	0x06	RW	Bit[7:0]: vsync_fall_lnt[7:0] Line counter that controls falling position of VSYNC
0x4706	VSYNC_CHG_PCNT	0x00	RW	Bit[7:0]: vsync_chg_pcnt[15:8] VSYNC change position indicated by pixel position
0x4707	VSYNC_CHG_PCNT	0x10	RW	Bit[7:0]: vsync_chg_pcnt[7:0] VSYNC change position indicated by pixel position
0x4708	POLARITY_CTRL	0x09	RW	Bit[7]: Clock DDR mode enable Bit[6]: hts_man_en Bit[5]: VSYNC gate enable Bit[4]: HREF gate enable Bit[3]: r_fo_nofrst Bit[2]: HREF polarity Bit[1]: VSYNC polarity Bit[0]: PCLK polarity
0x4709	BIT_TEST_ORDER	0x00	RW	Bit[6:4]: Data bit swap
0x470C	R_READ_CTRL	0x81	RW	Bit[1]: first_lv_sel Bit[0]: r_lpcnt_free
0x470F	BYP_SEL	0x00	RW	Bit[4]: href_sel Bit[3:0]: bypass_sel

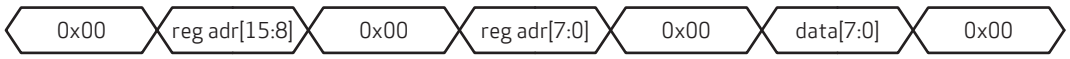
5.3 embedded line

The OG02B1B supports embedded line output in MIPI mode.

Embedded lines can be output after internal SOF. The MIPI receiver will see embedded lines after "frame start" short packet. The number of embedded lines can be programmed from 1 line to 15 lines. Group and embedded lines share the register bus so it is necessary to avoid two operations from occurring at the same time. Please avoid group operation between SOF and first image line.

The contents of the embedded lines are 16-bit registers addresses and the 8-bit values stored at the addresses. One byte data of "0" is inserted between every two bytes of embedded data.

figure 5-6 embedded line data without tag data



The related control registers are shown in **table 5-8**.

table 5-8 embedded line registers

address	register name	default value	R/W	description
0x3214	GROUP LENGTH4	–	R	Group4 Register Number
0x3216	EMB_LINE_NUM	0x01	RW	Bit[3:0]: Embedded line number
0x3217	PADDING_DATA	0x00	RW	Bit[3:0]: Tag
0x3218	EMBED_LINE_CTRL	0x00	RW	Bit[7:6]: emb_ln_blk_ctrl Bit[5]: embline_addr_en Bit[4]: embline_tag_en Bit[3]: frame_trig_sel 0: tc_grp_wr 1: EOF Bit[2]: Debug mode Bit[1]: embline_sof_en Bit[0]: Debug mode

The registers to be sent out through embedded lines are specified by group recording. The "value" following the register address is no longer the register value, but the number of registers to send out starting from that address. Refer to the following example.

```
C0 3208 04 ;start recording the registers to be sent out through embedded line
C0 3D81 01 ;one register starting from address 0x3D81
C0 4605 02 ;two registers starting from address 0x4605
C0 4816 0A ;ten registers starting from address 0x4816
C0 3208 14 ;finish recording
```

Group 4 is used to specify the list of registers for embedded line at the beginning of each frame.

The following are two examples to output one embedded line at the beginning of each frame.

Example 1 – embedded line with RAW10 output

```
C0 3016 F1
C0 0100 01
C0 4814 6B ;dt_man en, both embed/image data type are 0x2B
C0 3218 32
C0 3216 01
C0 3208 04
C0 3D81 01
C0 4605 02
C0 4816 0A
C0 3208 14
C0 3662 65 ; [1] raw10
C0 366F 1A ; [6] MSB
C0 3674 11 ; [0] embed_en, add embed data before normal image
C0 3016 F0
```

Note that under MIPI RAW10, if set to auto mode (0x4814[6] = 0), the embedded line data type is fixed to 0x12. While it still outputs with 10-bit, use 0x366F[6] to select MSB or LSB, and receive the correct 8-bit embedded data.

Example 2 – embedded line with RAW8 output

```
C0 3016 F1
C0 0100 01
C0 4814 6A ; dt_man en, both embed/image data type are 0x2A
C0 3218 32
C0 3216 01
C0 3208 04
C0 3D81 01
C0 4605 02
C0 4816 0A
C0 3208 14
C0 3662 67 ; [1] raw8
C0 366F 1A ; [6] MSB
C0 3674 11 ; [0] embed_en, add embed data before normal image
C0 3016 F0
```

Note that under MIPI RAW8, if set to auto mode (0x4814[6] = 0), the embedded line data type is fixed to 0x12. Please set 0x366F[6] = 0 (MSB enable) to correct output for 8-bit embedded data.

6 serial camera control bus (SCCB) interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

The OG02B1B responds to two SCCB ID, one is set by register SC_SCCB_ID0 (default 0x20) or register SC_SCCB_ID1 (default 0xC0), the other is set by register SC_SCCB_ID2 (default 0xE0). When SID pin is low, SC_SCCB_ID1 value is selected as the first SCCB ID. When SID pin is high, SC_SCCB_ID0 value is selected as the first SCCB ID. These ID's are all programmable. In a multi-sensor system, SC_SCCB ID2 can be used as a broadcasting ID to allow programming registers to all sensors simultaneously, and the other SCCB ID can be used as a unique ID to access each individual sensor.

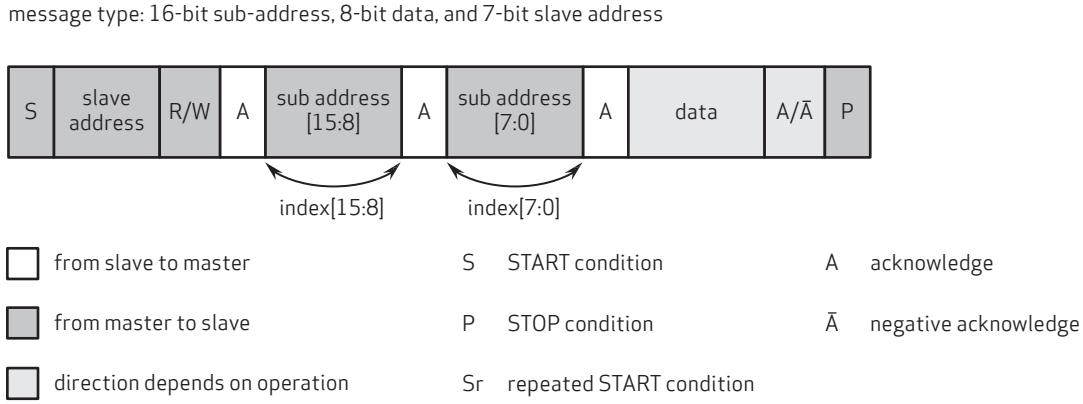
6.1 data transfer protocol

Data transfer of the OG02B1B follows SCCB protocol.

6.2 message format

The OG02B1B supports the message format shown in **figure 6-1**. The repeated START (Sr) condition is not shown in SCCB single read from random location, but is shown in SCCB single read from current location and SCCB sequential read from random location.

figure 6-1 message type



6.3 read / write operation

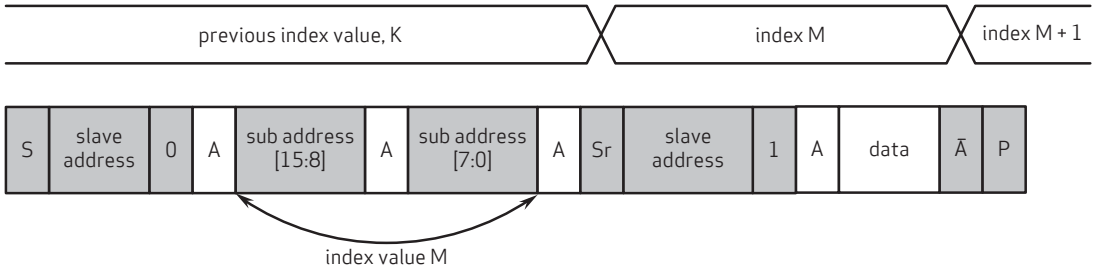
The OG02B1B supports four different read operations and two different write operations:

- a single read from random locations
- a sequential read from random locations
- a single read from current location
- a sequential read from current location
- single write to random locations
- sequential write starting from random location

The sub-address in the sensor automatically increases by one after each read/write operation.

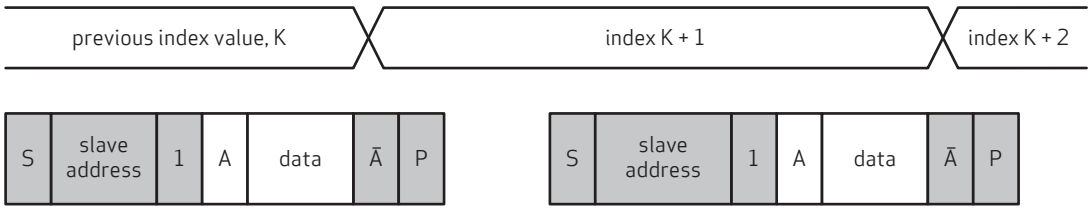
In a single read from random locations, the master does a dummy write operation to desired sub-address, issues a repeated start condition and then addresses the camera again with a read operation. After acknowledging its slave address, the camera starts to output data onto the SDA line as shown in **figure 6-2**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 6-2 SCCB single read from random location



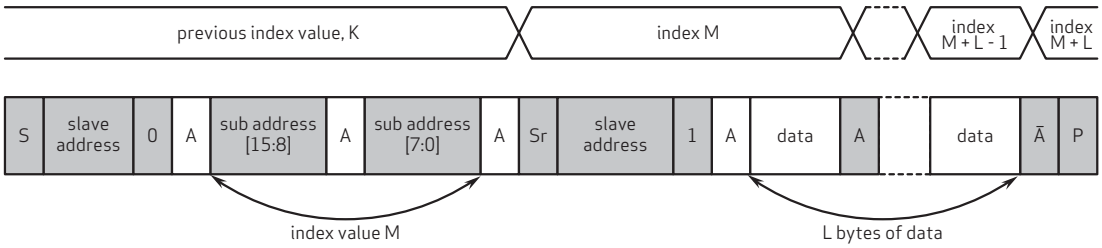
If the host addresses the camera with read operation directly without the dummy write operation, the camera responds by setting the data from last used sub-address to the SDA line as shown in **figure 6-3**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 6-3 SCCB single read from current location



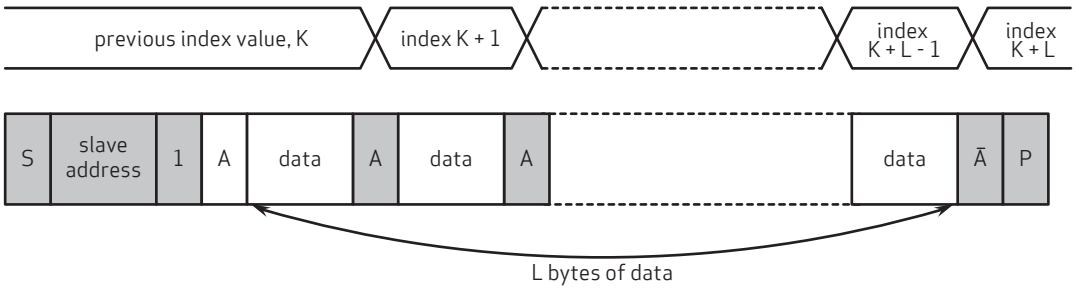
The sequential read from a random location is illustrated in **figure 6-4**. The master does a dummy write to the desired sub-address, issues a repeated start condition after acknowledge from slave and addresses the slave again with read operation. If a master issues an acknowledge after receiving data, it acts as a signal to the slave that the read operation shall continue from the next sub-address. When master has read the last data byte, it issues a negative acknowledge and stop condition.

figure 6-4 SCCB sequential read from random location



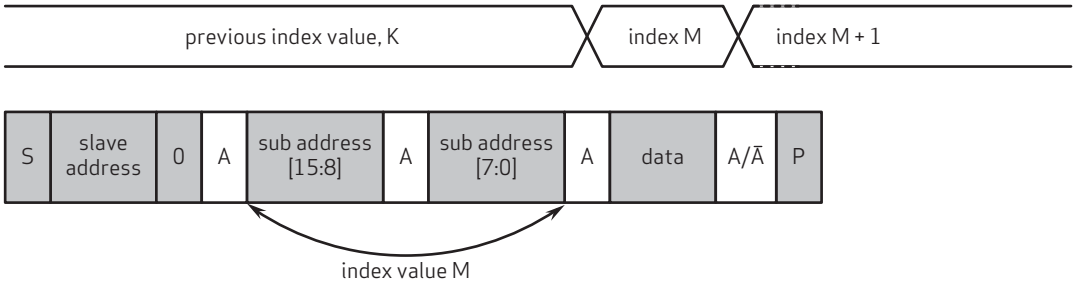
The sequential read from current location is similar to a sequential read from a random location. The only exception is that there is no dummy write operation as shown in **figure 6-5**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 6-5 SCCB sequential read from current location



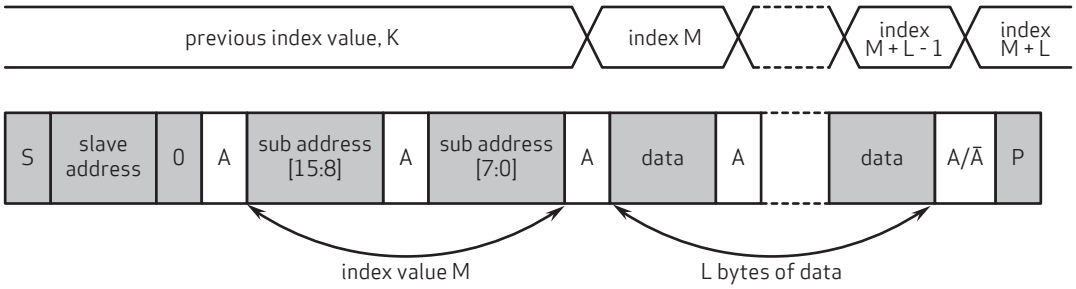
The write operation to a random location is illustrated in **figure 6-6**. The master issues a write operation to the slave, sets the sub-address and data correspondingly after the slave has acknowledged. The write operation is terminated with a stop condition from the master.

figure 6-6 SCCB single write to random location



The sequential write is illustrated in **figure 6-7**. The slave automatically increments the sub-address after each data byte. The sequential write operation is terminated with stop condition from the master.

figure 6-7 SCCB sequential write to random location



6.4 SCCB timing

figure 6-8 SCCB interface timing

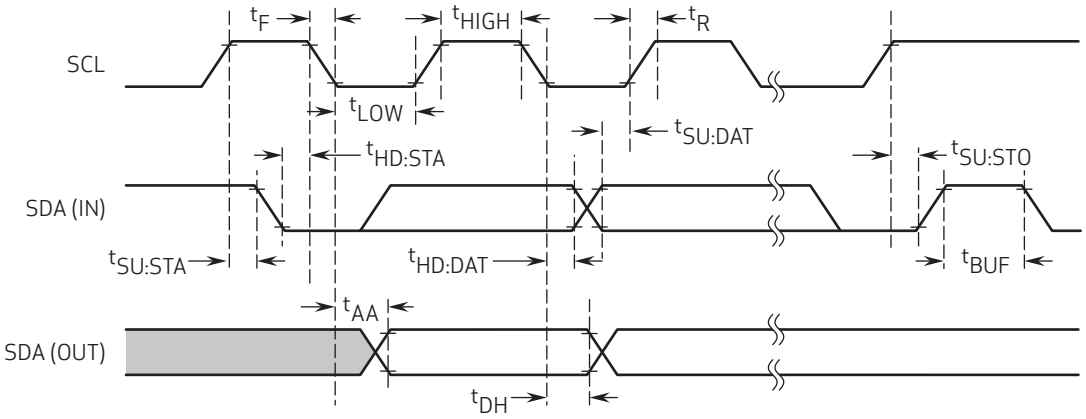


table 6-1 SCCB interface timing specifications[ab]

symbol	parameter	min	typ	max	unit
f_{SCL}	clock frequency			400	kHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SCL low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	0.6			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs
t_{DH}	data out hold time	0.05			µs

a. SCCB timing is based on 400kHz mode

b. timing measurement shown at beginning of rising edge or end of falling edge signifies 30%,
timing measurement shown in middle of rising/falling edge signifies 50%,
timing measurement shown at end of rising edge or beginning of falling edge signifies 70%

7 one-time programmable (OTP) memory

The OG02B1B has 128 bytes embedded one time programmable (OTP) memory. The OTP memory can be programmed and read back via SCCB bus. This document provides general guidelines for programming and accessing the OTP memory.

7.1 OTP memory structure

108 bytes of OTP memory are reserved for OmniVision internal use. These bytes are usually used to store product information or used by some internal functions. The remaining 20 bytes are fully user programmable. The user can store production tracking information, camera module calibration data, etc. to these bytes.

table 7-1 OTP memory structure

start address	end address	byte usage	assignment	byte type
0x7000	0x7017	24	reserved for OmniVision	data
0x7018	0x702B	20	reserved for customer	data
0x702C	0x707F	84	reserved for OmniVision	data

7.2 accessing OTP memory

The OG02B1B supports one-time programmable (OTP) memory to store chip identification and manufacturing information, which can be used to update the sensor's default setting and can be controlled through the SCCB (see **table 7-2**).

There is a dedicated 128 byte buffer, which is used to temporarily store data to be programmed (written) in to OTP or loaded (read) form OTP. Addresses for this OTP buffer ranges from 0x7000 to 0x707F.

The OTP memory access conditions are based on typical conditions: 1ms after sensor streaming, 2.8~3.0V AVDD, 1.2V DVDD, and 80 MHz system clock.

OTP write in partial mode example:

```
C0 3D84 40; [6]partial mode enable
C0 3D85 00
C0 3D88 70 ;; partial mode OTP write start address high byte
C0 3D89 38 ;; partial mode OTP write start address low byte
C0 3D8A 70 ;; partial mode OTP write end address high byte
C0 3D8B 7F ;; partial mode OTP write end address low byte
           ;; It is 707F in this example
C0 7038 xx ;; Data[0]
C0 7039 xx ;; Data[1]
```

```
C0 703A xx ;; Data[2]
C0 703B xx ;; Data[3]
C0 703C xx ;; Data[4]
…
…
C0 707F xx ;; Data[1023]
C0 3D80 01 ;[0] program enable
```

OTP read example:

```
C0 3D84 40; [6]partial mode enable
C0 3D88 70 ;; partial mode OTP write start address high byte
C0 3D89 38 ;; partial mode OTP write start address low byte
C0 3D8A 70 ;; partial mode OTP write end address high byte
C0 3D8B 7F ;; partial mode OTP write end address low byte
C0 3D81 01 ;; OTP read enable
```

To use OTP memory under different operating conditions, please contact your local OmniVision FAE.

table 7-2 OTP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3D80	OTP_PROGRAM_CTRL	–	RW	Bit[7]: OTP_wr_busy (read only) Bit[0]: OTP_program_enable (write only)
0x3D81	OTP_LOAD_CTRL	–	RW	Bit[7]: OTP_rd_busy (read only) Bit[5]: OTP_bist_error (read only) Bit[4]: OTP_bist_done (read only) Bit[2]: bist_result_clr (write only) Bit[1]: autoload_m (write only) Bit[0]: OTP_load_enable (write only)
0x3D82	OTP_PGM_PULSE	0x65	RW	Program Strobe Pulse Width Unit: 8×system Clock Period
0x3D83	OTP_LOAD_PULSE	0x06	RW	Load Strobe Pulse Width Unit: System Clock Period
0x3D84	OTP_MODE_CTRL	0x00	RW	Bit[7]: Program disable 0: Not used 1: Disable Bit[6]: Mode select 0: Auto mode 1: Manual mode Bit[0]: bank_sram_switch

table 7-2 OTP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3D85	OTP_REG85	0x1B	RW	Bit[6]: OTP BIST compare value Bit[5]: OTP BIST mode select Bit[4]: OTP BIST enable
0x3D86	SRAM_TEST_ SIGNALS	0x0F	RW	Bit[4]: sram_TEST Bit[2:0]: sram_RM
0x3D87	OTP_PS2CS	0x0A	RW	OTP PS to CSB Delay Unit: System Clock Period
0x3D88	OTP_START_ ADDRESS	0x00	RW	OTP Start High Address for Manual Mode
0x3D89	OTP_START_ ADDRESS	0x00	RW	OTP Start Low Address for Manual Mode
0x3D8A	OTP_EN_ADDRESS	0x00	RW	OTP End High Address for Manual Mode
0x3D8B	OTP_END_ADDRESS	0x00	RW	OTP End Low Address for Manual Mode
0x3D8E	OTP_BIST_ERR_ ADDRESS	–	R	OTP Check Error Address High
0x3D8F	OTP_BIT_ERR_ADDRESS	–	R	OTP Check Error Address Low

7.2.1 procedure for accessing OTP memory

Since the OTP memory can only be programmed once, the user should be very careful when accessing the OTP. Here is a detailed procedure for OTP access.

7.2.2 procedure to read OTP content

1. Clear software buffer which is to receive the OTP content.
2. Configure PLL and set register 0x100 to 1 if not yet set.
3. Set register 0x3D81 to 0x01.
4. Wait 15ms.
5. Read register 0x7000~0x707F and set to the software buffer.

The OTP read operation is performed to verify the OTP memory is blank before program data to it, or to verify OTP contents after programming data to it.

Verifying the OTP content at the last step of camera module testing is highly recommended in case the OTP content is accidently overwritten during the module testing.

7.2.3 procedure to program OTP content

1. Follow **procedure to read OTP content** to make sure the OTP to be programmed is blank.
2. Program the intended OTP content to its corresponding register buffer, and clear unused register buffer to 0.
   a. For customer - registers 0x7000~0x707F must be cleared to 0x00 before initiating the OTP programming command
3. Read back registers 0x7000~0x707F to make sure they are the correct data to program to OTP memory or 0 for all other bits.
4. Write 0x01 to register 0x3D80 to initiate OTP programming.
5. Wait 15ms, any register access during this period is prohibited.
6. Follow **procedure to read OTP content** to read back the OTP content.
7. Compare the OTP content read back to the intended OTP content.

7.3 power supply requirement for OTP memory programming

The OTP memory is programmed using the analog power. The AVDD voltage for OTP programming must be 2.6V ~ 3.0V. The power supply should be able to provide extra 50mA for OTP programming.

8 operating specifications

8.1 absolute maximum ratings

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

8.2 functional temperature

table 8-2 functional temperature

parameter	range
operating temperature[a]	-30°C to +85°C junction temperature
stable image temperature[b]	0°C to +50°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

8.3 DC characteristics

table 8-3 DC characteristics (-30°C < T_J < 85°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	2.7	2.8	3.0	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	3.0	V
V_{DD-D}	supply voltage (digital core)	1.14	1.2	1.26	V
I_{DD-A}			32	40	mA
I_{DD-IO}	active (operating) current[a]		1	2	mA
I_{DD-D}			80	125	mA
$I_{DDS-XSHUTDOWN}$	standby current		1	25	µA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.2V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[b]	SCL and SDA	-0.5	0	0.54	V
V_{IH}[b]	SCL and SDA	1.28	1.8	3.0	V

a. 1600x1300 @ 60fps

b. based on DOVDD = 1.8V

8.4 timing characteristics

figure 8-1 reference clock input timing diagram

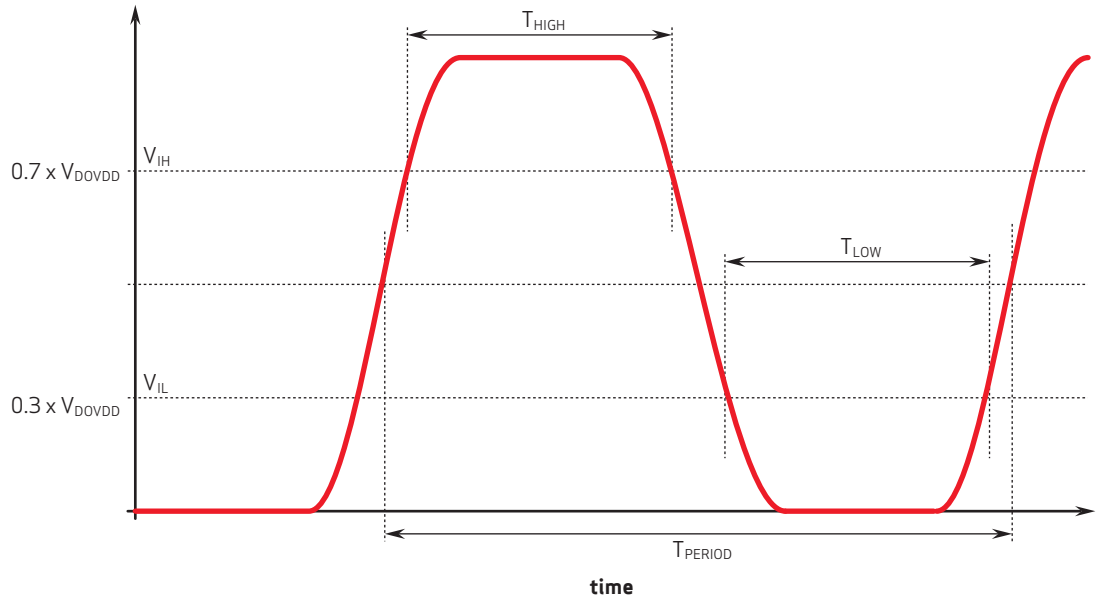


table 8-4 timing characteristics

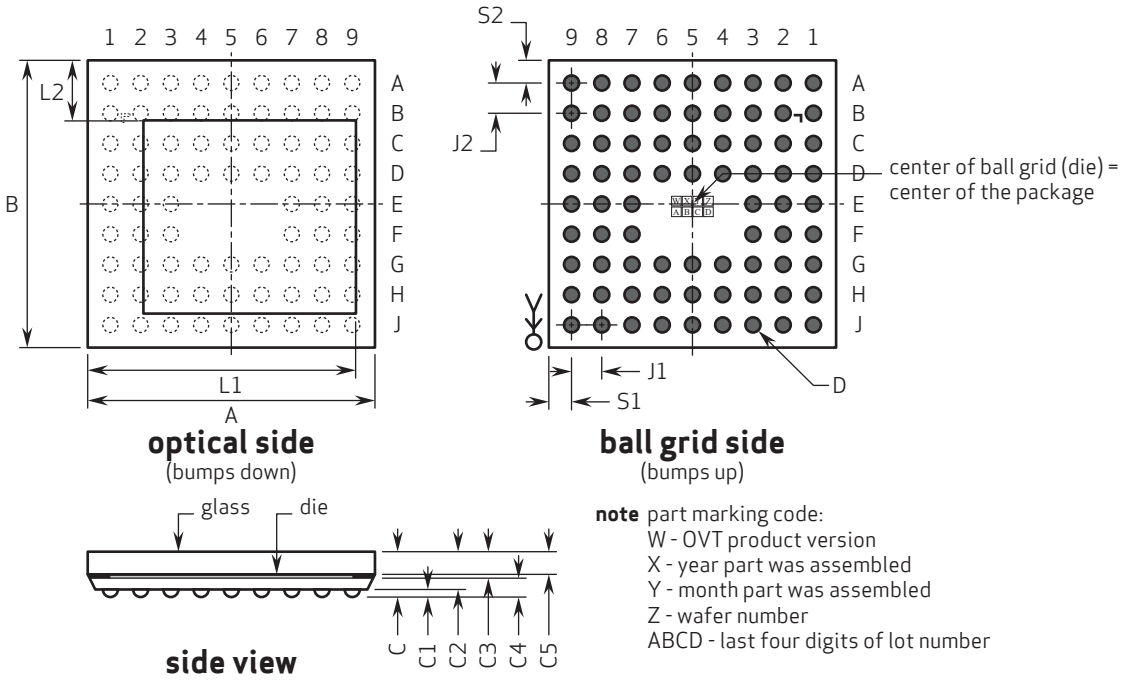
symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{XVCLK}	frequency (XVCLK)[a]	6	24	27	MHz
T_{PERIOD}	period (XVCLK)	37.0	41.7	166.7	ns
T_{LOW}	low level width (XVCLK)	0.35×T_{PERIOD}		0.65×T_{PERIOD}	ns
T_{HIGH}	high level width (XVCLK)	0.35×T_{PERIOD}		0.65×T_{PERIOD}	ns

a. for input clock range 6~27 MHz, the OG02B1B can tolerate input clock period jitter up to 600ps peak-to-peak

9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications



note part marking code:
W - OVT product version
X - year part was assembled
Y - month part was assembled
Z - wafer number
ABCD - last four digits of lot number

table 9-1 package dimensions (sheet 1 of 2)

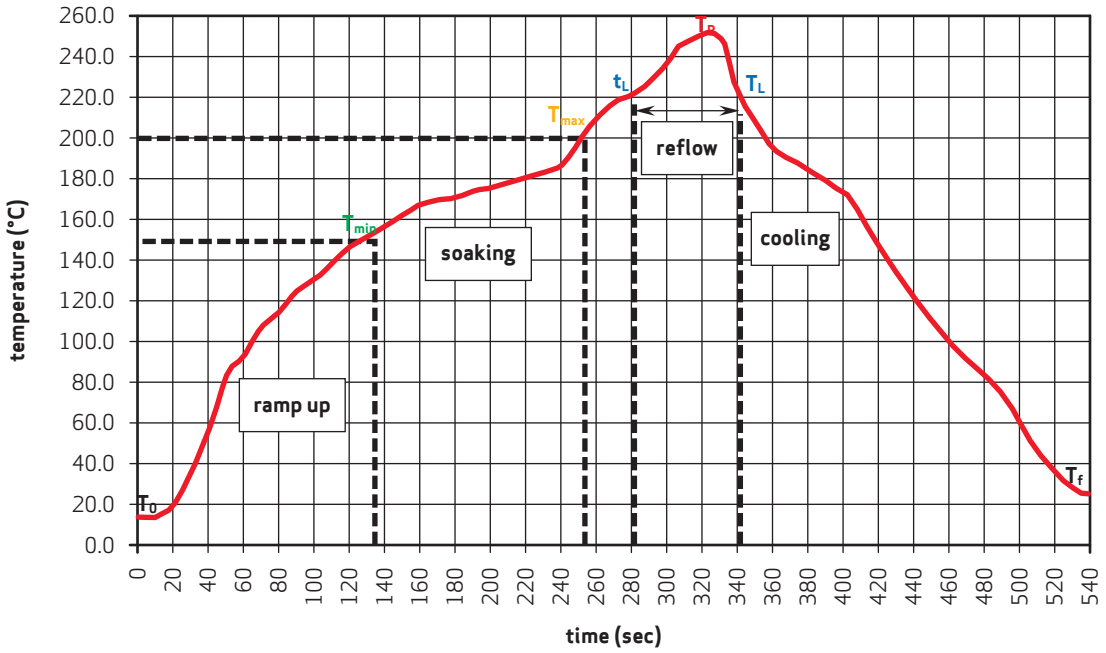
parameter	symbol	min	typ	max	unit
package body dimension x	A	7194	7219	7244	µm
package body dimension y	B	6132	6157	6182	µm
package height	C	795	855	915	µm
ball height	C1	195	225	255	µm
package body thickness	C2	585	630	675	µm
thickness from top glass surface to wafer	C3	425	445	465	µm
image plane height	C4	355	410	465	µm
glass thickness	C5	390	400	410	µm
ball diameter	D	295	325	355	µm

table 9-1 package dimensions (sheet 2 of 2)

parameter	symbol	min	typ	max	unit
total pin count	N		75 (12 NC)		
pin count x-axis	N1		9		
pin count y-axis	N2		9		
pins pitch x-axis	J1		700		µm
pins pitch y-axis	J2		630		µm
pixel to package edge dimension A	L1	6414.648	6449.648	6484.648	µm
pixel to package edge dimension B	L2	1350.852	1385.852	1420.852	µm
edge-to-pin center distance along x	S1	779.5	809.5	839.5	µm
edge-to-pin center distance along y	S2	528.5	558.5	588.5	µm
air gap between sensor and glass		40	45	50	µm
tilt between die and cover glass				0.15	degree
die rotation				0.1	degree

9.2 IR reflow specifications

figure 9-2 IR reflow ramp rate requirements



note The OG02B1B uses a lead free package.

note OmniVision recommends CSP packages use underfill as a part of camera assembly process.

table 9-2 reflow conditions[ab]

zone	description	exposure
ramp up A (T_0 to T_{min})	heating from room temperature to 150°C	temperature slope ≤ 3°C per second
soaking	heating from 150°C to 200°C	90 ~ 150 seconds
ramp up B (t_L to T_p)	heating from 217°C to 245°C	temperature slope ≤ 3°C per second
peak temperature	maximum temperature in SMT	245°C +0/-5°C (duration max 30 sec)
reflow (t_L to T_L)	temperature higher than 217°C	30 ~ 120 seconds
ramp down A (T_p to T_L)	cooling from 245°C to 217°C	temperature slope ≤ 3°C per second
ramp down B (T_L to T_f)	cooling from 217°C to room temperature	temperature slope ≤ 2°C per second
T_0 to T_p	room temperature to peak temperature	≤ 8 minutes

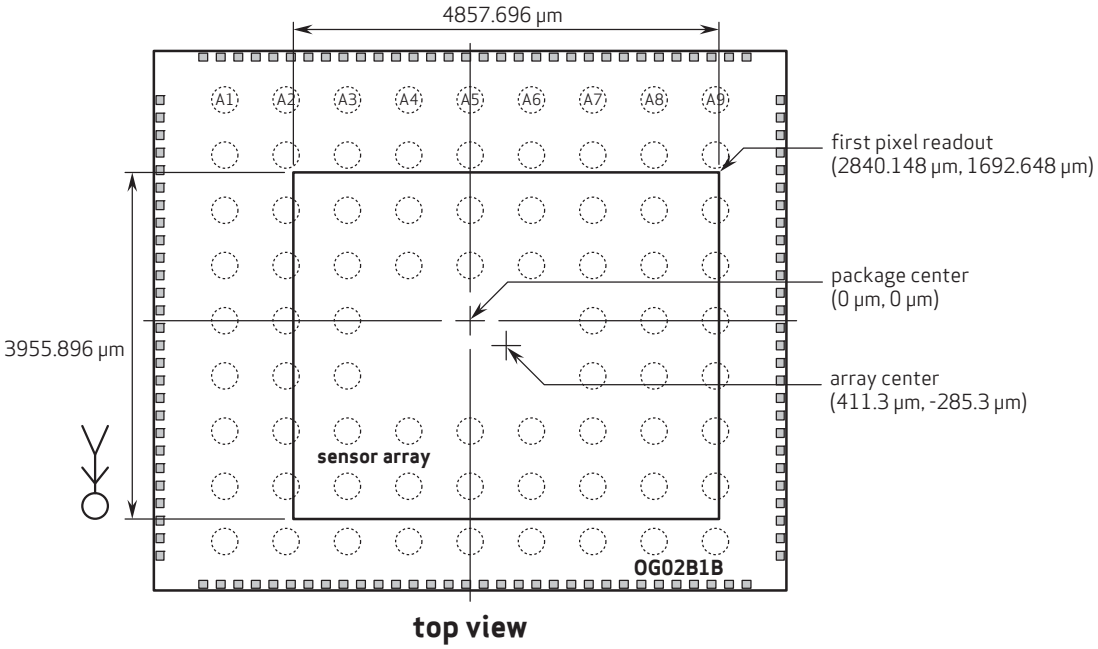
a. maximum number of reflow cycles = 3

b. N2 gas reflow or control O2 gas PPM<500 as recommended

10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pin A1 oriented down on the PCB.

10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)

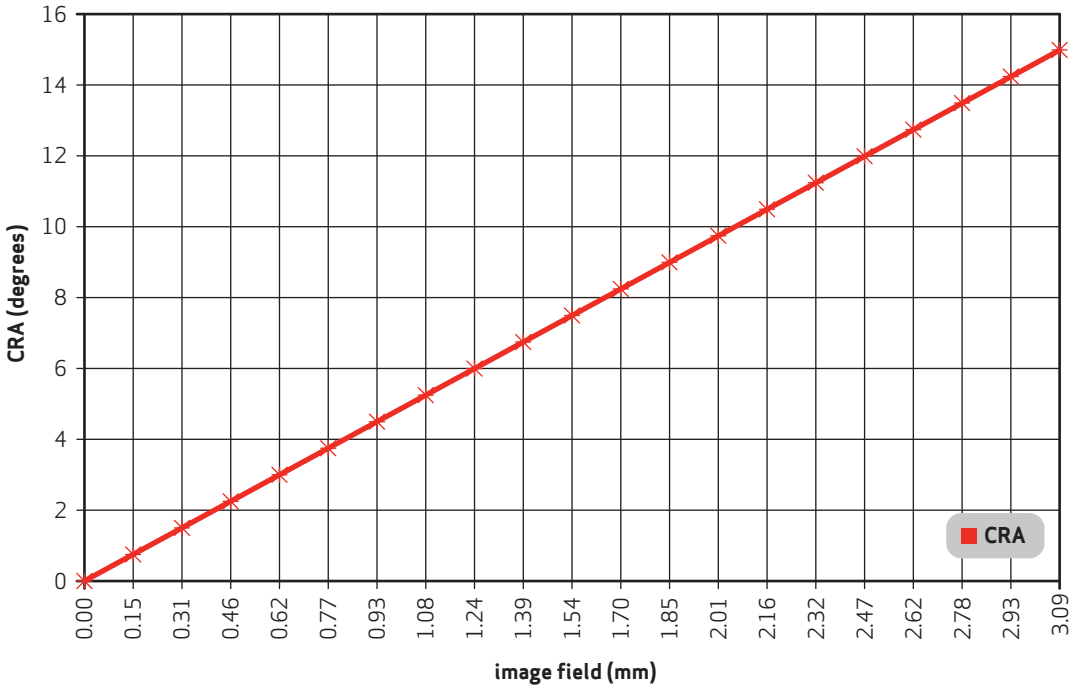


table 10-1 CRA versus image height plot (sheet 1 of 2)

field (%)	image height (mm)	CRA (degrees)
0.00	0.00	0.00
0.05	0.15	0.75
0.10	0.31	1.50
0.15	0.46	2.25
0.20	0.62	3.00
0.25	0.77	3.75
0.30	0.93	4.50
0.35	1.08	5.25
0.40	1.24	6.00
0.45	1.39	6.75

table 10-1 CRA versus image height plot (sheet 2 of 2)

field (%)	image height (mm)	CRA (degrees)
0.50	1.54	7.50
0.55	1.70	8.25
0.60	1.85	9.00
0.65	2.01	9.75
0.70	2.16	10.50
0.75	2.32	11.25
0.80	2.47	12.00
0.85	2.62	12.75
0.90	2.78	13.50
0.95	2.93	14.25
1.00	3.09	15.00

10.3 IR cut off wavelength

Wavelength above 975nm must be cut off for both monochrome and color sensors to avoid package structure ghosting. For color sensors, it is recommended to cut wavelength at 650nm or shorter for good color reproduction.

appendix A register table

A.1 module name and address range

table A-1 module name and address range

module name	address range
SYSTEM	0x0100~0x010C
PLL	0x0300~0x0319
SC	0x3000~0x303F
SCCB	0x3100~0x31FF
GROUP HOLD	0x3200~0x321F
AEC_PK	0x3501~0x3525
ANA CONTROL	0x3600~0x36D1
SENSOR CONTROL	0x3700~0x37EF
TIMING	0x3800~0x383D
GLOBAL SHUTTER	0x3880~0x3933
OTP	0x3D80~0x3D95
BLC	0x4000~0x4049
ISP_FC	0x4240~0x4244
FORMAT	0x4300~0x4329
TPM	0x4400~0x4424
FC	0x4440~0x444B
COLUMN_SYNC	0x4500~0x450F
VFIFO	0x4600~0x4606
DVP	0x4700~0x4711
MIPI	0x4800~0x484F
PSV	0x4F00~0x4F14
ISP_MAIN	0x5000~0x5036
ISP_WIN	0x5A00~0x5A2F
ISP_DPC	0x5B00~0x5B35
ISP_OTP_DPC	0x5C00~0x5C23
ISP_GAIN_FMT	0x5D06~0x5D0B
ISP_PRE	0x5E00~0x5E2E
ISP_DGC_COMP	0x5F00~0x5F05

A.2 device control registers

The following tables provide descriptions of the device control registers contained in the OG02B1B. For all register enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0xC0 for write and 0xC1 for read.

A.2.1 system [0x0100, 0x0103, 0x0106 - 0x010C]

table A-2 system control registers

address	register name	default value	R/W	description
0x0100	MODE SELECT	0x00	RW	Bit[7:1]: Not used Bit[0]: Streaming 0: software_standby 1: streaming
0x0103	SOFTWARE RESET	–	W	Bit[7:1]: Not used Bit[0]: sw_reset 0: Off 1: On
0x0106	FAST STANDBY CTRL	0x01	RW	Bit[7:1]: Not used Bit[0]: fast_standby 0: Frame completes before mode entry 1: Frame may be truncated before mode end
0x0107	SC_SCCB_ID0	0x20	RW	SCCB Slave 20
0x0108	DEBUG MODE	–	–	Debug Mode
0x0109	SC_SCCB_ID1	0xC0	RW	SCCB Slave C0
0x010A	DEBUG	–	–	Debug
0x010B	ENTER SOFTWARE STANDBY	0x00	RW	Bit[7:1]: Not used Bit[0]: Enter software standby 0: Keep 1: Enter software standby
0x010C	ENTER SAFE MODE	0x00	RW	Bit[7:1]: Not used Bit[0]: Enter safe mode 0: Keep 1: Enter safe mode

A.2.2 PLL [0x0300 - 0x0319]

table A-3 PLL control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x0300	PLL_CTRL_00	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: pll1_prediv
0x0301	PLL_CTRL_01	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: pll1_mult[9:8]
0x0302	PLL_CTRL_02	0x32	RW	Bit[7:0]: pll1_mult[7:0]
0x0303	PLL_CTRL_03	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: pll1_divm
0x0304	PLL_CTRL_04	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: pll1_div_mipi
0x0305	PLL_CTRL_05	0x02	RW	Bit[7:2]: Reserved Bit[1:0]: pll1_divsp
0x0306	PLL_CTRL_06	0x01	RW	Bit[7:1]: Reserved Bit[0]: pll1_divs
0x0307	PLL_CTRL_07	0x00	RW	Bit[7:1]: Reserved Bit[0]: pll1_div_rst_sync
0x0308	PLL_CTRL_08	0x00	RW	Bit[7:1]: Reserved Bit[0]: pll1_bypass
0x0309	PLL_CTRL_09	0x09	RW	Bit[7:6]: pll1_precision Bit[5:4]: pll1_cnt_ref Bit[3]: pll1_lock_det_en Bit[2:0]: pll1_cp
0x030A	PLL_CTRL_0A	0x00	RW	Bit[7:1]: Reserved Bit[0]: pll1_predivp
0x030B	PLL_CTRL_0B	0x04	RW	Bit[7:3]: Reserved Bit[2:0]: pll2_prediv
0x030C	PLL_CTRL_0C	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: pll2_mult[9:8]
0x030D	PLL_CTRL_0D	0x5A	RW	Bit[7:0]: pll2_mult[7:0]
0x030E	PLL_CTRL_0E	0x04	RW	Bit[7:3]: Reserved Bit[2:0]: pll2_divs
0x030F	PLL_CTRL_0F	0x02	RW	Bit[7:4]: Reserved Bit[3:0]: pll2_divsp
0x0310	PLL_CTRL_10	0x09	RW	Bit[7:6]: pll2_precision Bit[5:4]: pll2_cnt_ref Bit[3]: pll2_lock_det_en Bit[2:0]: pll2_cp

table A-3 PLL control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x0311	PLL_CTRL_11	0x00	RW	Bit[7:1]: Reserved Bit[0]: pll2_bypass
0x0312	PLL_CTRL_12	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: pll2_div_sa1
0x0313	PLL_CTRL_13	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: pll2_div_dac
0x0314	PLL_CTRL_14	0x00	RW	Bit[7:1]: Reserved Bit[0]: pll2_predivp
0x0315	PLL_CTRL_15	0x00	RW	Bit[7:1]: Reserved Bit[0]: pll2_div_rst_sync
0x0316~ 0x0317	RSVD	–	–	Reserved
0x0318	PLL_CTRL_18	0x00	RW	Bit[7:1]: Reserved Bit[0]: pll1_rst_o
0x0319	PLL_CTRL_19	0x00	RW	Bit[7:1]: Reserved Bit[0]: pll2_rst_o

A.2.3 SC [0x3000 - 0x303F]

table A-4 SC registers (sheet 1 of 9)

address	register name	default value	R/W	description
0x3000	RSVD	–	–	Reserved
0x3001	SC_CTRL_01	0x02	RW	Bit[7]: pd_data_en Bit[6]: pd_data_en Bit[5:0]: pd_pk
0x3002	SC_CTRL_02	–	R	Bit[7:0]: dvp_prbs_chk_err
0x3003	SC_CTRL_03	–	R	Bit[7:5]: Reserved Bit[4]: dvp_prbs_err_real Bit[3:2]: Reserved Bit[1]: pll1_freq_match Bit[0]: pll2_freq_match
0x3004	SC_CTRL_04	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: io_pad_out_en[17:16]
0x3005	SC_CTRL_05	0x00	RW	Bit[7:0]: io_pad_out_en[15:8]
0x3006	SC_CTRL_06	0x04	RW	Bit[7:0]: io_pad_out_en[7:0]

table A-4 SC registers (sheet 2 of 9)

address	register name	default value	R/W	description
0x3007	SC_CTRL_07	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: io_pad_out[17:16]
0x3008	SC_CTRL_08	0x00	RW	Bit[7:0]: io_pad_out[15:8]
0x3009	SC_CTRL_09	0x00	RW	Bit[7:0]: io_pad_out[7:0]
0x300A~ 0x300B	RSVD	–	–	Reserved
0x300C	SC_CTRL_0C	–	R	version_id
0x300D	SC_CTRL_0D	0x00	RW	Bit[7]: gclk_embline Bit[6]: gclk_dpcm Bit[5]: gclk_testmode Bit[4]: gclk_smia Bit[3]: gclk_otp Bit[2]: Reserved Bit[1]: gclk_mipi Bit[0]: gclk_dvp
0x300E	SC_CTRL_0E	0x00	RW	Bit[7]: gclk_vfifo Bit[6]: Reserved Bit[5]: gclk_isp Bit[4]: gclk_blc Bit[3]: Reserved Bit[2]: gclk_aec Bit[1]: gclk_stb Bit[0]: gclk_fc
0x300F	SC_CTRL_0F	0xF0	RW	Bit[7]: Reserved Bit[6]: daclk_en Bit[5:4]: sramclk_o divider 00: /1 01: /2 10: /4 11: /1 Bit[3:0]: Reserved
0x3010	SC_CTRL_10	0xC1	RW	Bit[7]: scale_div_man_en Bit[6]: daclk_en Bit[5:4]: daclk_sel (divider) 00: /1 01: /2 10: /4 11: /1 Bit[3]: Reserved Bit[2:0]: pll_scale_div

table A-4 SC registers (sheet 3 of 9)

address	register name	default value	R/W	description
0x3011	SC_CTRL_11	0x08	RW	Bit[7]: hstx_open_term Bit[6:5]: d1_skew Bit[4]: pllclk_out_enable Bit[3]: mipi_pad Bit[2:0]: pgm_vcm High speed common mode voltage
0x3012	SC_MIPI_PHY0	0x70	RW	Bit[7:4]: sel_drv Bit[3:2]: ck_skew Bit[1:0]: d0_skew
0x3013	SC_MIPI_PHY1	0x10	RW	Bit[7]: lp_sr Bit[6]: pgm_bp_hs_en_lat Bit[5:4]: pgm_lptx 01: Driving strength of low speed transmitter Bit[3:2]: r_iref Bit[1:0]: Bit select
0x3014	SC_MIPI_SC_CTRL0	0x04	RW	Bit[7:6]: mipi_ck_skew_o Bit[5]: mipi_phy_rst_o Bit[4]: r_phy_pd_mipi 0: Not used 1: Power down PHY HS TX Bit[3]: r_phy_pd_lprx 0: Not used 1: Power down PHY LP RX module Bit[2]: mipi_en 0: DVP enable 1: MIPI enable Bit[1]: mipi_susp_reg MIPI system suspend register 0: Not used 1: Suspend Bit[0]: lane_dis_op 0: Use mipi_release1/2 and lane_disable1/2 to disable two data lane 1: Use lane_disable1/2 to disable two data lane
0x3015	SC_MIPI_SC_CTRL1	0x10	RW	Bit[7:0]: MIPI ULPS resume mark1 detect length

table A-4 SC registers (sheet 4 of 9)

address	register name	default value	R/W	description
0x3016	SC_CLKRST0	0xF0	RW	Bit[7]: sclk_fc Bit[6]: sclk_stb Bit[5]: sclk_aec Bit[4]: sclk_tc Bit[3]: rst_fc Bit[2]: rst_stb Bit[1]: rst_aec Bit[0]: rst_tc
0x3017	SC_CLKRST1	0xF0	RW	Bit[7]: sclk_blc Bit[6]: sclk_isp Bit[5]: sclk_psv_ctrl Bit[4]: sclk_vfifo Bit[3]: rst_blc Bit[2]: rst_isp Bit[1]: rst_psv_ctrl Bit[0]: rst_vfifo
0x3018	SC_CLKRST2	0xF0	RW	Bit[7]: pclk_dvp Bit[6]: sclk_mipi Bit[5]: sclk_ac Bit[4]: sclk_otp Bit[3]: rst_dvp Bit[2]: rst_mipi Bit[1]: rst_ac Bit[0]: rst_otp
0x3019	SC_CLKRST3	0xF0	RW	Bit[7]: sclk_smia Bit[6]: sclk_testmode Bit[5]: sclk_dpcm Bit[4]: sclk_embline Bit[3]: rst_smia Bit[2]: rst_testmode Bit[1]: rst_dpcm Bit[0]: rst_embline
0x301A	SC_CLKRST4	0xF0	RW	Bit[7]: sdclk_sd Bit[6]: padclk_mipi_sc Bit[5]: pclk_vfifo Bit[4]: pclk_mipi Bit[3]: rst_sd Bit[2]: rst_mipi_sc Bit[1]: Reserved Bit[0]: rst_srb

table A-4 SC registers (sheet 5 of 9)

address	register name	default value	R/W	description
0x301B	SC_CLKRST5	0xF0	RW	Bit[7]: sclk_src Bit[6]: sclk_cvdn Bit[5]: sclk_asram_tst Bit[4]: sclk_snr_sync Bit[3]: rst_src Bit[2]: rst_cvdn Bit[1]: rst_asram_tst Bit[0]: rst_snr_sync
0x301C	SC_CLKRST6	0xF2	RW	Bit[7]: sclk_bist Bit[6]: sclk_srb Bit[5]: sclk_grp Bit[4]: Reserved Bit[3]: rst_bist Bit[2]: rst_srb Bit[1]: rst_grp Bit[0]: Reserved
0x301D	SC_FREX_RST	0x00	RW	Bit[7]: frex_mask_aec Bit[6]: frex_mask_blc Bit[5]: frex_mask_isp Bit[4]: frex_mask_dvp Bit[3]: frex_mask_mipi Bit[2]: frex_mask_vfifo Bit[1]: Reserved Bit[0]: frex_mask_mipi_phy
0x301E	SC_CTRL_1E	0x03	RW	Bit[7:5]: Sdiv Divider for sigma-delta (sdclk) Bit[4]: Reserved Bit[3]: pclk_sel 0: pll_pclk 1: pll_pclk_d2 Bit[2:1]: Reserved Bit[0]: sclk2x_sel 0: pll_sclk 1: pll_sclk_d2

table A-4 SC registers (sheet 6 of 9)

address	register name	default value	R/W	description
0x301F	SC_CLOCK_SEL	0x03	RW	Bit[7:6]: mipi_data_skew_o Bit[5]: mipi_clk_lane_ctrl 0: Clock lane hold LP00 when pd_mipi 1: Clock lane is high-z when pd_mipi Bit[4]: mipi_ctr_en 0: Disable function 1: Enable MIPI remote reset and suspend control sc Bit[3]: mipi_rst_sel 0: MIPI remote reset all registers 1: MIPI remote reset all digital module Bit[2]: gpio_pclk_en Bit[1]: frex_ef_sel Bit[0]: cen_global_o
0x3020	SC_CTRL_20	0x00	RW	Bit[7]: gclk_pwm Bit[6]: gclk_fmt Bit[5]: gclk_strobe Bit[4:2]: Reserved Bit[1]: gclk_srb Bit[0]: gclk_bist
0x3021	SC_CTRL_21	0x00	RW	Bit[7]: gclk_sync Bit[6]: gclk_asram_tst Bit[5]: gclk_cvdn Bit[4]: gclk_src Bit[3]: gpclk_mipi Bit[2]: gpclk_vfifo Bit[1:0]: Reserved
0x3022	SC_MISC_CTRL	0x01	RW	Bit[7:4]: Debug control Bit[3]: mipi_lvds_mode_o Bit[2]: Clock lane disable 1 Bit[1]: Clock lane disable 0 Bit[0]: pd_mipi_rst_sync pd_mipi enable when rst_sync

table A-4 SC registers (sheet 7 of 9)

address	register name	default value	R/W	description
0x3023	SC_CTRL_23	0x07	RW	Bit[7]: Reserved Bit[6]: phy_pd_mipi_pwdn_dis Bit[5]: phy_pd_lprx_pwdn_dis Bit[4]: r_stb_rst_dis_o 0: Reset all block at software standby mode 1: TC, sensor_control, ISP is reset, others are not Bit[3]: pd_ana_dis Bit[2]: pd_big_regulator_dis Bit[1]: phy_pd_mipi_slppd_dis Bit[0]: phy_pd_lprx_slppd_dis
0x3024	SC_CTRL_24	0x00	RW	Bit[7:1]: Reserved Bit[0]: pd_mipi_auto
0x3025	SC_GP_IO_SEL0	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: io_pad_sel_o[17:16]
0x3026	SC_GP_IO_SEL1	0x00	RW	Bit[7:0]: io_pad_sel_o[15:8]
0x3027	SC_GP_IO_SEL2	0x00	RW	Bit[7:0]: io_pad_sel_o[7:0]
0x3028	SC_GP_IO_IN0	–	R	Bit[7:0]: io_pad_i[23:16]
0x3029	SC_GP_IO_IN1	–	R	Bit[7:0]: io_pad_i[15:8]
0x302A	SC_GP_IO_IN2	–	R	Bit[7:0]: io_pad_i[7:0]
0x302B	SC_SCCB_ID2	0xE0	RW	Bit[7:0]: sccb_id[7:0]
0x302C	SC_LP_CTRL0	0x01	RW	Bit[7:0]: sc_lp_ctrl_o[39:32]
0x302D	SC_LP_CTRL1	0x00	RW	Bit[7:0]: sc_lp_ctrl_o[31:24]
0x302E	SC_LP_CTRL2	0x00	RW	Bit[7:0]: sc_lp_ctrl_o[23:16]
0x302F	SC_LP_CTRL3	0x00	RW	Bit[7:0]: sc_lp_ctrl_o[15:8]
0x3030	SC_LP_CTRL4	0x10	RW	Bit[7]: r_auto_sleep_en Bit[6]: r_gpio_sel 0: Not used 1: Sleep can be read by GPIO (Y9) Bit[5]: r_wake_up_pol Bit[4]: r_aslp_repeat Bit[3]: Reserved Bit[2]: r_fsin_wake_up_en Bit[1:0]: Reserved
0x3031	IO_Y_OEN_SLEEP0	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: io_y_oen_sleep[17:16]
0x3032	IO_Y_OEN_SLEEP1	0xFF	RW	Bit[7:0]: io_y_oen_sleep[15:8]

table A-4 SC registers (sheet 8 of 9)

address	register name	default value	R/W	description
0x3033	IO_Y_OEN_SLEEP2	0xFF	RW	Bit[7:0]: io_y_oen_sleep[7:0]
0x3034	IO_Y_OEN_PWDN0	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: io_y_oen_pwdn[17:16]
0x3035	IO_Y_OEN_PWDN1	0xFF	RW	Bit[7:0]: io_y_oen_pwdn[15:8]
0x3036	IO_Y_OEN_PWDN2	0xFF	RW	Bit[7:0]: io_y_oen_pwdn[7:0]
0x3037	SC_CTRL_37	0xF0	RW	Bit[7]: Reserved Bit[6]: sclk_strobe Bit[5]: sclk_fmt Bit[4]: sclk_pwm Bit[3]: rst_grp Bit[2]: rst_strobe Bit[1]: rst_fmt Bit[0]: rst_pwm
0x3038	SC_CTRL_38	0x50	RW	Bit[7]: Reserved Bit[6]: clk_tpm_src 0: SCLK 1: p_clk Bit[5]: clk_psram_11x_02x Bit[4]: Reserved Bit[3]: clk_src_11x_02x Bit[2]: frex_mask_strobe Bit[1]: frex_mask_fmt Bit[0]: frex_mask_pwm
0x3039	SC_CTRL_39	0x32	RW	Bit[7:5]: mipi_lane_num 0: One-lane mode 1: Two-lane mode, etc Bit[4]: mipi_en 0: DVP enable 1: MIPI enable Bit[3:2]: r_phy_pd_mipi Bit[1]: phy_rst option 0: Not used 1: Reset PHY when rst_sync Bit[0]: lane_dis_option 0: Not used 1: Disable lanes when pd_mipi
0x303A	SC_CTRL_3A	0x00	RW	Bit[7:0]: MIPI lane disable
0x303B	SC_CTRL_3B	0x00	RW	Bit[7:2]: Reserved Bit[1]: sccb_pgm_id_en Bit[0]: sccb_id2_nack_en
0x303C	SC_CTRL_3C	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: r_ppump_div

table A-4 SC registers (sheet 9 of 9)

address	register name	default value	R/W	description
0x303D	SC_CTRL_3D	0x02	RW	Bit[7:4]: r_npump2_div Bit[3:0]: r_npump1_div
0x303E	SC_CTRL_3E	0x07	RW	Bit[7:6]: Reserved Bit[5:0]: r_pump_ctrl
0x303F	SC_CTRL_3F	0x03	RW	Bit[7:0]: r_frame_on_num

A.2.4 SCCB [0x3100 - 0x3107, 0x31FF]

table A-5 SCCB control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3100	SB_SCCB_CTRL	0x00	RW	Bit[7:4]: Reserved Bit[3]: r_sda_dly_en Bit[2:0]: r_sda_dly
0x3101	SB_SCCB_OPT	0x12	RW	Bit[7:5]: Reserved Bit[4]: en_ss_addr_inc Bit[3]: r_sda_byp_sync 0: Two clock stage sync for sda_i 1: No sync for sda_i Bit[2]: r_scl_byp_sync 0: Two clock stage sync for scl_i 1: No sync for scl_i Bit[1]: r_msk_glitch Bit[0]: r_msk_stop
0x3102	SB_SCCB_FILTER	0x00	RW	Bit[7:4]: r_sda_num Bit[3:0]: r_scl_num
0x3103	SB_PLL_CLK_SEL	0x00	RW	Bit[7:6]: Reserved Bit[5]: r_sc_vs_sel Bit[4]: r_sc_sclk_sw Bit[3]: r_pumpclk_sw Bit[2]: r_pclk_sw_ext Bit[1]: r_pclk_sw Bit[0]: r_sclk_sw
0x3104	RSVD	–	–	Reserved
0x3105	SB_PADCLK_DIV	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_padclk_div[5:0]

table A-5 SCCB control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3106	SB_SRB_CTRL_0	0x08	RW	Bit[7]: sclk2x_o_en Bit[6]: sclk_o_en Bit[5:3]: arb_ctrl Bit[2]: pad_clk_sw Bit[1:0]: sclk_sel 00: pll_sclk 01: pll_sclk_d2 10: pll_sclk_d4 11: pll_sclk
0x3107	SB_SRB_CTRL_1	0x00	RW	Bit[7:6]: Reserved Bit[5]: disable_auto_wake Bit[4]: pd_mipi_dis_aslp Bit[3]: pumpclk_cutoff_byp Bit[2]: pclk_cutoff_byp Bit[1]: clk_cutoff_byp Bit[0]: p_clk_i_gate_en
0x31FF	SB_SWITCH	0x01	RW	Bit[7:1]: Reserved Bit[0]: sccb_sel 0: sccb_wo_clk (needs padclk to switch) 1: sccb_w_clk

A.2.5 group hold [0x3200 - 0x3204, 0x3206 - 0x320E, 0x3210 - 0x321F]

table A-6 group hold registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3200	GROUP ADR0	0x00	RW	Group0 Start Address in SRAM Actual Address is {0x3200[6:0], 4'h0}
0x3201	GROUP ADR1	0x08	RW	Group1 Start Address in SRAM Actual Address is {0x3201[6:0], 4'h0}
0x3202	GROUP ADR2	0x10	RW	Group2 Start Address in SRAM Actual Address is {0x3202[6:0], 4'h0}
0x3203	GROUP ADR3	0x18	RW	Group3 Start Address in SRAM Actual Address is {0x3203[6:0], 4'h0}
0x3204	GROUP ADR4	0x20	RW	SOF Triggered Embedded Line Data Start Address in SRAM Actual Address is {0x3204[6:0], 4'h0}

table A-6 group hold registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3206	FSIN_GRP	0x10	RW	FSIN Control Bit[7:5]: Reserved Bit[4]: fsin_en Bit[3:2]: Reserved Bit[1:0]: Start group in FSIN mode
0x3207	COMBINE_LAUNCH _CTRL	–	RW	Bit[7:4]: Launch select 0xA: Launch in frame blanking 0xE: Launch immediately 0x6: Launch in horizontal blanking Others: Not used Bit[3]: cmb_launch_grp3 Bit[2]: cmb_launch_grp2 Bit[1]: cmb_launch_grp1 Bit[0]: cmb_launch_grp0
0x3208	GROUP ACCESS	–	W	Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 1010: Group launch 1110: Fast group launch Others: Reserved Bit[3:0]: Group ID 0000: Group bank 0 0001: Group bank 1 0010: Group bank 2 0011: Group bank 3 Others: Reserved
0x3209	GROUP0 PERIOD	0x00	RW	Frame Number to Stay in Group 0
0x320A	GROUP1 PERIOD	0x00	RW	Frame Number to Stay in Group 1
0x320B	GROUP2 PERIOD	0x00	RW	Frame Number to Stay in Group 2
0x320C	GROUP3 PERIOD	0x00	RW	Frame Number to Stay in Group 3
0x320D	GRP SW_CTRL	0x01	RW	Context Switch Control Bit[7:6]: Reserved Bit[5]: Repeat switch mode Bit[4]: Context switch enable Bit[3:2]: Reserved Bit[1:0]: Switch back group
0x320E	SRAM TEST	0x00	RW	Bit[7:6]: RA Bit[5]: Test1 Bit[4]: TEST_srm Bit[3:0]: Group hold SRAM RM[3:0]
0x3210	GROUP LENGTH0	–	R	Group0 Register Number
0x3211	GROUP LENGTH1	–	R	Group1 Register Number

table A-6 group hold registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3212	GROUP LENGTH2	–	R	Group2 Register Number
0x3213	GROUP LENGTH3	–	R	Group3 Register Number
0x3214	GROUP LENGTH4	–	R	Group4 Register Number
0x3216	EMB_LINE_NUM	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Embedded line number
0x3217	PADDING_DATA	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Tag
0x3218	EMBED_LINE_CTRL	0x00	RW	Bit[7:6]: emb_ln_blk_ctrl Bit[5]: embline_addr_en Bit[4]: embline_tag_en Bit[3]: frame_trig_sel 0: tc_grp_wr 1: EOF Bit[2]: Debug mode Bit[1]: embline_sof_en Bit[0]: Debug mode
0x3219	EMBED_TAG_DATA	0x55	RW	Bit[7:0]: tag_data
0x321A	GROUP ACT	–	R	Active Group
0x321B	SRAM TEST1	0x0F	RW	Bit[7:5]: Not used Bit[4]: TEST_srm Bit[3:0]: RM
0x321C	GROUP0 FRAME COUNT	–	R	Frame Count When in Group 0
0x321D	GROUP1 FRAME COUNT	–	R	Frame Count When in Group 1
0x321E	GROUP2 FRAME COUNT	–	R	Frame Count When in Group 2
0x321F	GROUP3 FRAME COUNT	–	R	Frame Count When in Group 3

A.2.6 aec_pk [0x3501 - 0x3511, 0x3514 - 0x351A, 0x351E - 0x3525]

table A-7 aec_pk registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3501	EXPO	0x05	RW	Bit[7:0]: Exposure[15:8]
0x3502	EXPO	0xA0	RW	Bit[7:0]: Exposure[7:0]
0x3503	AEC MANUAL	0xA8	RW	Bit[7]: Not used Bit[6]: Digital gain delay option 0: Delay 2 frames 1: Delay 1 frame Bit[5]: Format change update enable Bit[4]: Gain delay option 0: Delay 2 frames 1: Delay 1 frame Bit[3:0]: Reserved
0x3504	GAIN OPTION	0x08	RW	Bit[7]: Real gain as sensor gain Bit[6]: ISP real gain option 0: Keep ISP real gain 1: Use BLC real gain as ISP real gain Bit[5]: Digital gain option 0: Apply digital gain in BLC 1: Apply digital gain in MWB Bit[4]: Gain delay by exposure change Bit[3]: Initial update enable Bit[2:0]: Not used
0x3505	MANUAL UPDATE	–	W	Bit[7:1]: Not used Bit[0]: Manual update enable
0x3506	EXPO FINE	0x00	RW	Bit[7:0]: Fine exposure[15:8]
0x3507	EXPO FINE	0x00	RW	Bit[7:0]: Fine exposure[7:0]
0x3508	GAIN COARSE	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Coarse real gain
0x3509	GAIN FINE	0x00	RW	Bit[7:4]: Fine real gain Bit[3:0]: Not used
0x350A	DIGIGAIN COARSE	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Coarse digital gain
0x350B	DIGIGAIN FINE	0x00	RW	Bit[7:0]: Digital fine gain[9:2] 4.10 format
0x350C	DIGIGAIN FINE	0x00	RW	Bit[7:6]: Digital fine gain[1:0] 4.10 format Bit[5:0]: Not used
0x350D	SNR GAIN MAP	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Sensor gain mapping option

table A-7 aec_pk registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x350E	EXPO COARSE CUR	–	R	Bit[7:0]: Current coarse exposure[15:8]
0x350F	EXPO COARSE CUR	–	R	Bit[7:0]: Current coarse exposure[7:0]
0x3510	EXPO FINE CUR	–	R	Bit[7:0]: Current fine exposure[15:8]
0x3511	EXPO FINE CUR	–	R	Bit[7:0]: Current fine exposure[7:0]
0x3514	ORG GAIN COARSE CUR	–	R	Bit[7:5]: Not used Bit[4:0]: Current coarse real gain
0x3515	ORG GAIN FINE CUR	–	R	Bit[7:4]: Current fine real gain Bit[3:0]: Not used
0x3516	SNR GAIN COARSE	–	R	Bit[7:4]: Not used Bit[3:0]: Coarse sensor gain
0x3517	SNR GAIN FINE	–	R	Bit[7:4]: Not used Bit[3:0]: Fine sensor gain
0x3518	DIG GAIN BLC COARSE	–	R	Bit[7:4]: Not used Bit[3:0]: Coarse BLC digital gain
0x3519	DIG GAIN BLC FINE	–	R	Bit[7:0]: Fine BLC digital gain[9:2]
0x351A	DIG GAIN BLC FINE	–	R	Bit[7:6]: Fine BLC digital gain[1:0] Bit[5:0]: Not used
0x351E	BLC GAIN COARSE	–	R	Bit[7:5]: Not used Bit[4:0]: Coarse BLC real gain
0x351F	BLC GAIN FINE	–	R	Bit[7:4]: Fine BLC real gain Bit[3:0]: Not used
0x3520	ISP GAIN COARSE	–	R	Bit[7:1]: Not used Bit[0]: Coarse ISP real gain[8]
0x3521	ISP GAIN COARSE	–	R	Bit[7:0]: Coarse ISP real gain[7:0]
0x3522	ISP GAIN FINE	–	R	Bit[7:4]: Fine ISP real gain Bit[3:0]: Not used
0x3523	DIGI_CUR_L	–	R	Bit[7:0]: Current long digital gain[15:8]
0x3524	DIGI_CUR_S	–	R	Bit[7:0]: Current short digital gain[7:0]
0x3525	DIGI_CUR_S	–	R	Bit[7:0]: Current short digital gain[15:8]

A.2.7 ana control [0x3600 - 0x36D1]

table A-8 ana control registers (sheet 1 of 7)

address	register name	default value	R/W	description
0x3600	R_TEST0	0x0F	RW	Bit[7:6]: Reserved Bit[5]: atest_in_enable Bit[4:0]: atest_select
0x3601~ 0x360F	RSVD	–	–	Reserved
0x3610	R_ARRAY0	0x80	RW	Bit[7:4]: vln_local_bias_current_control Bit[3:0]: col_skip
0x3611	R_ARRAY1	0x00	RW	Bit[7]: blsw_dip_enable (col_input_floating_en) Bit[6]: vln_casc_baypss Bit[5]: vln_local_bias_enable Bit[4:3]: ASRAM counter clock divider Bit[2]: Dcomp cascode bias bypass Bit[1]: Column test mode short to ground Bit[0]: Column test mode enable
0x3612	R_ARRAY2	0x10	RW	Bit[7]: ASRAM memory disable Bit[6:5]: ASRAM memory read clock delay Bit[4:2]: ASRAM memory read pre-charge delay Bit[1:0]: ASRAM counter clock delay
0x3613	R_ARRAY3	0x00	RW	Bit[7:6]: Reserved Bit[5]: sel_hvdd_rsd 0: RSD_high = AVDD 1: RSD_high = HVDD Bit[4]: Bitline test enable Bit[3]: ASRAM counter test sel1 Bit[2]: ASRAM counter clock select Bit[1]: ASRAM counter test sel Bit[0]: ASRAM counter clock phase select
0x3614~ 0x361F	RSVD	–	–	Reserved
0x3620	R_DAC0	0x71	RW	Bit[7:6]: Clock delay Bit[5:0]: Define ADC range 101010: For FWC10000 101111: For FWC8000
0x3621	R_DAC1	0xEC	RW	Bit[7]: Reserved Bit[6]: Input clock 0: Divided by 4 1: Divided by 2 Bit[5:0]: Reserved

table A-8 ana control registers (sheet 2 of 7)

address	register name	default value	R/W	description
0x3622	R_DAC2	0x40	RW	Bit[7]: Reserved Bit[6:4]: Constant gm current reference Bit[3]: integ_cas_bp Bit[2:0]: Resistor-generated current reference
0x3623	R_DAC3	0x02	RW	Bit[7:6]: Reserved Bit[5:4]: ramp_clock_divider Bit[3:0]: Reserved
0x3624~ 0x362F	RSVD	–	–	Reserved
0x3630	R_PWC0	0x88	RW	Bit[7:4]: Vln current reference Bit[3:0]: Master current reference
0x3631	R_PWC1	0x88	RW	Bit[7:4]: Vdac current reference Bit[3:0]: Dcomp1 current reference control
0x3632	R_PWC2	0x87	RW	Bit[7:4]: Pump current reference control Bit[3:0]: Blacksun rst voltage
0x3633	R_PWC3	0x7B	RW	Bit[7:4]: NVDD1 voltage control Bit[3:0]: HVDD voltage control
0x3634	R_PWC4	0xAA	RW	Bit[7:4]: NVDD3 voltage control Bit[3:0]: NVDD2 voltage control
0x3635	R_PWC5	0x06	RW	Bit[7:6]: Reserved Bit[5:4]: Control input current for biasing block of vramp_buffer Bit[3:0]: Bandgap trim options
0x3636	R_PWC6	0xA0	RW	Bit[7]: Add a LPF at AVDD power 0: Short resistor 1: Add a resistor Bit[6]: Reserved Bit[5:0]: Bias trim options
0x3637	R_PWC7	0x00	RW	Bit[7:5]: Change p-pump VCTRL PMOS multiple 000: m=8 111: m=1 Others: Not used Bit[4:2]: Control error amplifier current Bit[1:0]: Feedback resistor control 00: 40K 01: 320K 10: 80K 11: 360K
0x3638~ 0x363F	RSVD	–	–	Reserved

table A-8 ana control registers (sheet 3 of 7)

address	register name	default value	R/W	description
0x3640	R_OSC0	0x00	RW	Bit[7]: OSC1 and OSC2 IO device OSC work, OSC1 output Bit[6]: OSC2 IO device OSC work Bit[5]: OSC1 IO device OSC work Bit[4]: Ring OSC power down-output Bit[3]: OSC1 and OSC2 core device OSC work, OSC1 output Bit[2]: OSC2 core device OSC work Bit[1]: OSC1 core device OSC work Bit[0]: Ring OSC power down
0x3641~ 0x365F	RSVD	–	–	Reserved
0x3660	R_CORE_0	0x80	RW	Bit[7]: rip_sof_en Bit[6]: frame_mask Bit[5]: Reserved Bit[4]: r_ecl_sig_en_disable Bit[3]: r_col_vln_sig_clamp_en_disable Bit[2:0]: pad_share_gpio10_o_sel
0x3661	R_CORE_1	0xBA	RW	Bit[7]: r_pad_strobe_i_dis Bit[6:4]: r_pad_share_strobe_o Bit[3:0]: r_pad_share_strobe_i
0x3662	R_CORE_2	0x65	RW	Bit[7]: Reserved Bit[6]: pll1_lock_en Bit[5]: pll2_lock_en Bit[4]: r_pad_gpio2_i_dis Bit[3]: vsync_st_sel Bit[2]: mipi_2lane_en Bit[1]: Reserved Bit[0]: r_pad_gpio_i_dis
0x3663	R_CORE_3	0xF0	RW	Bit[7]: rst_top_auto Bit[6]: Reserved Bit[5]: rst_pll1_auto Bit[4]: rst_pll2_auto Bit[3]: rst_top Bit[2]: Reserved Bit[1]: rst_pll1 Bit[0]: rst_pll2
0x3664	R_CORE_4	0xF0	RW	Bit[7]: rst_adc_auto Bit[6]: rst_adc_man Bit[5]: rst_array_auto Bit[4]: rst_array_man Bit[3]: rst_otp_auto Bit[2]: rst_opt_man Bit[1]: rst_pwc_auto Bit[0]: rst_pwc_man

table A-8 ana control registers (sheet 4 of 7)

address	register name	default value	R/W	description
0x3665	RSVD	–	–	Reserved
0x3666	R_CORE_6	0x00	RW	Bit[7]: Reserved Bit[6:4]: r_pad_share_fsin_o Bit[3:0]: r_pad_share_fsin_i
0x3667	R_CORE_7	0x8A	RW	Bit[7]: r_pad_pwm_i_dis Bit[6:4]: r_pad_share_pwm_o Bit[3:0]: r_pad_share_pwm_i
0x3668	R_CORE_8	0x98	RW	Bit[7:4]: r_pad_share_sid1_i Bit[3:0]: r_pad_share_sid0_i
0x3669	R_CORE_9	0x0A	RW	Bit[7]: r_vsync_div Bit[6]: r_strobe_fmod12_in Bit[5]: parameter_hold Bit[4]: re_time_disable Bit[3]: r_fmt_vsync_opt Bit[2:1]: r_mipi_vc_id_man Bit[0]: dvp_dis_fmt_chg
0x366A	R_CORE_A	0x00	RW	Bit[7:0]: r_strobe_add_dmy_in[15:8]
0x366B	R_CORE_B	0x00	RW	Bit[7:0]: r_strobe_add_dmy_in[7:0]
0x366C	R_CORE_C	0x00	RW	Bit[7:0]: p_y[9:2]
0x366D	R_CORE_D	0x00	RW	Bit[7:6]: p_y[1:0] Bit[5]: p_pclk Bit[4]: p_href Bit[3]: Reserved Bit[2]: p_strobe Bit[1]: p_pwm Bit[0]: p_fsin
0x366E	R_CORE_E	0x00	RW	Bit[7]: Reserved Bit[6:0]: bypass_select
0x366F	R_CORE_F	0x5A	RW	Bit[7]: Reserved Bit[6]: emb_data_lsb Bit[5]: bist_err_flag_dis Bit[4]: opt_bist_err_flag_dis Bit[3]: d_rst_mipi_auto Bit[2]: d_rst_mipi Bit[1]: Reserved Bit[0]: d_rst_mipi_vbk_en
0x3670	R_CORE_10	0x08	RW	Bit[7]: r_frame_insert Bit[6:5]: r_aec_pk_vsync_opt Bit[4:0]: r_exp_ofst
0x3671	RSVD	–	–	Reserved

table A-8 ana control registers (sheet 5 of 7)

address	register name	default value	R/W	description
0x3672	R_CORE_12	0x08	RW	Bit[7]: Reserved Bit[6]: d_rst_pll1_vbk_en Bit[5]: d_rst_pll2_vbk_en Bit[4]: d_rst_top_vbk_en Bit[3]: d_rst_adc_vbk_en Bit[2]: d_rst_array_vbk_en Bit[1]: d_rst_otp_vbk_en Bit[0]: d_rst_pwc_vbk_en
0x3673	R_CORE_13	0x00	RW	Bit[7]: rst_ac_test Bit[6]: rst_tc_test Bit[5]: pll2_wdg_en Bit[4]: pll1_wdg_en Bit[3:0]: wdp_width[3:0]
0x3674	R_CORE_14	0x10	RW	Bit[7:5]: dvp_rd_pause_vsize[10:8] Bit[4]: scblk_man Bit[3]: dvp_vsize_sel Bit[2]: sc_blk_sel Bit[1]: dvp_en Bit[0]: embed_en
0x3675	R_CORE_15	0x00	RW	Bit[7:0]: dvp_rd_pause_vsize[7:0]
0x3676	R_CORE_16	0x00	RW	Bit[7]: Reserved Bit[6:4]: r_pad_share_href_o Bit[3:0]: r_pad_share_href_i
0x3677	R_CORE_17	0x00	RW	Bit[7]: Reserved Bit[6:4]: r_pad_share_pclk_o Bit[3:0]: r_pad_share_pclk_i
0x3678	R_CORE_18	0x00	RW	Bit[7:0]: otp_auto_load_adr_st[7:0]
0x3679	R_CORE_19	0x00	RW	Bit[7]: fsin_lock Bit[6]: pwm_lock Bit[5]: strobe_lock Bit[4]: gpio10_lock Bit[3]: Reserved Bit[2]: dig_test_frame Bit[1:0]: Reserved
0x367A~ 0x367C	RSVD	–	–	Reserved
0x367D	R_CORE_NEW_7D	0x00	RW	Bit[7:5]: Reserved Bit[4]: r_col_dcomp_selcap_en Bit[3:0]: Reserved
0x367E	R_CORE_NEW_7E	0xD0	RW	Bit[7:4]: r_ramp_vref_man Bit[3]: r_col_dcomp_offset_man_en Bit[2:0]: r_col_dcomp_offset_man

table A-8 ana control registers (sheet 6 of 7)

address	register name	default value	R/W	description
0x367F	R_CORE_NEW_7F	0x00	RW	Bit[7]: Reserved Bit[6:4]: r_sel_cap_thre Bit[3]: r_ramp_vref_en Bit[2]: r_row_vfd_lo_en Bit[1]: r_blksun_sig_en Bit[0]: r_ramp_vofs_en
0x3680	R_CORE_NEW_80	0x44	RW	Bit[7:4]: r_row_vfd_lo_8x Bit[3:0]: r_row_vfd_lo_4x
0x3681	R_CORE_NEW_81	0x44	RW	Bit[7:4]: r_row_vfd_lo_2x Bit[3:0]: r_row_vfd_lo_1x
0x3682	R_CORE_NEW_82	0xAA	RW	Bit[7:4]: r_blksun_sig_8x Bit[3:0]: r_blksun_sig_4x
0x3683	R_CORE_NEW_83	0xAA	RW	Bit[7:4]: r_blksun_sig_2x Bit[3:0]: r_blksun_sig_1x
0x3684	R_CORE_NEW_84	0x0E	RW	Bit[7:5]: Reserved Bit[4:0]: r_ramp_vofs_8x
0x3685	R_CORE_NEW_85	0x0E	RW	Bit[7:5]: Reserved Bit[4:0]: r_ramp_vofs_4x
0x3686	R_CORE_NEW_86	0x0E	RW	Bit[7:5]: Reserved Bit[4:0]: r_ramp_vofs_2x
0x3687	R_CORE_NEW_87	0x0E	RW	Bit[7:5]: Reserved Bit[4:0]: r_ramp_vofs_1x
0x3688	R_CORE_NEW_88	0xDD	RW	Bit[7:4]: r_ramp_vref_8x Bit[3:0]: r_ramp_vref_4x
0x3689	R_CORE_NEW_89	0xDD	RW	Bit[7:4]: r_ramp_vref_2x Bit[3:0]: r_ramp_vref_1x
0x368A	R_CORE_NEW_8A	0xDD	RW	Bit[7:4]: r_sel_cap_8x Bit[3:0]: r_sel_cap_4x
0x368B	R_CORE_NEW_89	0xDD	RW	Bit[7:4]: r_sel_cap_2x Bit[3:0]: r_sel_cap_1x
0x368C~ 0x369F	RSVD	–	–	Reserved
0x36A0	R_ASRAM_0	0x02	RW	Bit[7:0]: r_asram_0
0x36A1	R_ASRAM_1	0x05	RW	Bit[7:0]: r_asram_1
0x36A2	R_ASRAM_2	0x05	RW	Bit[7:0]: r_asram_2
0x36A3	R_ASRAM_3	0x00	RW	Bit[7:0]: r_asram_3
0x36A4	R_ASRAM_4	0x20	RW	Bit[7:0]: r_asram_4

table A-8 ana control registers (sheet 7 of 7)

address	register name	default value	R/W	description
0x36A5~ 0x36AF	RSVD	–	–	Reserved
0x36B0	R_DVP_TOP_0	0x00	RW	Bit[7:6]: r_pclk_dly Bit[5]: r_prbs_chk Bit[4]: r_pll_pclk_inv Bit[3]: r_pclk_pol Bit[2]: r_dvpsync_rst Bit[1]: r_ddr_mode Bit[0]: r_byp
0x36B1	R_DVP_TOP_1	0x00	RW	Bit[7:1]: Reserved Bit[0]: r_pll_pclk_div2
0x36B2~ 0x36BF	RSVD	–	–	Reserved
0x36C0	R_PXTEST_0	0x00	RW	Bit[7:6]: px_vtest2[1:0] Bit[5:0]: px_vtest1[5:0]
0x36C1	R_PXTEST_1	0x00	RW	Bit[7:4]: px_vtest3[3:0] Bit[3:0]: px_vtest2[5:2]
0x36C2	R_PXTEST_2	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: px_vtest3[5:4]
0x36C3~ 0x36CF	RSVD	–	–	Reserved
0x36D0	R_TPM_0	0x00	RW	Bit[7:6]: Reserved Bit[5]: chop_op Bit[4]: chop_pd Bit[3:0]: Vrbg[3:0]
0x36D1	R_TPM_1	0x00	RW	Bit[7:6]: Reserved Bit[5]: chop_op Bit[4]: chop_pd Bit[3:0]: Vrbg[3:0]

A.2.8 sensor control [0x3700 - 0x37EF]

table A-9 sensor control registers (sheet 1 of 12)

address	register name	default value	R/W	description
0x3700	SNR_CTRL_00	0x20	RW	Bit[7:0]: r_rstgolow
0x3701	SNR_CTRL_01	0x10	RW	Bit[7:0]: r_initclk

table A-9 sensor control registers (sheet 2 of 12)

address	register name	default value	R/W	description
0x3702	SNR_CTRL_02	0x00	RW	Bit[7:1]: Reserved Bit[0]: r_invclk[8]
0x3703	SNR_CTRL_03	0x34	RW	Bit[7:0]: r_invclk[7:0]
0x3704	SNR_CTRL_04	0x1C	RW	Bit[7:0]: r_ramp_gap
0x3705	SNR_CTRL_05	0x0C	RW	Bit[7:0]: r_cnt_dwn_gap
0x3706	SNR_CTRL_06	0x00	RW	Bit[7:0]: r_cnt_dwn[15:8]
0x3707	SNR_CTRL_07	0x56	RW	Bit[7:0]: r_cnt_dwn[7:0]
0x3708	SNR_CTRL_08	0x08	RW	Bit[7:0]: r_xlckb_w
0x3709	SNR_CTRL_09	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: r_tx_samp[9:8]
0x370A	SNR_CTRL_0A	0x60	RW	Bit[7:0]: r_tx_samp[7:0]
0x370B	SNR_CTRL_0B	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: r_cntup_gap[9:8]
0x370C	SNR_CTRL_0C	0x40	RW	Bit[7:0]: r_cntup_gap[7:0]
0x370D	SNR_CTRL_0D	0x00	RW	Bit[7:0]: r_cnt_up[15:8]
0x370E	SNR_CTRL_0E	0xFA	RW	Bit[7:0]: r_cnt_up[7:0]
0x370F	SNR_CTRL_0F	0x07	RW	Bit[7:0]: r_samp_gap[15:8]
0x3710	SNR_CTRL_10	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: r_gap
0x3711	SNR_CTRL_11	0x04	RW	Bit[7:4]: Reserved Bit[3:0]: r_samp_rst_high
0x3712	SNR_CTRL_12	0x00	RW	Bit[7]: r_rd_pause_en Bit[6]: r_rs_re Bit[5]: r_rsall0 Bit[4]: r_rst_re Bit[3]: r_txhigh Bit[2]: r_rp_tx_re Bit[1]: r_rrblue_re Bit[0]: r_rrblue_al
0x3713	SNR_CTRL_13	0x00	RW	Bit[7:5]: Reserved Bit[4]: r_db_samp Bit[3]: r_yreven_re Bit[2]: r_yreven_al Bit[1]: r_srs_end_early Bit[0]: r_dkblc

table A-9 sensor control registers (sheet 3 of 12)

address	register name	default value	R/W	description
0x3714	SNR_CTRL_14	0x03	RW	Bit[7:5]: Reserved Bit[4]: r_rp_addr_en_re Bit[3]: r_noxlckb Bit[2:0]: r_srsdip
0x3715	SNR_CTRL_15	0x14	RW	Bit[7:4]: r_ckap_r Bit[3:0]: r_addr_chg
0x3716	SNR_CTRL_16	0x01	RW	Bit[7:4]: Reserved Bit[3:0]: r_rst_go_high
0x3717	SNR_CTRL_17	0x01	RW	Bit[7:4]: Reserved Bit[3]: r_rblue_odd_pix_re Bit[2]: r_rred_odd_pix_re Bit[1]: r_odd_pix_all0 Bit[0]: r_rp_addr_en_mask_opt
0x3718	SNR_CTRL_18	0x11	RW	Bit[7:0]: r_integ_high1
0x3719	SNR_CTRL_19	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: r_integ_high2[9:8]
0x371A	SNR_CTRL_1A	0x7F	RW	Bit[7:0]: r_integ_high2[7:0]
0x371B	SNR_CTRL_1B	0x0A	RW	Bit[7:0]: r_vln_en_low
0x371C	SNR_CTRL_1C	0x0A	RW	Bit[7:0]: r_dcomp_en_low
0x371D	SNR_CTRL_1D	0x0A	RW	Bit[7:0]: r_sram_start_pnt1
0x371E	SNR_CTRL_1E	0x0C	RW	Bit[7:0]: r_sram_start_pnt2
0x371F	SNR_CTRL_1F	0x0C	RW	Bit[7:0]: r_integ_low1
0x3720	SNR_CTRL_20	0x02	RW	Bit[7:2]: Reserved Bit[1:0]: r_sram_start1_opt
0x3721	SNR_CTRL_21	0x02	RW	Bit[7:0]: r_integ_low2
0x3722	SNR_CTRL_22	0x0C	RW	Bit[7:0]: r_dcomp_vbn_sh_high
0x3723	SNR_CTRL_23	0x0A	RW	Bit[7:0]: r_dcomp2_vbn_sh_high
0x3724	SNR_CTRL_24	0x0A	RW	Bit[7:0]: r_ramp_buf_en_low
0x3725	SNR_CTRL_25	0x6A	RW	Bit[7:4]: r_samp_high Bit[3:0]: r_samp_low
0x3726	SNR_CTRL_26	0x06	RW	Bit[7:4]: Reserved Bit[3:0]: r_vln_en_high
0x3727	SNR_CTRL_27	0x06	RW	Bit[7:4]: Reserved Bit[3:0]: r_ramp_buf_en_high
0x3728	SNR_CTRL_28	0x0A	RW	Bit[7:4]: Reserved Bit[3:0]: r_samp_sig_flag_low

table A-9 sensor control registers (sheet 4 of 12)

address	register name	default value	R/W	description
0x3729	SNR_CTRL_29	0x06	RW	Bit[7:4]: Reserved Bit[3:0]: r_dcomp_en_high
0x372A	SNR_CTRL_2A	0x05	RW	Bit[7:0]: r_vln_vbn_sh_high
0x372B	SNR_CTRL_2B	0x02	RW	Bit[7:4]: Reserved Bit[3:0]: r_vln_vbn_sh_low
0x372C	SNR_CTRL_2C	0x00	RW	Bit[7:4]: Reserved Bit[3]: r_ramp_vofs_samp_all1 Bit[2]: r_ramp_vofs_samp_re Bit[1]: r_dcomp_voffset_en_all0 Bit[0]: r_dcomp_voffset_en_re
0x372D	SNR_CTRL_2D	0x20	RW	Bit[7:4]: Reserved Bit[3:0]: r_vln_bnc_sh_low
0x372E	SNR_CTRL_2E	0x02	RW	Bit[7:6]: Reserved Bit[5]: r_ramp_buf_en_all1 Bit[4]: r_ramp_buf_en_re Bit[3:0]: r_dcomp_vbn_sh_low
0x372F	SNR_CTRL_2F	0x0C	RW	Bit[7:0]: r_ramp_vref_samp_high
0x3730	SNR_CTRL_30	0x28	RW	Bit[7:0]: r_ramp_vref_samp_low
0x3731	SNR_CTRL_31	0x00	RW	Bit[7]: r_dcomp_vbn_sh_all1 Bit[6]: r_ramp_vref_samp_all1 Bit[5]: r_samp_all1 Bit[4]: r_vln_en_all1 Bit[3]: r_dcomp_vbn_sh_re Bit[2]: r_ramp_vref_samp_re Bit[1]: r_samp_re Bit[0]: r_vln_en_re
0x3732	SNR_CTRL_32	0x20	RW	Bit[7]: Reserved Bit[6]: r_vref_samp_opt Bit[5]: r_dcomp_en_all1 Bit[4]: r_vln_vbn_sh_all1 Bit[3]: r_dcomp2_vbn_sh_all1 Bit[2]: r_dcomp_en_re Bit[1]: r_vln_vbn_sh_re Bit[0]: r_dcomp2_vbn_sh_re
0x3733	SNR_CTRL_33	0x00	RW	Bit[7:6]: Reserved Bit[5]: r_integ_all0_dwn Bit[4]: r_integ_all0_up Bit[3]: r_integ_re Bit[2]: r_dcomp_en_all0_dwn Bit[1]: r_dcomp_en_all0_up Bit[0]: r_dcomp_cmp_en_re

table A-9 sensor control registers (sheet 5 of 12)

address	register name	default value	R/W	description
0x3734	SNR_CTRL_34	0x00	RW	Bit[7:1]: Reserved Bit[0]: r_frm_rst_re
0x3735	SNR_CTRL_35	0x00	RW	Bit[7:2]: Reserved Bit[1]: r_col_count_reset_all0_dwn Bit[0]: r_col_count_reset_all0_up
0x3736	SNR_CTRL_36	0x00	RW	Bit[7]: r_samp_rst_flag_all1 Bit[6]: r_samp_sig_flag_all1 Bit[5]: r_cmp_en_all0_dwn Bit[4]: r_cmp_en_all0_up Bit[3]: r_samp_rst_flag_re Bit[2]: r_samp_sig_flag_re Bit[1]: r_sample_last_opt Bit[0]: r_cmp_en_re
0x3737	SNR_CTRL_37	0x05	RW	Bit[7:0]: r_col_count_reset_low1 = r_ramp_gap - register 0x3737
0x3738	SNR_CTRL_38	0x06	RW	Bit[7:0]: r_col_count_reset_low2 = r_cntup_gap0 - register 0x3738
0x3739	SNR_CTRL_39	0x0A	RW	Bit[7:0]: r_col_count_reset_high1 = r_col_count_reset_low1 - register 0x3739
0x373A	SNR_CTRL_3A	0x0A	RW	Bit[7:0]: r_col_count_reset_high2 = r_col_count_reset_low2 - register 0x373A
0x373B	SNR_CTRL_3B	0x01	RW	Bit[7:3]: Reserved Bit[2:1]: r_samp_sig_flag_option Bit[0]: r_ecl_avdd_en_mask
0x373C	SNR_CTRL_3C	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: r_samp_sig_flag_high[9:8]
0x373D	SNR_CTRL_3D	0x06	RW	Bit[7:0]: r_samp_sig_flag_high[7:0]
0x373E	SNR_CTRL_3E	0x01	RW	Bit[7:2]: Reserved Bit[1:0]: r_sadd_bin_inc_sel 00: +1 01: +2 10: +4 11: Not used
0x373F	SNR_CTRL_3F	0x00	RW	Bit[7:3]: Reserved Bit[2]: r_rst_int_opt Bit[1:0]: r_rline_sw
0x3740	SNR_CTRL_40	0x00	RW	Bit[7:1]: Reserved Bit[0]: r_dacs_m_st_en
0x3741	SNR_CTRL_41	0x00	RW	Bit[7:0]: r_dacs_ini_man[15:8]

table A-9 sensor control registers (sheet 6 of 12)

address	register name	default value	R/W	description
0x3742	SNR_CTRL_42	0x00	RW	Bit[7:0]: r_dacs_ini_man[7:0]
0x3743	SNR_CTRL_43	0x00	RW	Bit[7:6]: Reserved Bit[5]: r_psr_samp_re Bit[4]: r_psr_samp_all0 Bit[3:2]: r_psr_samp_high[9:8] Bit[1:0]: r_psr_samp_low[9:8]
0x3744	SNR_CTRL_44	0x04	RW	Bit[7:0]: r_psr_samp_high[7:0]
0x3745	SNR_CTRL_45	0x5E	RW	Bit[7:0]: r_psr_samp_low[7:0]
0x3746~ 0x374F	RSVD	–	–	Reserved
0x3750	SNR_CTRL_50	0x0C	RW	Bit[7:0]: r_ramp_vofs_samp[15:8]
0x3751	SNR_CTRL_51	0x28	RW	Bit[7:0]: r_ramp_vofs_samp[7:0]
0x3752	SNR_CTRL_52	0x0A	RW	Bit[7:0]: r_samp_rst_low
0x3753	SNR_CTRL_53	0x04	RW	Bit[7:4]: Reserved Bit[3:0]: r_dcomp2_vbn_sh_low
0x3754	SNR_CTRL_54	0x44	RW	Bit[7:4]: r_dcomp_rst_high_sel_0 Bit[3:0]: r_dcomp_rst_high_sel_1
0x3755	SNR_CTRL_55	0x00	RW	Bit[7:5]: Reserved Bit[4:3]: r_dcomp_rst_low_sel_0[9:8] Bit[2]: Reserved Bit[1:0]: r_dcomp_rst_low_sel_1[9:8]
0x3756	SNR_CTRL_56	0x4E	RW	Bit[7:0]: r_dcomp_rst_low_sel_1[7:0]
0x3757	SNR_CTRL_57	0x00	RW	Bit[7:5]: Reserved Bit[4:3]: r_dcomp_2_rst_high_sel_0[9:8] Bit[2]: Reserved Bit[1:0]: r_dcomp_2_rst_high_sel_1[9:8]
0x3758	SNR_CTRL_58	0x04	RW	Bit[7:0]: r_dcomp_2_rst_high_sel_1[7:0]
0x3759	SNR_CTRL_59	0x00	RW	Bit[7:5]: Reserved Bit[4:3]: r_dcomp_2_rst_low_sel_0[9:8] Bit[2]: Reserved Bit[1:0]: r_dcomp_2_rst_low_sel_1[9:8]
0x375A	SNR_CTRL_5A	0x5E	RW	Bit[7:0]: r_dcomp_2_rst_low_sel_1[7:0]
0x375B	SNR_CTRL_5B	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: r_dcomp_3_rst_high
0x375C	SNR_CTRL_5C	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: r_dcomp_3_rst_low[9:8]
0x375D	SNR_CTRL_5D	0x98	RW	Bit[7:0]: r_dcomp_3_rst_low[7:0]

table A-9 sensor control registers (sheet 7 of 12)

address	register name	default value	R/W	description
0x375E	SNR_CTRL_5E	0x44	RW	Bit[7:4]: r_dcomp2_rst_high_set_1 Bit[3:0]: r_dcomp2_rst_high_set_0
0x375F	SNR_CTRL_5F	0x00	RW	Bit[7:5]: Reserved Bit[4:3]: r_dcomp2_rst_low_sel_0[9:8] Bit[2]: Reserved Bit[1:0]: r_dcomp2_rst_low_sel_1[9:8]
0x3760	SNR_CTRL_60	0x3C	RW	Bit[7:0]: r_dcomp2_rst_low_sel_1[7:0]
0x3761	SNR_CTRL_61	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: r_dcomp3_en_high[9:8]
0x3762	SNR_CTRL_62	0x58	RW	Bit[7:0]: r_dcomp3_en_high[7:0]
0x3763	SNR_CTRL_63	0x06	RW	Bit[7:4]: Reserved Bit[3:0]: r_dcomp3_en_low
0x3764	SNR_CTRL_64	0x00	RW	Bit[7:6]: Reserved Bit[5]: r_dcomp_rst_all0 Bit[4]: r_dcomp2_rst_all0 Bit[3]: r_dcomp_2_rst_all0 Bit[2]: r_dcomp_3_rst_all0 Bit[1]: r_count_init_clk_re Bit[0]: r_count_init_clk_all0
0x3765	SNR_CTRL_65	0x00	RW	Bit[7:6]: Reserved Bit[5]: r_dcomp3_en_all0 Bit[4]: r_dcomp3_en_re Bit[3]: r_dcomp_rst_re Bit[2]: r_dcomp2_rst_re Bit[1]: r_dcomp_2_rst_re Bit[0]: r_dcomp_3_rst_re
0x3766	SNR_CTRL_66	0x00	RW	Bit[7:2]: Reserved Bit[1]: r_sram_start2_opt Bit[0]: r_sram_start_manu_en
0x3767	SNR_CTRL_67	0x00	RW	Bit[7:0]: r_sram_start_man[15:8]
0x3768	SNR_CTRL_68	0x17	RW	Bit[7:0]: r_sram_start_man[7:0]
0x3769	SNR_CTRL_69	0x2C	RW	Bit[7:4]: r_dcomp_voffset_en_high Bit[3:0]: r_dcomp_voffset_en_low
0x376A	SNR_CTRL_6A	0x2C	RW	Bit[7:4]: r_dcomp_voffset_en2_high Bit[3:0]: r_dcomp_voffset_en2_low
0x376B	SNR_CTRL_6B	0x02	RW	Bit[7:0]: r_col_count_init_clk_high
0x376C	SNR_CTRL_6C	0x0c	RW	Bit[7:0]: r_col_count_init_clk_low
0x376D	SNR_CTRL_6D	0x00	RW	Bit[7:0]: psr_sw_1x
0x376E	SNR_CTRL_6E	0x00	RW	Bit[7:0]: psr_sw_2x

table A-9 sensor control registers (sheet 8 of 12)

address	register name	default value	R/W	description
0x376F	SNR_CTRL_6F	0x00	RW	Bit[7:0]: psr_sw_4x
0x3770	SNR_CTRL_70	0x00	RW	Bit[7:0]: psr_sw_8x
0x3771	SNR_CTRL_71	0x0C	RW	Bit[7:0]: r_vln_bnc_sh_high
0x3772	SNR_CTRL_72	0x01	RW	Bit[7:2]: Reserved Bit[1]: r_sh_vrhv_opt Bit[0]: r_sh_vrhv_all1
0x3773	SNR_CTRL_73	0x04	RW	Bit[7:0]: r_sh_vrhv_high
0x3774	SNR_CTRL_74	0x64	RW	Bit[7:0]: r_sh_vrhv_low
0x3775	SNR_CTRL_75	0x62	RW	Bit[7:4]: r_ck_ap_end Bit[3:0]: r_gap_ck_ap
0x3776	SNR_CTRL_76	0x01	RW	Bit[7:3]: Reserved Bit[2]: r_rst_all1 Bit[1]: r_rs_all1 Bit[0]: r_vbin4_rgb
0x3777	SNR_CTRL_77	0x00	RW	Bit[7:2]: Reserved Bit[1]: r_rfd_all1 Bit[0]: r_rfd_sel
0x3778	SNR_CTRL_78	0x00	RW	Bit[7]: Reserved Bit[6]: r_mono_br Bit[5]: r_mono_g Bit[4]: r_mono_rgb Bit[3]: r_ecl_avdd_en_re Bit[2]: r_ecl_avdd_en_all1 Bit[1:0]: r_tx_ch_sw
0x3779	SNR_CTRL_79	0x05	RW	Bit[7:0]: r_sg_dly
0x377A	SNR_CTRL_7A	0x0A	RW	Bit[7:0]: r_sg_width
0x377B	SNR_CTRL_7B	0x00	RW	Bit[7:5]: Reserved Bit[4]: r_fx1_en Bit[3:1]: Not used Bit[0]: r_zeroline_en
0x377C	SNR_CTRL_7C	0x42	RW	Bit[7:6]: r_zeroline_mask Bit[5:0]: r_zeroline_num
0x377D	SNR_CTRL_7D	0x02	RW	Bit[7:6]: Reserved Bit[5]: r_dcomp_vcn_sh_all1 Bit[4]: r_dcomp_vcn_sh_re Bit[3:0]: r_dcomp_vcn_sh_low
0x377E	SNR_CTRL_7E	0x0C	RW	Bit[7:0]: r_dcomp_vcn_sh_high
0x377F	SNR_CTRL_7F	0x00	RW	Bit[7:1]: Reserved Bit[0]: r_gst_dis

table A-9 sensor control registers (sheet 9 of 12)

address	register name	default value	R/W	description
0x3780~ 0x379A	RSVD	–	–	Reserved
0x379B	SNR_CTRL_9B	0x00	RW	Bit[7:0]: r_fexp_offset[15:8]
0x379C	SNR_CTRL_9C	0x00	RW	Bit[7:0]: r_fexp_offset[7:0]
0x379D~ 0x379F	RSVD	–	–	Reserved
0x37A0	SNR_CTRL_A0	–	R	frm_cnt
0x37A1	SNR_CTRL_A1	–	R	Bit[7:0]: da_hts[15:8]
0x37A2	SNR_CTRL_A2	–	R	Bit[7:0]: da_hts[7:0]
0x37A3	SNR_CTRL_A3	0xA0	RW	Bit[7:6]: r_ecl_avdd_ofst_ed Bit[5:4]: r_ecl_avdd_ofst Bit[3]: r_fast_up_re Bit[2]: r_fast_up_all1 Bit[1:0]: r_fast_up_sig_hi_sel
0x37A4	SNR_CTRL_A4	0x04	RW	Bit[7:0]: r_fast_up_hi_blk
0x37A5	SNR_CTRL_A5	0x10	RW	Bit[7:0]: r_fast_up_low_blk
0x37A6	SNR_CTRL_A6	0x0A	RW	Bit[7:0]: r_fast_up_hi_sig
0x37A7	SNR_CTRL_A7	0x10	RW	Bit[7:0]: r_fast_up_low_sig
0x37A8	SNR_CTRL_A8	0x4E	RW	Bit[7:0]: r_dcomp_rst_low_sel_0[7:0]
0x37A9	SNR_CTRL_A9	0x04	RW	Bit[7:0]: r_dcomp_2_rst_high_sel_0[15:8]
0x37AA	SNR_CTRL_AA	0x5E	RW	Bit[7:0]: r_dcomp_2_rst_low_sel_0[7:0]
0x37AB	SNR_CTRL_AB	0x3C	RW	Bit[7:0]: r_dcomp2_rst_low_sel_0[7:0]
0x37AC	SNR_CTRL_AC	0x08	RW	Bit[7]: r_ecl_sig_en_re Bit[6]: r_ecl_sig_en_all1 Bit[5:4]: r_ecl_sig_en_option Bit[3:0]: r_ecl_sig_en_low
0x37AD	SNR_CTRL_AD	0x06	RW	Bit[7:0]: r_ecl_sig_en_high[7:0]
0x37AE	SNR_CTRL_AE	0x04	RW	Bit[7:6]: r_ecl_sig_en_high[9:8] Bit[5]: r_ecl_blk_en_re Bit[4]: r_ecl_blk_en_all1 Bit[3:0]: r_ecl_blk_en_high
0x37AF	SNR_CTRL_AF	0x04	RW	Bit[7:0]: r_ecl_blk_en_low
0x37B0	SNR_CTRL_B0	0x14	RW	Bit[7:0]: snr_ctrl_B0
0x37B1	SNR_CTRL_B1	0x24	RW	Bit[7:0]: snr_ctrl_B1
0x37B2	SNR_CTRL_B2	0x34	RW	Bit[7:0]: snr_ctrl_B2

table A-9 sensor control registers (sheet 10 of 12)

address	register name	default value	R/W	description
0x37B3	SNR_CTRL_B3	0x30	RW	Bit[7:0]: snr_ctrl_B3
0x37B4	SNR_CTRL_B4	0x24	RW	Bit[7:0]: snr_ctrl_B4
0x37B5	SNR_CTRL_B5	0x32	RW	Bit[7:0]: snr_ctrl_B5
0x37B6	SNR_CTRL_B6	0x06	RW	Bit[7:0]: snr_ctrl_B6
0x37B7	SNR_CTRL_B7	0x14	RW	Bit[7:0]: snr_ctrl_B7
0x37B8	SNR_CTRL_B8	0x0A	RW	Bit[7:0]: snr_ctrl_B8
0x37B9	SNR_CTRL_B9	0x07	RW	Bit[7:0]: snr_ctrl_B9
0x37BA	SNR_CTRL_BA	0xC0	RW	Bit[7:0]: snr_ctrl_BA
0x37BB	SNR_CTRL_BB	0x26	RW	Bit[7:0]: snr_ctrl_BB
0x37BC	SNR_CTRL_BC	0x30	RW	Bit[7:0]: snr_ctrl_BC
0x37BD	SNR_CTRL_BD	0x08	RW	Bit[7:0]: snr_ctrl_BD
0x37BE	SNR_CTRL_BE	0x12	RW	Bit[7:0]: snr_ctrl_BE
0x37BF	SNR_CTRL_BF	0x0C	RW	Bit[7:0]: snr_ctrl_BF
0x37C0	SNR_CTRL_C0	0x05	RW	Bit[7:0]: snr_ctrl_C0
0x37C1	SNR_CTRL_C1	0x1B	RW	Bit[7:0]: snr_ctrl_C1
0x37C2	SNR_CTRL_C2	0x02	RW	Bit[7:0]: snr_ctrl_C2
0x37C3	SNR_CTRL_C3	0x3F	RW	Bit[7:0]: snr_ctrl_C3
0x37C4	SNR_CTRL_C4	0x02	RW	Bit[7:0]: snr_ctrl_C4
0x37C5	SNR_CTRL_C5	0x34	RW	Bit[7:0]: snr_ctrl_C5
0x37C6	SNR_CTRL_C6	0x28	RW	Bit[7:0]: snr_ctrl_C6
0x37C7	SNR_CTRL_C7	0x2E	RW	Bit[7:0]: snr_ctrl_C7
0x37C8	SNR_CTRL_C8	0x0A	RW	Bit[7:0]: snr_ctrl_C8
0x37C9	SNR_CTRL_C9	0x10	RW	Bit[7:0]: snr_ctrl_C9
0x37CA	SNR_CTRL_CA	0x02	RW	Bit[7:0]: snr_ctrl_CA
0x37CB	SNR_CTRL_CB	0x03	RW	Bit[7:0]: snr_ctrl_CB
0x37CC	SNR_CTRL_CC	0x00	RW	Bit[7:0]: snr_ctrl_CC
0x37CD	SNR_CTRL_CD	0x03	RW	Bit[7:0]: snr_ctrl_CD
0x37CE	SNR_CTRL_CE	0x0C	RW	Bit[7:0]: snr_ctrl_CE
0x37CF	SNR_CTRL_CF	0x02	RW	Bit[7:0]: snr_ctrl_CF
0x37D0	SNR_CTRL_D0	0x00	RW	Bit[7:0]: snr_ctrl_D0

table A-9 sensor control registers (sheet 11 of 12)

address	register name	default value	R/W	description
0x37D1	SNR_CTRL_D1	0x05	RW	Bit[7:0]: snr_ctrl_D1
0x37D2	SNR_CTRL_D2	0x00	RW	Bit[7:0]: snr_ctrl_D2
0x37D3	SNR_CTRL_D3	0x00	RW	Bit[7:0]: snr_ctrl_D3
0x37D4	SNR_CTRL_D4	0x08	RW	Bit[7:0]: snr_ctrl_D4
0x37D5	SNR_CTRL_D5	0x28	RW	Bit[7:0]: snr_ctrl_D5
0x37D6	SNR_CTRL_D6	0x10	RW	Bit[7:0]: snr_ctrl_D6
0x37D7	SNR_CTRL_D7	0x45	RW	Bit[7:0]: snr_ctrl_D7
0x37D8	SNR_CTRL_D8	0x00	RW	Bit[7:0]: snr_ctrl_D8
0x37D9	SNR_CTRL_D9	0x00	RW	Bit[7:0]: snr_ctrl_D9
0x37DA	SNR_CTRL_DA	0x56	RW	Bit[7:0]: snr_ctrl_DA
0x37DB	SNR_CTRL_DB	0x56	RW	Bit[7:0]: snr_ctrl_DB
0x37DC	SNR_CTRL_DC	0x56	RW	Bit[7:0]: snr_ctrl_DC
0x37DD	SNR_CTRL_DD	0xFA	RW	Bit[7:0]: snr_ctrl_DD
0x37DE	SNR_CTRL_DE	0xFA	RW	Bit[7:0]: snr_ctrl_DE
0x37DF	SNR_CTRL_DF	0xFA	RW	Bit[7:0]: snr_ctrl_DF
0x37E0	SNR_CTRL_E0	0x00	RW	Bit[7:0]: snr_ctrl_E0
0x37E1	SNR_CTRL_E1	0x00	RW	Bit[7:0]: snr_ctrl_E1
0x37E2	SNR_CTRL_E2	0x00	RW	Bit[7:0]: snr_ctrl_E2
0x37E3	SNR_CTRL_E3	0x00	RW	Bit[7:0]: snr_ctrl_E3
0x37E4	SNR_CTRL_E4	0x00	RW	Bit[7:0]: snr_ctrl_E4
0x37E5	SNR_CTRL_E5	0x00	RW	Bit[7:0]: snr_ctrl_E5
0x37E6	SNR_CTRL_E6	0x00	RW	Bit[7:0]: snr_ctrl_E6
0x37E7	SNR_CTRL_E7	0x00	RW	Bit[7:0]: snr_ctrl_E7
0x37E8	SNR_CTRL_E8	0x00	RW	Bit[7:0]: snr_ctrl_E8
0x37E9	SNR_CTRL_E9	0x00	RW	Bit[7:0]: snr_ctrl_E9
0x37EA	SNR_CTRL_EA	0x00	RW	Bit[7:0]: snr_ctrl_EA
0x37EB	SNR_CTRL_EB	0x00	RW	Bit[7:0]: snr_ctrl_EB
0x37EC	SNR_CTRL_EC	0x00	RW	Bit[7:0]: snr_ctrl_EC
0x37ED	SNR_CTRL_ED	0x00	RW	Bit[7:0]: snr_ctrl_ED
0x37EE	SNR_CTRL_EE	0x00	RW	Bit[7:0]: snr_ctrl_EE

table A-9 sensor control registers (sheet 12 of 12)

address	register name	default value	R/W	description
0x37EF	SNR_CTRL_EF	0x00	RW	Bit[7:0]: snr_ctrl_EF

A.2.9 timing [0x3800 - 0x3837, 0x383C - 0x383D]

table A-10 timing control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x3800	TIMING_X_ADDR_START	0x00	RW	Bit[7:0]: x_addr_start[15:8] Array horizontal start point
0x3801	TIMING_X_ADDR_START	0x00	RW	Bit[7:0]: x_addr_start[7:0] Array horizontal start point
0x3802	TIMING_Y_ADDR_START	0x00	RW	Bit[7:0]: y_addr_start[15:8] Array vertical start point
0x3803	TIMING_Y_ADDR_START	0x00	RW	Bit[7:0]: y_addr_start[7:0] Array vertical start point
0x3804	TIMING_X_ADDR_END	0x06	RW	Bit[7:0]: x_addr_end[15:8] Array horizontal end point
0x3805	TIMING_X_ADDR_END	0x4F	RW	Bit[7:0]: x_addr_end[7:0] Array horizontal end point
0x3806	TIMING_Y_ADDR_END	0x05	RW	Bit[7:0]: y_addr_end[15:8] Array vertical end point
0x3807	TIMING_Y_ADDR_END	0x23	RW	Bit[7:0]: y_addr_end[7:0] Array vertical end point
0x3808	TIMING_X_OUTPUT_SIZE	0x06	RW	Bit[7:0]: x_output_size[15:8] ISP horizontal output width
0x3809	TIMING_X_OUTPUT_SIZE	0x40	RW	Bit[7:0]: x_output_size[7:0] ISP horizontal output width
0x380A	TIMING_Y_OUTPUT_SIZE	0x05	RW	Bit[7:0]: y_output_size[15:8] ISP vertical output height
0x380B	TIMING_Y_OUTPUT_SIZE	0x14	RW	Bit[7:0]: y_output_size[7:0] ISP vertical output height
0x380C	TIMING_HTS	0x03	RW	Bit[7:0]: HTS[15:8] Total pixels per line
0x380D	TIMING_HTS	0x88	RW	Bit[7:0]: HTS[7:0] Total pixels per line

table A-10 timing control registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x380E	TIMING_VTS	0x05	RW	Bit[7:0]: VTS[15:8] Total lines per frame
0x380F	TIMING_VTS	0xC2	RW	Bit[7:0]: VTS[7:0] Total lines per frame
0x3810	TIMING_ISP_X_WIN	0x00	RW	Bit[7:0]: isp_x_win[15:8] ISP horizontal windowing offset
0x3811	TIMING_ISP_X_WIN	0x08	RW	Bit[7:0]: isp_x_win[7:0] ISP horizontal windowing offset
0x3812	TIMING_ISP_Y_WIN	0x00	RW	Bit[7:0]: isp_y_win[15:8] ISP vertical windowing offset
0x3813	TIMING_ISP_Y_WIN	0x08	RW	Bit[7:0]: isp_y_win[7:0] ISP vertical windowing offset
0x3814	TIMING_X_INC	0x11	RW	Bit[7:4]: x_odd_inc Bit[3:0]: x_even_inc
0x3815	TIMING_Y_INC	0x11	RW	Bit[7:4]: y_odd_inc Bit[3:0]: y_even_inc
0x3816	TIMING_RSVD	0x00	RW	Bit[7:0]: HSYNC start point[15:8]
0x3817	TIMING_RSVD	0x00	RW	Bit[7:0]: HSYNC start point[7:0]
0x3818	TIMING_RSVD	0x04	RW	Bit[7:0]: HSYNC end point[15:8]
0x3819	TIMING_RSVD	0x00	RW	Bit[7:0]: HSYNC end point[7:0]
0x381A	TIMING_RSVD	0x00	RW	Bit[7:0]: HSYNC first active row start position[15:8]
0x381B	TIMING_RSVD	0x00	RW	Bit[7:0]: HSYNC first active row start position[7:0]
0x381C	TIMING_RSVD	0x00	RW	Bit[7:0]: Thumbnail horizontal output width[15:8]
0x381D	TIMING_RSVD	0x00	RW	Bit[7:0]: Thumbnail horizontal output width[7:0]
0x381E	TIMING_RSVD	0x00	RW	Bit[7:0]: Thumbnail vertical output height[15:8]
0x381F	TIMING_RSVD	0x00	RW	Bit[7:0]: Thumbnail vertical output height[7:0]

table A-10 timing control registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x3820	TIMING_FORMAT1	0x40	RW	Bit[7]: vsub48_blc_dis Bit[6]: vflip_blc Bit[5]: Reserved Bit[4]: half_row_p1 Bit[3]: Reserved Bit[2]: Vflip Vertical image flip Bit[1]: Vbinf Vertical binning Bit[0]: Reserved
0x3821	TIMING_FORMAT2	0x00	RW	Bit[7:4]: Reserved Bit[3]: Fman Bit[2]: Horizontal image mirror Bit[1]: Reserved Bit[0]: Horizontal binning
0x3822	TIMING_REG22	0x50	RW	Bit[7:5]: addr0_num[3:1] Bit[4:0]: ablc_num[5:1]
0x3823	TIMING_REG23	0x00	RW	Bit[7]: fmt_chg_min_dly (write only) Bit[6]: ext_vs_re Bit[5]: ext_vs_en Bit[4]: r_init_man Bit[3]: vts_no_latch Bit[2:0]: ablc_adj
0x3824	TIMING_CS_RST_FSIN	0x00	RW	CS Reset Value High Byte at vs_ext
0x3825	TIMING_CS_RST_FSIN	0x00	RW	CS Reset Value Low Byte at vs_ext
0x3826	TIMING_RST_FSIN	0x00	RW	R Reset Value High Byte at vs_ext
0x3827	TIMING_RST_FSIN	0x00	RW	R Reset Value Low Byte at vs_ext
0x3828	TIMING_FVTS	0x00	RW	Fractional Vertical Timing Size High Byte
0x3829	TIMING_FVTS	0x00	RW	Fractional Vertical Timing Size Low Byte
0x382A	TIMING_REG2A	0x00	RW	Bit[7:4]: Reserved Bit[3]: vts_auto_en Bit[2]: Not used Bit[1:0]: href_w
0x382B	TIMING_REG2B	0xFA	RW	Bit[7:4]: grp_wr_start Bit[3:0]: tc_r_int_adj
0x382C	TIMING_REG2C	0x05	RW	Bit[7:0]: hts_global_tx[15:8]
0x382D	TIMING_REG2D	0xB0	RW	Bit[7:0]: hts_global_tx[7:0]

table A-10 timing control registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x382E	TIMING_REG2E	0x01	RW	Bit[7:3]: Reserved Bit[2]: r_tc_hts_blank 0: Uniform HTS 1: Separate HTS for global transfer Bit[1]: r_blc_lines_sync_tc 0: tc_href 1: tc_href synced to image line start Bit[0]: r_blc_lines_sync 0: tc_href 1: blc_href synced to image line start
0x382F	TIMING_REG2F	0x04	RW	Bit[7]: r_pd_row_st_opt 0: auto_vbk_st 1: manu_vbk_st Bit[6]: r_pd_row_ed_opt 0: auto_vbk_ed 1: manu_vbk_ed Bit[5]: r_pd_ana_to_sys 0: ana_vbk cover sys_vbk 1: ana_vbk same as sys_vbk Bit[4]: r_pd_sys_to_ana 0: sys_vbk covered by ana_vbk 1: sys_vbk same as ana_vbk Bit[3:0]: r_pd_row_ofst[3:0] Auto offset after vbk_st and before vbk_ed
0x3830	TIMING_TC_R	–	R	Bit[7:0]: System row counter[15:8]
0x3831	TIMING_TC_R	–	R	Bit[7:0]: System row counter[7:0]
0x3832	TIMING_REG32	0x00	RW	Bit[7:0]: pd_vbk_st[15:8] Start of power saving in vblank upper byte reference to row count
0x3833	TIMING_REG33	0x05	RW	Bit[7:0]: pd_vbk_st[7:0] Start of power saving in vblank lower byte reference to row count
0x3834	TIMING_REG34	0x00	RW	Bit[7:0]: pd_vbk_ed[15:8] End of power saving in vblank upper byte reference to row count
0x3835	TIMING_REG35	0x05	RW	Bit[7:0]: pd_vbk_ed[7:0] End of power saving in vblank lower byte reference to row count
0x3836	RSVD	–	–	Reserved

table A-10 timing control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x3837	TIMING_REG37	0x00	RW	Bit[7:5]: Reserved Bit[4]: dcw_bw Bit[3]: dcw_bin_man Bit[2]: dcw_bin Bit[1]: dcw_bin_sum Bit[0]: dcw_en
0x383C~ 0x383D	RSVD	–	–	Reserved

A.2.10 global shutter [0x3880 - 0x38EC, 0x3900 - 0x3933]

table A-11 global shutter control registers (sheet 1 of 8)

address	register name	default value	R/W	description
0x3880	GLOBAL_SHUTTER_CTRL_00	0x10	RW	Bit[7:4]: r_samr_pre Offset before exposure for glbshut_frame_pchg Bit[3:0]: r_samr_m Offset before exposure for glbshut_line_pchg
0x3881	GLOBAL_SHUTTER_CTRL_01	0x44	RW	Bit[7:3]: r_rd_restart_dly Bit[2:1]: r_rdstop_pre Bit[0]: r_rampen_neg 0: Rampen active high 1: Rampen active low
0x3882	GLOBAL_SHUTTER_CTRL_02	0x01	RW	Bit[7:0]: r_gst_col_ofst[15:8]
0x3883	GLOBAL_SHUTTER_CTRL_03	0x00	RW	Bit[7:0]: r_gst_col_ofst[7:0]
0x3884	GLOBAL_SHUTTER_CTRL_04	0x00	RW	Bit[7:0]: r_gst_row_ofst[15:8]
0x3885	GLOBAL_SHUTTER_CTRL_05	0x02	RW	Bit[7:0]: r_gst_row_ofst[7:0]
0x3886	GLOBAL_SHUTTER_CTRL_06	0x00	RW	Bit[7:0]: r_gst_gpchg_pre[15:8]
0x3887	GLOBAL_SHUTTER_CTRL_07	0x15	RW	Bit[7:0]: r_gst_gpchg_pre[7:0]
0x3888	GLOBAL_SHUTTER_CTRL_08	0x44	RW	Bit[7:4]: r_gst_blpchg_r Bit[3:0]: r_gst_frmrst_r
0x3889	GLOBAL_SHUTTER_CTRL_09	0x04	RW	Bit[7:4]: Reserved Bit[3:0]: r_gst_rspchg_r
0x388A	GLOBAL_SHUTTER_CTRL_0A	0x00	RW	Bit[7:0]: r_gst_og_w[15:8]
0x388B	GLOBAL_SHUTTER_CTRL_0B	0x50	RW	Bit[7:0]: r_gst_og_w[7:0]

table A-11 global shutter control registers (sheet 2 of 8)

address	register name	default value	R/W	description
0x388C	GLOBAL_SHUTTER_CTRL_0C	0x44	RW	Bit[7:4]: r_gst_blpchg_f Bit[3:0]: r_gst_rspchg_f
0x388D	GLOBAL_SHUTTER_CTRL_0D	0x04	RW	Bit[7:4]: Reserved Bit[3:0]: r_gst_frmrst_f
0x388E	GLOBAL_SHUTTER_CTRL_0E	0x00	RW	Bit[7:0]: r_gst_tx_pre[15:8]
0x388F	GLOBAL_SHUTTER_CTRL_0F	0x50	RW	Bit[7:0]: r_gst_tx_pre[7:0]
0x3890	GLOBAL_SHUTTER_CTRL_10	0x04	RW	Bit[7:4]: Reserved Bit[3:0]: r_gst_sg_pre
0x3891	GLOBAL_SHUTTER_CTRL_11	0x44	RW	Bit[7:4]: r_gst_sg_suf Bit[3:0]: r_gst_tx_suf
0x3892	GLOBAL_SHUTTER_CTRL_12	0x00	RW	Bit[7:0]: r_gst_tx_w[15:8]
0x3893	GLOBAL_SHUTTER_CTRL_13	0xF0	RW	Bit[7:0]: r_gst_tx_w[7:0]
0x3894	GLOBAL_SHUTTER_CTRL_14	0x20	RW	Bit[7]: r_gst_sg_g_high Bit[6]: r_gst_rs_high Bit[5]: r_gst_bitshrt_high Bit[4]: r_gst_bitisw_high Bit[3]: r_gst_blen_high Bit[2]: r_gst_frmrst_high Bit[1]: r_gst_tx_high Bit[0]: r_gst_row_high
0x3895	GLOBAL_SHUTTER_CTRL_15	0x00	RW	Bit[7]: r_gst_sg_g_low Bit[6]: r_gst_rs_low Bit[5]: r_gst_bitshrt_low Bit[4]: r_gst_bitisw_low Bit[3]: r_gst_blen_low Bit[2]: r_gst_frmrst_low Bit[1]: r_gst_tx_low Bit[0]: r_gst_row_low
0x3896	GLOBAL_SHUTTER_CTRL_16	0x00	RW	Bit[7:0]: r_gsp_col_ofst[15:8]
0x3897	GLOBAL_SHUTTER_CTRL_17	0x10	RW	Bit[7:0]: r_gsp_col_ofst[7:0]
0x3898	GLOBAL_SHUTTER_CTRL_18	0x30	RW	Bit[7:6]: Reserved Bit[5]: r_gst_exp_nonoverlap Bit[4]: r_gsp_line Bit[3:2]: Not used Bit[1:0]: r_gsp_start_opt
0x3899	GLOBAL_SHUTTER_CTRL_19	0x01	RW	Bit[7]: r_vln_en_stop Bit[6:4]: Reserved Bit[3:0]: r_vln_en_ahead_line
0x389A	GLOBAL_SHUTTER_CTRL_1A	0x01	RW	Bit[7:0]: r_gsp_lpchg_pre[15:8]
0x389B	GLOBAL_SHUTTER_CTRL_1B	0x00	RW	Bit[7:0]: r_gsp_lpchg_pre[7:0]

table A-11 global shutter control registers (sheet 3 of 8)

address	register name	default value	R/W	description
0x389C	GLOBAL_SHUTTER_CTRL_1C	0x44	RW	Bit[7:4]: r_gsp_rspchg_r Bit[3:0]: r_gsp_blpchg_r
0x389D	GLOBAL_SHUTTER_CTRL_1D	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: r_gsgs_start_opt
0x389E	GLOBAL_SHUTTER_CTRL_1E	0x00	RW	Bit[7:0]: r_gsp_og_w[15:8]
0x389F	GLOBAL_SHUTTER_CTRL_1F	0x3C	RW	Bit[7:0]: r_gsp_og_w[7:0]
0x38A0	GLOBAL_SHUTTER_CTRL_20	0x44	RW	Bit[7:4]: r_gsp_blpchg_f Bit[3:0]: r_gsp_rspchg_f
0x38A1	GLOBAL_SHUTTER_CTRL_21	0x05	RW	Bit[7:0]: r_gsp_lpchg_ed
0x38A2	GLOBAL_SHUTTER_CTRL_22	0x00	RW	Bit[7:0]: r_gsgs_col_ofst[15:8]
0x38A3	GLOBAL_SHUTTER_CTRL_23	0x10	RW	Bit[7:0]: r_gsgs_col_ofst[7:0]
0x38A4	GLOBAL_SHUTTER_CTRL_24	0x10	RW	Bit[7]: Reserved Bit[6]: r_gsp_act_high Bit[5]: r_gsp_rs_high Bit[4]: r_gsp_bitshrt_high Bit[3]: r_gsp_bitisw_high Bit[2]: r_gsp_blen_high Bit[1]: r_gsp_og_high Bit[0]: r_gst_og_high
0x38A5	GLOBAL_SHUTTER_CTRL_25	0x00	RW	Bit[7]: Reserved Bit[6]: r_gsp_act_low Bit[5]: r_gsp_rs_low Bit[4]: r_gsp_bitshrt_low Bit[3]: r_gsp_bitisw_low Bit[2]: r_gsp_blen_low Bit[1]: r_gsp_og_low Bit[0]: r_gst_og_low
0x38A6	GLOBAL_SHUTTER_CTRL_26	0x00	RW	Bit[7:0]: r_gsgs_lpchg_pre[15:8]
0x38A7	GLOBAL_SHUTTER_CTRL_27	0x50	RW	Bit[7:0]: r_gsgs_lpchg_pre[7:0]
0x38A8	GLOBAL_SHUTTER_CTRL_28	0x00	RW	Bit[7:0]: r_gsgs_lpchg_w[15:8]
0x38A9	GLOBAL_SHUTTER_CTRL_29	0xF0	RW	Bit[7:0]: r_gsgs_lpchg_w[7:0]
0x38AA	GLOBAL_SHUTTER_CTRL_2A	0x44	RW	Bit[7:4]: r_gsgs_vgslpchg_suf Bit[3:0]: r_gsgs_vgslpchg_w
0x38AB	GLOBAL_SHUTTER_CTRL_2B	0x00	RW	Bit[7:2]: Reserved Bit[1]: r_gs_vgs_low Bit[0]: r_gs_gs_low
0x38AC	GLOBAL_SHUTTER_CTRL_2C	0x00	RW	Bit[7:0]: r_gsgs_ppchg_pre[15:8]
0x38AD	GLOBAL_SHUTTER_CTRL_2D	0x50	RW	Bit[7:0]: r_gsgs_ppchg_pre[7:0]

table A-11 global shutter control registers (sheet 4 of 8)

address	register name	default value	R/W	description
0x38AE	GLOBAL_SHUTTER_CTRL_2E	0x00	RW	Bit[7:0]: r_gsgs_ppchg_w[15:8]
0x38AF	GLOBAL_SHUTTER_CTRL_2F	0x78	RW	Bit[7:0]: r_gsgs_ppchg_w[7:0]
0x38B0	GLOBAL_SHUTTER_CTRL_30	0x44	RW	Bit[7:4]: r_gsgs_vgsppchg_suf Bit[3:0]: r_gsgs_vgsppchg_w
0x38B1	GLOBAL_SHUTTER_CTRL_31	0x02	RW	Bit[7:4]: Reserved Bit[3:2]: r_gs_vgs_combo Bit[1:0]: r_gs_gs_combo
0x38B2	GLOBAL_SHUTTER_CTRL_32	0x00	RW	Bit[7:0]: r_exp_row_ofst[15:8]
0x38B3	GLOBAL_SHUTTER_CTRL_33	0x02	RW	Bit[7:0]: r_exp_row_ofst[7:0]
0x38B4	GLOBAL_SHUTTER_CTRL_34	0x00	RW	Bit[7:6]: Reserved Bit[5]: t_gs_re Bit[4]: t_gs_all0 Bit[3:1]: Reserved Bit[0]: t_gs_pluse_en
0x38B5	GLOBAL_SHUTTER_CTRL_35	0x00	RW	Bit[7:6]: Reserved Bit[5]: t_tsg_re Bit[4]: t_tsg_all0 Bit[3:1]: Reserved Bit[0]: t_tsg_2nd_pluse_en
0x38B6	GLOBAL_SHUTTER_CTRL_36	0x00	RW	Bit[7]: t_rsg_re Bit[6]: t_rsg_all0 Bit[5]: t_rsd_re Bit[4]: t_rsd_all0 Bit[3:1]: Reserved Bit[0]: t_rsd_2nd_pluse_en
0x38B7	GLOBAL_SHUTTER_CTRL_37	0x00	RW	Bit[7]: t_frmrst_re Bit[6]: t_frmrst_all0 Bit[5]: t_og_re Bit[4]: t_og_all0 Bit[3:1]: Reserved Bit[0]: t_og_2nd_pluse_en
0x38B8~ 0x38BF	RSVD	–	–	Reserved
0x38C0	GLOBAL_SHUTTER_CTRL_40	0x00	RW	Bit[7:0]: t_gs_rise[15:8]
0x38C1	GLOBAL_SHUTTER_CTRL_41	0xBE	RW	Bit[7:0]: t_gs_rise[7:0]
0x38C2	GLOBAL_SHUTTER_CTRL_42	0x01	RW	Bit[7:0]: t_gs_fall[15:8]
0x38C3	GLOBAL_SHUTTER_CTRL_43	0x0E	RW	Bit[7:0]: t_gs_fall[7:0]
0x38C4	GLOBAL_SHUTTER_CTRL_44	0x01	RW	Bit[7:0]: t_tsg_rise1[15:8]
0x38C5	GLOBAL_SHUTTER_CTRL_45	0x18	RW	Bit[7:0]: t_tsg_rise1[7:0]

table A-11 global shutter control registers (sheet 5 of 8)

address	register name	default value	R/W	description
0x38C6	GLOBAL_SHUTTER_CTRL_46	0x02	RW	Bit[7:0]: t_tsg_fall1[15:8]
0x38C7	GLOBAL_SHUTTER_CTRL_47	0xA8	RW	Bit[7:0]: t_tsg_fall1[7:0]
0x38C8	GLOBAL_SHUTTER_CTRL_48	0x03	RW	Bit[7:0]: t_tsg_rise2[15:8]
0x38C9	GLOBAL_SHUTTER_CTRL_49	0x5C	RW	Bit[7:0]: t_tsg_rise2[7:0]
0x38CA	GLOBAL_SHUTTER_CTRL_4A	0x03	RW	Bit[7:0]: t_tsg_fall2[15:8]
0x38CB	GLOBAL_SHUTTER_CTRL_4B	0xAC	RW	Bit[7:0]: t_tsg_fall2[7:0]
0x38CC	GLOBAL_SHUTTER_CTRL_4C	0x00	RW	Bit[7:0]: t_rsd_rise1[15:8]
0x38CD	GLOBAL_SHUTTER_CTRL_4D	0x14	RW	Bit[7:0]: t_rsd_rise1[7:0]
0x38CE	GLOBAL_SHUTTER_CTRL_4E	0x00	RW	Bit[7:0]: t_rsd_fall1[15:8]
0x38CF	GLOBAL_SHUTTER_CTRL_4F	0xB4	RW	Bit[7:0]: t_rsd_fall1[7:0]
0x38D0	GLOBAL_SHUTTER_CTRL_50	0x02	RW	Bit[7:0]: t_rsd_rise2[15:8]
0x38D1	GLOBAL_SHUTTER_CTRL_51	0xB2	RW	Bit[7:0]: t_rsd_rise2[7:0]
0x38D2	GLOBAL_SHUTTER_CTRL_52	0x03	RW	Bit[7:0]: t_rsd_fall2[15:8]
0x38D3	GLOBAL_SHUTTER_CTRL_53	0x52	RW	Bit[7:0]: t_rsd_fall2[7:0]
0x38D4	GLOBAL_SHUTTER_CTRL_54	0x00	RW	Bit[7:0]: t_rsg_rise[15:8]
0x38D5	GLOBAL_SHUTTER_CTRL_55	0x02	RW	Bit[7:0]: t_rsg_rise[7:0]
0x38D6	GLOBAL_SHUTTER_CTRL_56	0x03	RW	Bit[7:0]: t_rsg_fall[15:8]
0x38D7	GLOBAL_SHUTTER_CTRL_57	0xE8	RW	Bit[7:0]: t_rsg_fall[7:0]
0x38D8	GLOBAL_SHUTTER_CTRL_58	0x00	RW	Bit[7:0]: t_og_rise1[15:8]
0x38D9	GLOBAL_SHUTTER_CTRL_59	0x3C	RW	Bit[7:0]: t_og_rise1[7:0]
0x38DA	GLOBAL_SHUTTER_CTRL_5A	0x00	RW	Bit[7:0]: t_og_fall1[15:8]
0x38DB	GLOBAL_SHUTTER_CTRL_5B	0x8C	RW	Bit[7:0]: t_og_fall1[7:0]
0x38DC	GLOBAL_SHUTTER_CTRL_5C	0x02	RW	Bit[7:0]: t_og_rise2[15:8]
0x38DD	GLOBAL_SHUTTER_CTRL_5D	0xDA	RW	Bit[7:0]: t_og_rise2[7:0]
0x38DE	GLOBAL_SHUTTER_CTRL_5E	0x03	RW	Bit[7:0]: t_og_fall2[15:8]
0x38DF	GLOBAL_SHUTTER_CTRL_5F	0x2A	RW	Bit[7:0]: t_og_fall2[7:0]
0x38E0	GLOBAL_SHUTTER_CTRL_60	0x00	RW	Bit[7:0]: t_frmrst_rise[15:8]
0x38E1	GLOBAL_SHUTTER_CTRL_61	0x02	RW	Bit[7:0]: t_frmrst_rise[7:0]
0x38E2	GLOBAL_SHUTTER_CTRL_62	0x03	RW	Bit[7:0]: t_frmrst_fall[15:8]
0x38E3	GLOBAL_SHUTTER_CTRL_63	0xE8	RW	Bit[7:0]: t_frmrst_fall[7:0]

table A-11 global shutter control registers (sheet 6 of 8)

address	register name	default value	R/W	description
0x38E4	GLOBAL_SHUTTER_CTRL_64	0x00	RW	Bit[7:0]: r_nvdd_row_offset[15:8]
0x38E5	GLOBAL_SHUTTER_CTRL_65	0x03	RW	Bit[7:0]: r_nvdd_row_offset[7:0]
0x38E6	GLOBAL_SHUTTER_CTRL_66	0x00	RW	Bit[7:0]: r_npump_t2_clk_offset[15:8]
0x38E7	GLOBAL_SHUTTER_CTRL_67	0x03	RW	Bit[7:0]: r_npump_t2_clk_offset[7:0]
0x38E8	GLOBAL_SHUTTER_CTRL_68	0x00	RW	Bit[7]: t_addr_en_re Bit[6]: t_addr_en_all0 Bit[5]: npump_t2_clk_re Bit[4]: npump_t2_clk_all0 Bit[3:2]: Reserved Bit[1]: gs_nvdd_en_re Bit[0]: gs_nvdd_en_all0
0x38E9	GLOBAL_SHUTTER_CTRL_69	0x00	RW	Bit[7:0]: t_addr_en_rise[15:8]
0x38EA	GLOBAL_SHUTTER_CTRL_6A	0x02	RW	Bit[7:0]: t_addr_en_rise[7:0]
0x38EB	GLOBAL_SHUTTER_CTRL_6B	0x03	RW	Bit[7:0]: t_addr_en_fall[15:8]
0x38EC	GLOBAL_SHUTTER_CTRL_6C	0xE8	RW	Bit[7:0]: t_addr_en_fall[7:0]
0x3900	PWM_CTRL_00	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: r_strobe_st_opt
0x3901	PWM_CTRL_01	0x01	RW	Bit[7:0]: r_strobe_row_st[15:8]
0x3902	PWM_CTRL_02	0xB4	RW	Bit[7:0]: r_strobe_row_st[7:0]
0x3903	PWM_CTRL_03	0x00	RW	Bit[7:0]: r_strobe_cs_st[15:8]
0x3904	PWM_CTRL_04	0x00	RW	Bit[7:0]: r_strobe_cs_st[7:0]
0x3905~ 0x390F	RSVD	–	–	Reserved
0x3910	PWM_CTRL_10	0xFF	RW	Bit[7:0]: div_reg[15:8]
0x3911	PWM_CTRL_11	0xFF	RW	Bit[7:0]: div_reg[7:0]
0x3912	PWM_CTRL_12	0x08	RW	Bit[7:0]: duty_reg[15:8] 0~65535: 0% ~ 100%
0x3913	PWM_CTRL_13	0x00	RW	Bit[7:0]: duty_reg[7:0] 0~65535: 0% ~ 100%
0x3914	PWM_CTRL_14	0x00	RW	Bit[7:0]: led_duty_cycle_low_reg[15:8]
0x3915	PWM_CTRL_15	0x00	RW	Bit[7:0]: led_duty_cycle_low_reg[7:0]
0x3916	PWM_CTRL_16	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: led_average_l_low_reg[9:8]
0x3917	PWM_CTRL_17	0x00	RW	Bit[7:0]: led_average_l_low_reg[7:0]

table A-11 global shutter control registers (sheet 7 of 8)

address	register name	default value	R/W	description
0x3918	PWM_CTRL_18	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: average_low_reg[9:8]
0x3919	PWM_CTRL_19	0x00	RW	Bit[7:0]: average_low_reg[7:0]
0x391A	PWM_CTRL_1A	0x00	RW	Bit[7:0]: led_duty_cycle_slope_reg
0x391B	PWM_CTRL_1B	0x74	RW	Bit[7:0]: led_pwm_ctrl1
0x391C	PWM_CTRL_1C	0x00	RW	Bit[7:0]: led_pwm_ctrl0
0x391D	PWM_CTRL_1D	0x10	RW	Bit[7:3]: Reserved Bit[2]: strobe_frame_vs_sel Bit[1]: Reserved Bit[0]: pwm_polarity
0x391E~ 0x391F	RSVD	–	–	Reserved
0x3920	PWM_CTRL_20	0xA5	RW	Bit[7:0]: strobe_pattern[7:0]
0x3921	PWM_CTRL_21	0x00	RW	Bit[7]: strobe_frame_sign_bit 0: Positive delay 1: Negative delay Bit[6:0]: strobe_frame_shift[30:24]
0x3922	PWM_CTRL_22	0x00	RW	Bit[7:0]: strobe_frame_shift[23:16]
0x3923	PWM_CTRL_23	0x00	RW	Bit[7:0]: strobe_frame_shift[15:8]
0x3924	PWM_CTRL_24	0x05	RW	Bit[7:0]: strobe_frame_shift[7:0]
0x3925	PWM_CTRL_25	0x00	RW	Bit[7:0]: Div value[31:24]
0x3926	PWM_CTRL_26	0x00	RW	Bit[7:0]: Div value[23:16]
0x3927	PWM_CTRL_27	0x00	RW	Bit[7:0]: Div value[15:8]
0x3928	PWM_CTRL_28	0x1A	RW	Bit[7:0]: Div value[7:0]
0x3929	PWM_CTRL_29	0x01	RW	Bit[7:0]: r_strobe_row_st[15:8]
0x392A	PWM_CTRL_2A	0xB4	RW	Bit[7:0]: r_strobe_row_st[7:0]
0x392B	PWM_CTRL_2B	0x00	RW	Bit[7:0]: r_strobe_cs_st[15:8]
0x392C	PWM_CTRL_2C	0x10	RW	Bit[7:0]: r_strobe_cs_st[7:0]
0x392D	PWM_CTRL_2D	0x05	RW	Bit[7:0]: step_onerow_man[15:8]
0x392E	PWM_CTRL_2E	0xF2	RW	Bit[7:0]: step_onerow_man[7:0]

table A-11 global shutter control registers (sheet 8 of 8)

address	register name	default value	R/W	description
0x392F	PWM_CTRL_2E	0x40	RW	Bit[7]: r_strobe_frm_pwen Bit[6]: r_strobe_frm_pwst Bit[5]: r_strobe_pol Bit[4]: r_strobe_step_pix Bit[3]: r_step_onerow_precision_man Bit[2:0]: r_strobe_st_opt
0x3930	PWM_CTRL_30	–	R	Bit[7:0]: led_duty_cycle_low[15:8]
0x3931	PWM_CTRL_31	–	R	Bit[7:0]: led_duty_cycle_low[7:0]
0x3932	PWM_CTRL_32	–	R	Bit[7:0]: Div value[15:8]
0x3933	PWM_CTRL_33	–	R	Bit[7:0]: Div value[7:0]

A.2.11 OTP [0x3D80 - 0x3D95]

table A-12 OTP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3D80	OTP_PROGRAM_CTRL	–	RW	Bit[7]: OTP_wr_busy (read only) Bit[6:1]: Not used Bit[0]: OTP_program_enable (write only)
0x3D81	OTP_LOAD_CTRL	–	RW	Bit[7]: OTP_rd_busy (read only) Bit[6]: Not used Bit[5]: OTP_bist_error (read only) Bit[4]: OTP_bist_done (read only) Bit[3]: Not used Bit[2]: bist_result_clr (write only) Bit[1]: autoload_m (write only) Bit[0]: OTP_load_enable (write only)
0x3D82	OTP_PGM_PULSE	0x65	RW	Program Strobe Pulse Width Unit: 8×system Clock Period
0x3D83	OTP_LOAD_PULSE	0x06	RW	Load Strobe Pulse Width Unit: System Clock Period
0x3D84	OTP_MODE_CTRL	0x00	RW	Bit[7]: Program disable 0: Not used 1: Disable Bit[6]: Mode select 0: Auto mode 1: Manual mode Bit[5:1]: Reserved Bit[0]: bank_sram_switch

table A-12 OTP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3D85	OTP_REG85	0x1B	RW	Bit[7]: Debug mode Bit[6]: OTP BIST compare value Bit[5]: OTP BIST mode select Bit[4]: OTP BIST enable Bit[3:0]: Reserved
0x3D86	SRAM_TEST_ SIGNALS	0x0F	RW	Bit[7:5]: Not used Bit[4]: sram_TEST Bit[3]: Not used Bit[2:0]: sram_RM
0x3D87	OTP_PS2CS	0x0A	RW	OTP PS to CSB Delay Unit: System Clock Period
0x3D88	OTP_START_ ADDRESS	0x00	RW	OTP Start High Address for Manual Mode
0x3D89	OTP_START_ ADDRESS	0x00	RW	OTP Start Low Address for Manual Mode
0x3D8A	OTP_EN_ADDRESS	0x00	RW	OTP End High Address for Manual Mode
0x3D8B	OTP_END_ ADDRESS	0x00	RW	OTP End Low Address for Manual Mode
0x3D8C~ 0x3D8D	RSVD	–	–	Reserved
0x3D8E	OTP_BIST_ERR_ ADDRESS	–	R	OTP Check Error Address High
0x3D8F	OTP_BIT_ERR_ ADDRESS	–	R	OTP Check Error Address Low
0x3D90	OTP BASE ADDR H	0x00	RW	OTP Base Address H
0x3D91	OTP BASE ADDR L	0x00	RW	OTP Base Address L
0x3D92	PROGRAM CTRL	0xE2	RW	Bit[7:4]: t_pgenb_end Bit[3:0]: t_pgenb_start
0x3D93	RSVD	–	–	Reserved
0x3D94	OTP_STROBE_GAP _PGM	0x12	RW	Gap Between Strobe Pulse When Programming
0x3D95	OTP_STROBE_GAP _LOAD	0x06	RW	Gap Between Strobe Pulse When Loading

A.2.12 BLC [0x4000 - 0x4017, 0x4020 - 0x403F, 0x4042 - 0x4049]

table A-13 BLC control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x4000	BLC_CTRL_00	0xCF	RW	Bit[7:4]: r_off_avg_weight_o Bit[3]: r_target_adj_dis_o Bit[2]: r_off_cmp_en_o Bit[1]: r_dither_en_o Bit[0]: r_mf_en_o
0x4001	BLC_CTRL_01	0x20	RW	Bit[7:6]: r_hdr_option_o Bit[5]: r_kcoef_man_en_o Bit[4]: r_off_man_en_o Bit[3]: r_zero_ln_out_en_o Bit[2]: r_blk_ln_out_en_o Bit[1:0]: r_byp_mode_o
0x4002	BLC_CTRL_02	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: r_blk_lvl_target_o[10:8]
0x4003	BLC_CTRL_03	0x10	RW	Bit[7:0]: r_blk_lvl_target_o[7:0]
0x4004	BLC_CTRL_04	0x00	RW	Bit[7:4]: Not used Bit[3:0]: r_hwin_off_o[11:8]
0x4005	BLC_CTRL_05	0x02	RW	Bit[7:0]: r_hwin_off_o[7:0]
0x4006	BLC_CTRL_06	0x00	RW	Bit[7:4]: Not used Bit[3:0]: r_hwin_pad_o[11:8]
0x4007	BLC_CTRL_07	0x02	RW	Bit[7:0]: r_hwin_pad_o[7:0]
0x4008	BLC_CTRL_08	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: r_up_bl_start_o[3:0]
0x4009	BLC_CTRL_09	0x07	RW	Bit[7:4]: Reserved Bit[3:0]: r_up_bl_end_o[3:0]
0x400A	BLC_CTRL_0A	0xFF	RW	Bit[7:3]: Reserved Bit[2:0]: r_off_lim_th_o[10:8]
0x400B	BLC_CTRL_0B	0xFF	RW	Bit[7:0]: r_off_lim_th_o[7:0]
0x400C	BLC_CTRL_0C	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: r_dn_bl_start_o[3:0]
0x400D	BLC_CTRL_0D	0x07	RW	Bit[7:4]: Reserved Bit[3:0]: r_dn_bl_end_o[3:0]
0x400E	BLC_CTRL_0E	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: r_kcoef_man_o[10:8]
0x400F	BLC_CTRL_0F	0x80	RW	Bit[7:0]: r_kcoef_man_o[7:0]

table A-13 BLC control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x4010	BLC_CTRL_10	0x41	RW	Bit[7]: r_up_off_trig_en_o Bit[6]: r_gain_chg_trig_en_o Bit[5]: r_fmt_chg_trig_en_o Bit[4]: r_rst_trig_en_o Bit[3]: r_man_avg_en_o Bit[2]: r_man_trig_o Bit[1]: r_off_frz_en_o Bit[0]: r_off_always_up_o
0x4011	BLC_CTRL_11	0x7F	RW	Bit[7]: Reserved Bit[6]: r_off_chg_mf_en_o Bit[5]: r_fmt_chg_mf_en_o Bit[4]: r_gain_chg_mf_en_o Bit[3]: r_rst_mf_mode_o Bit[2]: r_off_chg_mf_mode_o Bit[1]: r_fmt_chg_mf_mode_o Bit[0]: r_gain_chg_mf_mode_o
0x4012	BLC_CTRL_12	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: r_rst_trig_fn_o
0x4013	BLC_CTRL_13	0x02	RW	Bit[7:6]: Reserved Bit[5:0]: r_fmt_trig_fn_o
0x4014	BLC_CTRL_14	0x02	RW	Bit[7:6]: Reserved Bit[5:0]: r_gain_trig_fn_o
0x4015	BLC_CTRL_15	0x02	RW	Bit[7:6]: Reserved Bit[5:0]: r_off_trig_fn_o
0x4016	BLC_CTRL_16	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: r_off_trig_th_o[10:8]
0x4017	BLC_CTRL_17	0x00	RW	Bit[7:0]: r_off_trig_th_o[7:0]
0x4020	BLC_CTRL_20	0x00	RW	Bit[7:0]: r_off_cmp_th000_o[7:0]
0x4021	BLC_CTRL_21	0x00	RW	Bit[7:0]: r_off_cmp_k000_o[7:0]
0x4022	BLC_CTRL_22	0x00	RW	Bit[7:0]: r_off_cmp_th001_o[7:0]
0x4023	BLC_CTRL_23	0x00	RW	Bit[7:0]: r_off_cmp_k001_o[7:0]
0x4024	BLC_CTRL_24	0x00	RW	Bit[7:0]: r_off_cmp_th010_o[7:0]
0x4025	BLC_CTRL_25	0x00	RW	Bit[7:0]: r_off_cmp_k010_o[7:0]
0x4026	BLC_CTRL_26	0x00	RW	Bit[7:0]: r_off_cmp_th011_o[7:0]
0x4027	BLC_CTRL_27	0x00	RW	Bit[7:0]: r_off_cmp_k011_o[7:0]
0x4028	BLC_CTRL_28	0x00	RW	Bit[7:0]: r_off_cmp_th100_o[7:0]
0x4029	BLC_CTRL_29	0x00	RW	Bit[7:0]: r_off_cmp_k100_o[7:0]
0x402A	BLC_CTRL_2A	0x00	RW	Bit[7:0]: r_off_cmp_th101_o[7:0]

table A-13 BLC control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x402B	BLC_CTRL_2B	0x00	RW	Bit[7:0]: r_off_cmp_k101_o[7:0]
0x402C	BLC_CTRL_2C	0x00	RW	Bit[7:0]: r_off_cmp_th110_o[7:0]
0x402D	BLC_CTRL_2D	0x00	RW	Bit[7:0]: r_off_cmp_k110_o[7:0]
0x402E	BLC_CTRL_2E	0x00	RW	Bit[7:0]: r_off_cmp_th111_o[7:0]
0x402F	BLC_CTRL_2F	0x00	RW	Bit[7:0]: r_off_cmp_k111_o[7:0]
0x4030	BLC_CTRL_30	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: r_off_man000_o[10:8]
0x4031	BLC_CTRL_31	0x00	RW	Bit[7:0]: r_off_man000_o[7:0]
0x4032	BLC_CTRL_32	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: r_off_man001_o[10:8]
0x4033	BLC_CTRL_33	0x00	RW	Bit[7:0]: r_off_man001_o[7:0]
0x4034	BLC_CTRL_34	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: r_off_man010_o[10:8]
0x4035	BLC_CTRL_35	0x00	RW	Bit[7:0]: r_off_man010_o[7:0]
0x4036	BLC_CTRL_36	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: r_off_man011_o[10:8]
0x4037	BLC_CTRL_37	0x00	RW	Bit[7:0]: r_off_man011_o[7:0]
0x4038	BLC_CTRL_38	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: r_off_man100_o[10:8]
0x4039	BLC_CTRL_39	0x00	RW	Bit[7:0]: r_off_man100_o[7:0]
0x403A	BLC_CTRL_3A	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: r_off_man101_o[10:8]
0x403B	BLC_CTRL_3B	0x00	RW	Bit[7:0]: r_off_man101_o[7:0]
0x403C	BLC_CTRL_3C	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: r_off_man110_o[10:8]
0x403D	BLC_CTRL_3D	0x00	RW	Bit[7:0]: r_off_man110_o[7:0]
0x403E	BLC_CTRL_3E	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: r_off_man111_o[10:8]
0x403F	BLC_CTRL_3F	0x00	RW	Bit[7:0]: r_off_man111_o[7:0]

table A-13 BLC control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x4042	BLC_CTRL_42	0x11	RW	Bit[7]: r_format_trig_beh_o Bit[6]: r_gain_trig_beh_o Bit[5]: r_slope_man_en_o Bit[4]: r_slope_en_o Bit[3:2]: r_manu_cvdn_out_en_o Bit[1]: r_lim_off_en_o Bit[0]: r_mf_dn_en_o
0x4043	BLC_CTRL_43	0x50	RW	Bit[7]: r_2bits_precision_en_o Bit[6]: r_bot_blk_ln_en_o Bit[5]: r_dn_off_trig_en_o Bit[4]: r_byp_clip_en_o Bit[3]: r_cvdn_blc_en_man_o Bit[2]: r_cvdn_blc_en_o Bit[1]: r_dc_blc_en_man_o Bit[0]: r_dc_blc_en_o
0x4044	BLC_CTRL_44	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: r_rnd_gain_th_o[9:8]
0x4045	BLC_CTRL_45	0x20	RW	Bit[7:0]: r_rnd_gain_th_o[7:0]
0x4046	BLC_CTRL_46	0x00	RW	Bit[7:0]: r_thre_o[7:0]
0x4047	BLC_CTRL_47	0x00	RW	Bit[7]: r_thre_en_o Bit[6:2]: Reserved Bit[1:0]: r_thre_o[9:8]
0x4048	BLC_CTRL_48	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: r_thre_man_o[9:8]
0x4049	BLC_CTRL_49	0x00	RW	Bit[7:0]: r_thre_man_o[7:0]

A.2.13 isp_fc [0x4240 - 0x4244]

table A-14 isp_fc control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4240	FC CTRL00	0x00	RW	Bit[7:4]: Not used Bit[3]: sof_sel Bit[2]: fcnt_eof_sel Bit[1]: fcnt_mask_dis Bit[0]: fcnt_reset
0x4241	FRAME ON NUM	0x00	RW	Bit[7:4]: Not used Bit[3:0]: frame_on_number

table A-14 isp_fc control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4242	FRAME OFF NUM	0x00	RW	Bit[7:4]: Not used Bit[3:0]: frame_off_number
0x4243	FC CTRL03	0x00	RW	Bit[7]: Not used Bit[6]: rblue_mask_dis Bit[5]: data_mask_dis Bit[4]: valid_mask_dis Bit[3]: href_mask_dis Bit[2]: eof_mask_dis Bit[1]: sof_mask_dis Bit[0]: all_mask_dis
0x4244	FRAME COUNTER	–	R	Frame Counter

A.2.14 format [0x4300 - 0x4307, 0x4311 - 0x4316, 0x4320 - 0x4329]

table A-15 format registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4300	CLIP MAX H	0xFF	RW	Bit[7:0]: clip_max[9:2] Clip max value high byte
0x4301	CLIP MIN H	0x00	RW	Bit[7:0]: clip_min[9:2] Clip min value high byte
0x4302	CLIP LOW	0x0C	RW	Bit[7:4]: Not used Bit[3:2]: clip_max[1:0] Clip max value low byte Bit[1:0]: clip_min[1:0] Clip min value low byte
0x4303	TEST EN	0x00	RW	Bit[7:3]: Not used Bit[2]: r_moto_tst_en Bit[1]: r_tst_bit8 Bit[0]: r_moto_tst_md
0x4304	TEST CTRL 04	0x08	RW	Bit[7]: Not used Bit[6:4]: data_bit_swap Bit[3]: tst_full_win Bit[2:0]: Reserved
0x4305~ 0x4307	RSVD	–	–	Reserved
0x4311	VSYNC TRIGGER DLY H	0x04	RW	VSYNC Trigger Point to VSYNC Positive Edge Delay, MSB

table A-15 format registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4312	VSYNC TRIGGER DLY L	0x00	RW	VSYNC Trigger Point to VSYNC Positive Edge Delay, LSB
0x4313	VSYNC CTRL	0x00	RW	Bit[7:5]: Not used Bit[4]: r_vsync_pol Bit[3:2]: r_vsyncout_sel Bit[1]: r_vsync3_mod Bit[0]: r_vsync2_mod
0x4314	VSYNC WIDTH H	0x00	RW	VSYNC Width in Terms of Pixel Numbers, MSB
0x4315	VSYNC WIDTH M	0x01	RW	VSYNC Width in Terms of Pixel Numbers, Middle Byte
0x4316	VSYNC WIDTH L	0x00	RW	VSYNC Width in Terms of Pixel Numbers, LSB
0x4320	TEST PATTERN CTRL	0x80	RW	Bit[7:6]: pixel_order 00: GR/BG 01: RG/GB 10: BG/GR 11: GB/RG Bit[5]: byte_swap Bit[4]: bit_reverse Bit[3:2]: Reserved Bit[1]: solid_color_en Bit[0]: pn9_en
0x4321	RSVD	–	–	Reserved
0x4322	TEST DATA, BLUE	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Blue channel test data[9:8]
0x4323	TEST DATA, BLUE	0x00	RW	Bit[7:0]: Blue channel test data[7:0]
0x4324	TEST DATA, GB	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Gb channel test data[9:8]
0x4325	TEST DATA, GB	0x00	RW	Bit[7:0]: Gb channel test data[7:0]
0x4326	TEST DATA, GR	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Gr channel test data[9:8]
0x4327	TEST DATA, GR	0x00	RW	Bit[7:0]: Gr channel test data[7:0]
0x4328	TEST DATA, RED	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Red channel test data[9:8]
0x4329	TEST DATA, RED	0x00	RW	Bit[7:0]: Red channel test data[7:0]

A.2.15 TPM [0x4400 - 0x4424]

table A-16 TPM registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4400	SLOPE H	0x3E	RW	Bit[7:0]: r_tpm_slope[15:8]
0x4401	SLOPE L	0xC8	RW	Bit[7:0]: r_tpm_slope[7:0]
0x4402	OFFSET 3	0xBA	RW	Bit[7:0]: r_tpm_offset_3
0x4403	OFFSET 2	0xE4	RW	Bit[7:0]: r_tpm_offset_2
0x4404	OFFSET 1	0x7A	RW	Bit[7:0]: r_tpm_offset_1
0x4405	OFFSET 0	0xE2	RW	Bit[7:0]: r_tpm_offset_0
0x4406	TPM CTRL 06	0x88	RW	Bit[7:4]: r_div Bit[3:1]: db_period Bit[0]: clk_rev Reverse output clock
0x4407	TPM CTRL 07	0x31	RW	Bit[7]: Stall Bit[6]: int_on_failure Bit[5]: r_sof_update_en Bit[4]: tpm_cont Continuous updating Bit[3]: pd_tpm_snr Bit[2]: r_format_slope Bit[1]: mul_siv_sel Bit[0]: r_shift_ave
0x4408	TPM CTRL 08	0x23	RW	Bit[7:5]: Not used Bit[4:0]: shift_bit
0x4409	TPM CTRL 09	0xDF	RW	Bit[7]: Not used Bit[6]: alarm_en Bit[5]: calc_para_restart Bit[4]: calc_para_mode Bit[3]: tpm_en_0 Bit[2]: tpm_en_1 Bit[1]: tpm_use_0 Bit[0]: tpm_use_1
0x440A	DB LOW H	0x78	RW	Bit[7:0]: db_low[15:8]
0x440B	DB LOW L	0x98	RW	Bit[7:0]: db_low[7:0]
0x440C	DB HIGH H	0xCA	RW	Bit[7:0]: db_high[15:8]
0x440D	DB HIGH L	0x30	RW	Bit[7:0]: db_high[7:0]
0x440E	MAX DIFFERENCE	0x04	RW	Bit[7:0]: Max difference between two temperature sensors to trigger alarm
0x440F	TPM LOW INTEGER	0xE8	RW	Bit[7:0]: tpm_low, integer

table A-16 TPM registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4410	TPM LOW DECIMAL	0x00	RW	Bit[7:0]: tpm_low, decimal
0x4411	TPM HIGH INTEGER	0x78	RW	Bit[7:0]: tpm_high, integer
0x4412	TPM HIGH DECIMAL	0x00	RW	Bit[7:0]: tpm_high, decimal
0x4413	TPM MIN	0x00	RW	Bit[7:0]: Minimum temperature value
0x4414	TPM MAX	0xFF	RW	Bit[7:0]: Maximum temperature value
0x4415	TEST CYCLE HIGH	0x00	RW	Bit[7:0]: Number of test cycles[15:8]
0x4416	TEST CYCLE LOW	0x20	RW	Bit[7:0]: Number of test cycles[7:0]
0x4417	TPM2 INTEGER	–	R	Bit[7:0]: Temperature integer
0x4418	TPM2 DECIMAL	–	R	Bit[7:0]: Temperature decimal
0x4419	DB NUMBER	–	R	Bit[7:0]: db_number
0x441A	TPM A CALC HIGH	–	R	Bit[7:0]: Temperature A smul_result[15:8]
0x441B	TPM A CALC LOW	–	R	Bit[7:0]: Temperature A smul_result[7:0]
0x441C	TPM B CALC 3	–	R	Bit[7:0]: Temperature B smul_result[31:24]
0x441D	TPM B CALC 2	–	R	Bit[7:0]: Temperature B smul_result[23:16]
0x441E	TPM B CALC 1	–	R	Bit[7:0]: Temperature B smul_result[15:8]
0x441F	TPM B CALC 0	–	R	Bit[7:0]: Temperature B smul_result[7:0]
0x4420	DB REAL 0 H	–	R	Bit[7:0]: Temperature A db_real[15:8]
0x4421	DB REAL 0 L	–	R	Bit[7:0]: Temperature A db_real[7:0]
0x4422	DB REAL 1 H	–	R	Bit[7:0]: Temperature B db_real[15:8]
0x4423	DB REAL 1 L	–	R	Bit[7:0]: Temperature B db_real[7:0]
0x4424	ALARM	–	R	Alarm Flag

A.2.16 FC [0x 4440- 0x444B]

table A-17 FC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4440~ 0x4441	RSVD	–	–	Reserved

table A-17 FC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4442	CTRL2	0x04	RW	Bit[7:5]: Reserved Bit[4:2]: trigger_source_select 001: SOF 011: EOF 100: vblank_rise 101: vblank_fall 110: Scheduled Others: Undefined Bit[1:0]: Reserved
0x4443	RSVD	–	–	Reserved
0x4444	ROW SEL0	0x00	RW	Bit[7:0]: row_sel[15:8]
0x4445	ROW SEL1	0x00	RW	Bit[7:0]: row_sel[7:0]
0x4446	COL SEL0	0x00	RW	Bit[7:0]: column_sel[15:8]
0x4447	COL SEL1	0x00	RW	Bit[7:0]: column_sel[7:0]
0x4448~ 0x444B	FRAME COUNTER	–	R	Frame Counter

A.2.17 column_sync [0x4500 - 0x450F]

table A-18 column_sync registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4500	COL_SYNC_00	0x72	RW	Bit[7]: Reserved Bit[6:4]: FIFO read delay Bit[3]: Reserved Bit[2]: Rblue rev Bit[1]: Reserved Bit[0]: srclk_inv
0x4501	COL_SYNC_01	0x00	RW	Bit[7:5]: Reserved Bit[4]: r_fix_start_eol for sync_fifo Bit[3:2]: Reserved Bit[1]: mirror_man_enable Bit[0]: mirror_man
0x4502	COL_SYNC_02	0x00	RW	Bit[7:5]: Reserved Bit[4:3]: r_hskip2_opt Bit[2]: r_hskip4_en Bit[1]: r_hskip2_en Bit[0]: swap_sram_input_data from D[0:3] to D[3:0]

table A-18 column_sync registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4503	COL_SYNC_03	0x00	RW	Bit[7]: r_hskip_man_en Bit[6:4]: r_hbin4_opt Bit[3:2]: Not used Bit[1:0]: r_hbin2_opt
0x4504	COL_SYNC_04	0x00	RW	Bit[7:0]: r_sync_fifo_read_dly[15:8]
0x4505	COL_SYNC_05	0x20	RW	Bit[7:0]: r_sync_fifo_read_dly[7:0]
0x4506	COL_SYNC_06	0x0F	RW	Bit[7:6]: Reserved Bit[5]: r_sram_rme Bit[4]: r_sram_test1 Bit[3:0]: r_sram_rm
0x4507	COL_SYNC_07	0x0F	RW	Bit[7:6]: Reserved Bit[5]: r_sram_rme Bit[4]: r_sram_test1 Bit[3:0]: r_sram_rm
0x4508	COL_SYNC_08	0x00	RW	Bit[7:4]: Reserved Bit[3]: r_hbin4_opt_man_en Bit[2]: r_hbin2_opt_man_en Bit[1]: r_hskip4_opt_man_en Bit[0]: r_hskip2_opt_man_en
0x4509	COL_SYNC_09	0x00	RW	Bit[7]: r_bw_en Bit[6:4]: Reserved Bit[3:0]: r_hskip4_opt
0x450A	RSVD	–	–	Reserved
0x450B	COL_SYNC_0B	0x00	RW	Bit[7]: Reserved Bit[6]: chn_swap Bit[5]: rd_mem_ah Bit[4]: Reserved Bit[3:0]: rblue_opt[3:0]
0x450C~ 0x450F	RSVD	–	–	Reserved

A.2.18 VFIFO [0x4600 - 0x4606]

table A-19 VFIFO registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4600	VFIFO READ START	0x00	RW	VFIFO Read Start in Manual Mode High Byte
0x4601	VFIFO READ START	0x80	RW	VFIFO Read Start in Manual Mode Low Byte

table A-19 VFIFO registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4602	VFIFO CTRL02	0xF2	RW	Bit[7:4]: SRAM RM Bit[3]: SRAM TEST1 Bit[2]: Reserved Bit[1]: frame_rst_en Bit[0]: RAM bypass enable
0x4603	VFIFO CTRL03	0x00	RW	Bit[7:2]: Not used Bit[1]: discard_ro Discard previous CRC result Bit[0]: rst_crc_err_cnt Reset VFIFO CRC error counter
0x4604	VFIFO CTRL04	0x00	RW	Bit[7:0]: CRC error count threshold
0x4605	VFIFO CTRL05	–	R	Bit[7:5]: Not used Bit[4]: sram_always_on Bit[3:0]: Ready low tp number
0x4606	VFIFO STATUS	–	R	Bit[7:2]: Not used Bit[1]: ram_full Bit[0]: ram_empty

A.2.19 DVP [0x4700 - 0x4711]

table A-20 DVP registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4700	MODE_SEL	0x04	RW	Bit[7]: ccir656_fv_sel Bit[6]: ccir656_vblank_generate from VSYNC Useful for scaling case, use VSYNC to generate sync code at v-blank Bit[5]: ccir656_blank_seq H-blank toggle sequence 0: 80, 10 1: 10, 80 Bit[4]: ccir656_blank_enable Enable data toggle at h-blank Bit[3]: ccir656_v_select 0: Vertical blanking sync code start after end of last active line 1: Vertical blanking sync code start at end of last active line Bit[2]: ccir656_f_value 0: 656's sync code fixed at field 0 1: 656's sync code fixed at field 1 Bit[1]: ccir656_mode_enable Bit[0]: hsync_mode_enable
0x4701	VSYNCOUT_SEL	0x00	RW	VSYNCOUT_SEL 00: eof_o 01: Output gpo_vsync 10: Output hsync_o 11: eof_o
0x4702~ 0x4703	VSYNC_RISE_LNT	0x02	RW	Line Counter in IP These Two Registers Control Rising Position of VSYNC
0x4704~ 0x4705	VSYNC_FALL_LNT	0x06	RW	Falling Position of VSYNC
0x4706~ 0x4707	VSYNC_CHG_PCNT	0x10	RW	VSYNC Change Position Indicated by Pixel Position
0x4708	POLARITY_CTRL	0x09	RW	Bit[7]: Clock DDR mode enable Bit[6]: hts_man_en Bit[5]: VSYNC gate enable Bit[4]: HREF gate enable Bit[3]: r_fo_nofrst Bit[2]: HREF polarity Bit[1]: VSYNC polarity Bit[0]: PCLK polarity

table A-20 DVP registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4709	MOTO_ORDER	0x00	RW	Bit[7]: Reserved Bit[6:4]: Data bit swap Bit[3]: Test mode Bit[2]: Test bit 10 Bit[1]: Test bit 8 Bit[0]: Test mode enable
0x470A~ 0x470B	HSYNC_RD_ST	0x40	RW	HSYNC Start Position
0x470C	R_READ_CTRL	0x81	RW	Bit[7:4]: hsync_rd_st_offs Bit[3]: Not used Bit[2]: hsync_st_man Bit[1]: first_lv_sel Bit[0]: r_lpcnt_free
0x470D	R_HSYNC_HEADER	0x04	RW	Bit[7:0]: r_hsync_header
0x470E	R_HSYNC_TRAIL	0x00	RW	Bit[7:0]: r_hsync_trail
0x470F	BYP_SEL	0x00	RW	Bit[7:5]: Reserved Bit[4]: href_sel Bit[3:0]: bypass_sel
0x4710~ 0x4711	HTS_PCLK_MAN	–	–	hts_pclk_man

A.2.20 MIPI [0x4800 - 0x4808, 0x4810 - 0x4839, 0x483C - 0x484F]

table A-21 MIPI control registers (sheet 1 of 8)

address	register name	default value	R/W	description
0x4800	MIPI CTRL00	0x04	RW	Bit[7]: r_sc_valid_opt_o 0: Not used 1: MIPI always in high speed mode Bit[6]: Reserved Bit[5]: gate_sc_en 0: Clock lane is free running 1: Gate clock lane when there is no packet to transmit Bit[4]: line_sync_en 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[3]: Reserved Bit[2]: pclk_inv_o Bit[1]: first_bit Change clk_lane first bit 0: Output 8'h55 1: Output 8'hAA Bit[0]: LPX_select for pclk domain 0: Auto calculate t_lpx_p, unit pclk2x period 1: Use lpx_p_min
0x4801	RSVD	–	–	Reserved

table A-21 MIPI control registers (sheet 2 of 8)

address	register name	default value	R/W	description
0x4802	MIPI CTRL02	0x00	RW	Bit[7]: hs_prepare_sel 0: Auto calculate T_hs_prepare, unit pclk2x 1: Use hs_prepare_min_o[7:0] Bit[6]: clk_prepare_sel 0: Auto calculate T_clk_prepare, unit pclk2x 1: Use clk_prepare_min_o[7:0] Bit[5]: clk_post_sel 0: Auto calculate T_clk_post, unit pclk2x 1: Use clk_post_min_o[7:0] Bit[4]: clk_trail_sel 0: Auto calculate T_clk_trail, unit pclk2x 1: Use clk_trail_min_o[7:0] Bit[3]: hs_exit_sel 0: Auto calculate T_hs_exit, unit pclk2x 1: Use hs_exit_min_o[7:0] Bit[2]: hs_zero_sel 0: Auto calculate T_hs_zero, unit pclk2x 1: Use hs_zero_min_o[7:0] Bit[1]: hs_trail_sel 0: Auto calculate T_hs_trail, unit pclk2x 1: Use hs_trail_min_o[7:0] Bit[0]: clk_zero_sel 0: Auto calculate T_clk_zero, unit pclk2x 1: Use clk_zero_min_o[7:0]
0x4803	MIPI CTRL03	0x30	RW	Bit[7:6]: Not used Bit[5]: r_crc_1d_en Bit[4]: fifo_rd_spd_ol Bit[3]: manu_offset_o t_period manual offset, SMIA Bit[2]: r_manu_half2one, SMIA Bit[1:0]: Reserved
0x4804	RSVD	–	–	Reserved

table A-21 MIPI control registers (sheet 3 of 8)

address	register name	default value	R/W	description
0x4805	MIPI CTRL05	0x00	RW	Bit[7:4]: Not used Bit[3]: lpda_retim_manu_o Bit[2]: lpda_retim_sel_o 0: Not used 1: Manual Bit[1]: lpck_retim_manu_o Bit[0]: lpck_retim_sel_o 0: Not used 1: Manual
0x4806	MIPI CTRL06	0x00	RW	Bit[7:5]: Not used Bit[4]: pu_mark_en_o Power up mark1 enable Bit[3]: mipi_remot_rst Bit[2]: mipi_susp Bit[1]: smia_lane_ch_en Bit[0]: tx_lsb_first 0: High bit first 1: Low power transmit low bit first
0x4807	MIPI CTRL07	0x03	RW	Bit[7:4]: Not used Bit[3:0]: sw_t_lpx Ultra low power T_lpx
0x4808	MIPI CTRL08	0x18	RW	Bit[7:0]: wkup_dly Mark1 wakeup delay/2^10
0x4810	FCNT MAX	0xFF	RW	Bit[7:0]: fcnt_max[15:8] Maximum frame counter of frame sync short packet
0x4811	FCNT MAX	0xFF	RW	Bit[7:0]: fcnt_max[7:0] Maximum frame counter of frame sync short packet
0x4812	RSVD	–	–	Reserved
0x4813	MIPI CTRL13	0x00	RW	Bit[7:3]: Not used Bit[2]: vc_sel Bit[1:0]: VC ID
0x4814	MIPI CTRL14	0x2A	RW	Bit[7]: Not used Bit[6]: lpkt_dt_sel 0: Use mipi_dt 1: Use dt_man_o as long packet data Bit[5:0]: dt_man Manual data type
0x4815~ 0x4817	RSVD	–	–	Reserved

table A-21 MIPI control registers (sheet 4 of 8)

address	register name	default value	R/W	description
0x4818	HS ZERO MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_zero_min[9:8] Minimum value of hs_zero, unit ns
0x4819	HS ZERO MIN	0x70	RW	Bit[7:0]: hs_zero_min[7:0] Minimum value of hs_zero hs_zero_real = hs_zero_min_o + Tui*ui_hs_zero_min_o
0x481A	HS TRAIL MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_trail_min[9:8] Minimum value of hs_trail, unit ns
0x481B	HS TRAIL MIN	0x3C	RW	Bit[7:0]: hs_trail_min[7:0] Minimum value of hs_trail hs_trail_real = hs_trail_min_o + Tui*ui_hs_trail_min_o
0x481C	CLK ZERO MIN	0x01	RW	Bit[7:2]: Not used Bit[1:0]: clk_zero_min[9:8] Minimum value of clk_zero, unit ns
0x481D	CLK ZERO MIN	0x2C	RW	Bit[7:0]: clk_zero_min[7:0] Minimum value of clk_zero clk_zero_real = clk_zero_min_o + Tui*ui_clk_zero_min_o
0x481E	CLK PREPARE MAX	0x5F	RW	Bit[7:0]: clk_prepare_max[7:0] Maximum value of clk_prepare, unit ns
0x481F	CLK PREPARE MIN	0x26	RW	Bit[7:0]: clk_prepare_min[7:0] Minimum value of clk_prepare clk_prepare_real = clk_prepare_min_o + Tui*ui_clk_prepare_min_o
0x4820	CLK POST MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: clk_post_min[9:8] Minimum value of clk_post, unit ns
0x4821	CLK POST MIN	0x3C	RW	Bit[7:0]: clk_post_min[7:0] Minimum value of clk_post clk_post_real = clk_post_min_o + Tui*ui_clk_post_min_o
0x4822	CLK TRAIL MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: clk_trail_min[9:8] Minimum value of clk_trail, unit ns

table A-21 MIPI control registers (sheet 5 of 8)

address	register name	default value	R/W	description
0x4823	CLK TRAIL MIN	0x3C	RW	Bit[7:0]: clk_trail_min[7:0] Minimum value of clk_trail clk_trail_real = clk_trail_min_o + Tui*ui_clk_trail_min_o
0x4824	LPX P MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: lpx_p_min[9:8] Minimum value of lpx_p, unit ns
0x4825	LPX P MIN	0x32	RW	Bit[7:0]: lpx_p_min[7:0] Minimum value of lpx_p lpx_p_real = lpx_p_min_o + Tui*ui_lpx_p_min_o
0x4826	HS PREPARE MIN	0x32	RW	Bit[7:0]: hs_prepare_min[7:0] Minimum value of hs_prepare, unit ns
0x4827	HS PREPARE MAX	0x55	RW	Bit[7:0]: hs_prepare_max[7:0] Maximum value of hs_prepare hs_prepare_real = hs_prepare_max_o + Tui*ui_hs_prepare_max_o
0x4828	HS EXIT MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_exit_min[9:8] Minimum value of hs_exit, unit ns
0x4829	HS EXIT MIN	0x64	RW	Bit[7:0]: hs_exit_min[7:0] Low byte of minimum value of hs_exit hs_exit_real = hs_exit_min_o + Tui*ui_hs_exit_min_o
0x482A	UI HS ZERO MIN	0x06	RW	Bit[7:6]: Not used Bit[5:0]: ui_hs_zero_min[5:0] Minimum UI value of hs_zero, unit UI
0x482B	UI HS TRAIL MIN	0x04	RW	Bit[7:6]: Not used Bit[5:0]: ui_hs_trail_min[5:0] Minimum UI value of hs_trail, unit UI
0x482C	UI CLK ZERO MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_clk_zero_min[5:0] Minimum UI value of clk_zero, unit UI
0x482D	UI CLK PREPARE	0x00	RW	Bit[7:4]: ui_clk_prepare_max Maximum UI value of clk_prepare, unit UI Bit[3:0]: ui_clk_prepare_min Minimum UI value of clk_prepare, unit UI

table A-21 MIPI control registers (sheet 6 of 8)

address	register name	default value	R/W	description
0x482E	UI CLK POST MIN	0x34	RW	Bit[7:6]: Not used Bit[5:0]: ui_clk_post_min[5:0] Minimum UI value of clk_post, unit UI
0x482F	UI CLK TRAIL MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_clk_trail_min[5:0] Minimum UI value of clk_trail, unit UI
0x4830	UI LPX P MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_lpx_p_min[5:0] Minimum UI value of lpx_p (pclk2x domain), unit UI
0x4831	UI HS PREPARE	0x64	RW	Bit[7:4]: ui_hs_prepare_max Maximum UI value of hs_prepare, unit UI Bit[3:0]: ui_hs_prepare_min Minimum UI value of hs_prepare, unit UI
0x4832	UI HS EXIT MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_hs_exit_min[5:0] Minimum UI value of hs_exit, unit UI
0x4833	MIPI PKT STAR SIZE	0x10	RW	Bit[7:6]: Not used Bit[5:0]: r_rdy_mark
0x4834~ 0x4836	RSVD	–	–	Reserved
0x4837	PCLK PERIOD	0x14	RW	Bit[7:0]: pclk_period[7:0] Period of pclk2x, pclk_div=1, and 1-bit decimal
0x4838	MIPI LP GPIO0	0x00	RW	Bit[7]: lp_sel0 0: Auto generate mipi_lp_dir0_o 1: Use lp_dir_man0 to be mipi_lp_dir0_o Bit[6]: lp_dir_man0 0: Input 1: Output Bit[5]: lp_p0_o Bit[4]: lp_n0_o Bit[3]: lp_sel1 0: Auto generate mipi_lp_dir1_o 1: Use lp_dir_man1 to be mipi_lp_dir1_o Bit[2]: lp_dir_man1 0: Input 1: Output Bit[1]: lp_p1_o Bit[0]: lp_n1_o

table A-21 MIPI control registers (sheet 7 of 8)

address	register name	default value	R/W	description
0x4839	MIPI LP GPIO1	0x00	RW	Bit[7]: lp_sel2 0: Auto generate mipi_lp_dir2_o 1: Use lp_dir_man2 to be mipi_lp_dir2_o Bit[6]: lp_dir_man2 0: Input 1: Output Bit[5]: lp_p2_o Bit[4]: lp_n2_o Bit[3]: lp_sel3 0: Auto generate mipi_lp_dir3_o 1: Use lp_dir_man3 to be mipi_lp_dir3_o Bit[2]: lp_dir_man3 0: Input 1: Output Bit[1]: lp_p3_o Bit[0]: lp_n3_o
0x483A~ 0x483B	RSVD	–	–	Reserved
0x483C	MIPI CTRL3C	0x02	RW	Bit[7:4]: Not used Bit[3:0]: t_clk_pre Unit: pclk2x cycle
0x483D	MIPI LP GPIO4	0x00	RW	Bit[7]: lp_ck_sel0 0: Auto generate mipi_ck_lp_dir0_o 1: Use lp_ck_dir_man0 to be mipi_ck_lp_dir0_o Bit[6]: lp_ck_dir_man0 0: Input 1: Output Bit[5]: lp_ck_p0_o Bit[4]: lp_ck_n0_o Bit[3]: lp_ck_sel0 0: Auto generate mipi_ck_lp_dir0_o 1: Use lp_ck_dir_man0 to be mipi_ck_lp_dir0_o Bit[2]: lp_ck_dir_man0 0: Input 1: Output Bit[1]: lp_ck_p0_o Bit[0]: lp_ck_n0_o
0x483E	FCNT RD H	–	R	Fcnt RD H
0x483F	FCNT RD L	–	R	Fcnt RD L

table A-21 MIPI control registers (sheet 8 of 8)

address	register name	default value	R/W	description
0x484A	SEL MIPI CTRL4A	0x3F	RW	Bit[7:6]: Not used Bit[5]: slp_lp_pon_man_o Set for power up Bit[4]: slp_lp_pon_da Bit[3]: slp_lp_pon_ck Bit[2]: mipi_slp_man_st MIPI bus status manual control enable in sleep mode Bit[1]: clk_lane_state Bit[0]: data_lane_state
0x484B	MIPI OPTION	0x03	RW	Bit[7:4]: Not used Bit[3]: same_skewcal 0: Initial dskew calibration time controlled by 0x4853, periodic skew calibration time controlled by 0x4852 1: Initial and periodic skew calibration have same calibration time Bit[2]: line_st_sel_o 0: Line starts after HREF 1: Line starts after fifo_st Bit[1]: clk_start_sel_o 0: Clock starts after SOF 1: Clock starts after reset Bit[0]: sof_sel_o 0: Frame starts after HREF occurs 1: Frame starts after SOF
0x484C	MIPI CTRL 4C	0x00	RW	Bit[7:4]: Not used Bit[3]: smia_fcnt_i select Bit[2]: prbs_en Bit[1]: hs_test_only Bit[0]: set_frame_cnt_0
0x484D	TEST PATTEN DATA	0xB6	RW	Bit[7:0]: test_patten_data[7:0] Data lane test pattern
0x484E	FE DLY	0x10	RW	Bit[7:0]: r_fe_dly_o Last packet to frame end delay / 2
0x484F	TEST PATTERN CK DATA	0x55	RW	Bit[7:0]: Clock lane test pattern data

A.2.21 PSV [0x4F00 - 0x4F14]

table A-22 PSV control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4F00	PSV_CTRL	0x00	RW	Bit[7:4]: Reserved Bit[3]: psv_auto_on_dis 0: PSV mode auto enable if VTS > threshold 1: Disable PSV auto on mode, only depends on r_psv_mode_en Bit[2]: r_psv_mode_en Bit[1]: Reserved Bit[0]: psv_mode 0: Keep SCLK on (frame timing base on SCLK) 1: Shut off SCLK at blanking (frame timing switch to pad_clk domain)
0x4F01	AUTO_SLEEP_CTRL	0x00	RW	Bit[7:4]: Reserved Bit[3]: tc_sof_sync_en Bit[2]: vblkp_sync_dis Bit[1:0]: blank_retime_opt
0x4F02	HTS_PAD_CLK	0x00	RW	Bit[7:0]: hts_pad_clk[15:8]
0x4F03	HTS_PAD_CLK	0xB1	RW	Bit[7:0]: hts_pad_clk[7:0]
0x4F04	CS_CNT_INTIAL	0x00	RW	Bit[7:0]: cs_cnt_intial[15:8]
0x4F05	CS_CNT_INTIAL	0x0F	RW	Bit[7:0]: cs_cnt_intial[7:0]
0x4F06	STREAM_ST_OFFS	0x08	RW	Bit[7:0]: r_stream_st_offs[7:0]
0x4F07	PCHG_ST_OFFS	0x08	RW	Bit[7:0]: r_pchg_st_offs[7:0]
0x4F08	CLK_WINP_OFF	0x01	RW	Bit[7:4]: Not used Bit[3:0]: r_clk_winp_off[3:0]
0x4F09	STRM_REA OFFS	0x02	RW	Bit[7:4]: Not used Bit[3:0]: r_strm_rear_offs[3:0]
0x4F0A	PCHG_REA OFFS	0x02	RW	Bit[7:4]: Not used Bit[3:0]: r_pchg_rear_offs[3:0]
0x4F0B	RSVD	–	–	Reserved
0x4F0C	PSV_AUTO_ON_ THRESH	0x10	RW	Bit[7:0]: psv_auto_on_thresh[15:8]
0x4F0D	PSV_AUTO_ON_ THRESH	0x00	RW	Bit[7:0]: psv_auto_on_thresh[7:0]

table A-22 PSV control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4F0E~ 0x4F0F	RSVD	–	–	Reserved
0x4F10	ANA_PSV_PCH	0x00	RW	Bit[7:0]: ana_psv_pch[15:8]
0x4F11	ANA_PSV_PCH	0x18	RW	Bit[7:0]: ana_psv_pch[7:0]
0x4F12	ANA_PSV_STRM	0x0F	RW	Bit[7:0]: ana_psv_strm[15:8]
0x4F13	ANA_PSV_STRM	0x04	RW	Bit[7:0]: ana_psv_strm[7:0]
0x4F14	ANA_PSV_INV	0x00	RW	Bit[7:1]: Reserved Bit[0]: ana_psv_inv

A.2.22 isp_main [0x5000 - 0x5018, 0x5020 - 0x5027, 0x5030 - 0x5036]

table A-23 isp_main control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CTRL 00	0x9F	RW	Bit[7:6]: isp_sof_sel Bit[5]: isp_eof_sel Bit[4]: otp_dpc_en Bit[3]: dpc_en Bit[2]: dpc_buf_en Bit[1]: awbg_en Bit[0]: blc_en
0x5001	ISP CTRL 01	0x20	RW	Bit[7:6]: Reserved Bit[5]: ptdp_en Bit[4]: latch_en Bit[3]: r_size_man Bit[2]: r_pre_isp_raw_en Bit[1]: bypass_isp1 Bit[0]: bypass_isp0
0x5002	ISP CTRL 02	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: manual_x_addr_st[10:8]
0x5003	ISP CTRL 03	0x00	RW	Bit[7:0]: manual_x_addr_st[7:0]
0x5004	ISP CTRL 04	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: manual_y_addr_st[9:8]
0x5005	ISP CTRL 05	0x00	RW	Bit[7:0]: manual_y_addr_st[7:0]
0x5006	ISP CTRL 06	0x05	RW	Bit[7:3]: Reserved Bit[2:0]: manual_x_addr_end[10:8]
0x5007	ISP CTRL 07	0x0F	RW	Bit[7:0]: manual_x_addr_end[7:0]

table A-23 isp_main control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5008	ISP CTRL 08	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: manual_y_addr_end[9:8]
0x5009	ISP CTRL 09	0x2F	RW	Bit[7:0]: manual_y_addr_end[7:0]
0x500A~ 0x500F	RSVD	–	–	Reserved
0x5010	LINEAR GAIN	–	R	Bit[7:2]: Not used Bit[1:0]: AEC linear gain debug[9:8]
0x5011	LINEAR GAIN	–	R	Bit[7:0]: AEC linear gain debug[7:0]
0x5012~ 0x5017	RSVD	–	–	Reserved
0x5018	SENSOR BIAS	–	R	Sensor Bias Debug
0x5020	ISP_CTRL_20	0x00	RW	Bit[7]: Reserved Bit[6]: blc_px_man_en Bit[5:4]: blc_px_man Bit[3]: blc_vsync_sel Bit[2]: dig_gain_blc_man Bit[1:0]: dig_gain_blc
0x5021	ISP_CTRL_21	0x00	RW	Bit[7:4]: Reserved Bit[3]: r_blc_rblue_man_en Bit[2]: r_blc_rblue_man Bit[1]: r_blc_target_sel 0: blc_target[7:0] 1: blc_target[9:2] Bit[0]: r_bias_man_en
0x5022	ISP_CTRL_22	0x00	RW	Bit[7:0]: r_bias_man_value
0x5023	ISP_CTRL_23	0x00	RW	Bit[7:0]: otp_hsize_man[7:0]
0x5024	ISP_CTRL_24	0x00	RW	Bit[7:5]: dpc_dummy_num Bit[4:3]: Not used Bit[2:0]: otp_hsize_man[10:8]
0x5025	ISP_CTRL_26	0x00	RW	Bit[7]: otp_hszie_man_en Bit[6]: Reserved Bit[5:4]: ptdp_data_lshift Bit[3:2]: ptdp_data_rshift Bit[1]: ptdp_byp_clip_en Bit[0]: ptdp_in_sel

table A-23 isp_main control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5026	ISP_CTRL_26	0x00	RW	Bit[7]: x_bin_inv Bit[6]: y_bin_inv Bit[5]: x_bin4_man Bit[4]: y_bin4_man Bit[3:2]: Reserved Bit[1]: isp_bypass_win_off Bit[0]: isp_bypass_en
0x5027	ISP_CTRL_27	0x00	RW	Bit[7:4]: Reserved Bit[3]: addr_replace_en Bit[2:1]: output_size_man Bit[0]: Reserved
0x5030	ISP_CTRL_30	0x00	RW	Bit[7]: Reserved Bit[6]: isp_vsync_sel Bit[5:4]: dpc_px_man Bit[3]: dpc_px_man_en Bit[2]: dpc_bw_mode_en Bit[1]: dpc_size_man Bit[0]: Reserved
0x5031	ISP_CTRL_31	0x00	RW	Bit[7:0]: dpc_hsize_in[7:0]
0x5032	ISP_CTRL_32	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: dpc_hsize_in[10:8]
0x5033	ISP_CTRL_33	0x00	RW	Bit[7:0]: dpc_vsize_in[7:0]
0x5034	ISP_CTRL_34	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: dpc_vsize_in[9:8]
0x5035	ISP_CTRL_35	0x0F	RW	Bit[7]: Reserved Bit[6]: dpc_dis_clk_gt Bit[5]: dpc_sram_rme1 Bit[4]: dpc_sram_test1 Bit[3:0]: dpc_sram_rm1
0x5036	ISP_CTRL_36	0x8F	RW	Bit[7]: Reserved Bit[6]: dpc_dis_clk_gt Bit[5]: dpc_sram_rme1 Bit[4]: dpc_sram_test1 Bit[3:0]: dpc_sram_rm1

A.2.23 isp_win [0x5A00 - 0x5A2F]

table A-24 isp_win control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x5A00	XSTART MAN	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: x_start[10:8] Manual horizontal start for manual output window
0x5A01	XSTART MAN	0x00	RW	Bit[7:0]: x_start[7:0] Manual horizontal start for manual output window
0x5A02	YSTART MAN	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: y_start[9:8] Manual vertical start for manual output window
0x5A03	YSTART MAN	0x00	RW	Bit[7:0]: y_start[7:0] Manual vertical start for manual output window
0x5A04	XWIN MAN	0x05	RW	Bit[7:3]: Reserved Bit[2:0]: x_window[10:8] Manual horizontal window for manual output window
0x5A05	XWIN MAN	0x00	RW	Bit[7:0]: x_window[7:0] Manual horizontal window for manual output window
0x5A06	YWIN MAN	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: y_window[9:8] Manual vertical window for manual output window
0x5A07	YWIN MAN	0x20	RW	Bit[7:0]: y_window[7:0] Manual vertical window for manual output window

table A-24 isp_win control registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x5A08	WINC CTRL	0x86	RW	Bit[7]: r_out_size_sel 0: Initial XY size out 1: ROI XY size out Bit[6]: r_one_zone_en 0: 16 zones display 1: Single zone display enable Bit[5]: Reserved Bit[4]: win16_en 0: Not divided into 16 zones 1: 16 zones crop enable Bit[3]: win_valid_opt Bit[2]: emb_flag_sel Bit[1]: win_en_opt Bit[0]: win_man_en Manual window enable signal 0: Output window uses system parameters 1: Output window uses manual parameters which are set in registers 0x5A00~0x5A07
0X5A09	WINC_SEL	0x00	RW	Bit[7:3]: Reserved Bit[2:1]: roi_sel_man 00: Zone00 [00 01 02 03] 01: Zone05 [04 05 06 07] 10: Zone10 [08 09 10 11] 11: Zone15 [12 13 14 15] Bit[0]: roi_sel_man_en Manual signal zone select 0: Output zone is selected by GPIO pad 1: Output zone is selected by 0x5A09[2:1]
0x5A10	WIN16 XSTART0	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: win16_xstart0[10:8] First horizontal start for 16-window function
0x5A11	WIN16 XSTART0	0x00	RW	Bit[7:0]: win16_xstart0[7:0] First horizontal start for 16-window function
0x5A12	WIN16 XSTART1	0x00	RW	Bit[7:3]: Reserved Bit[2:0]: win16_xstart1[10:8] First horizontal start for 16-window function
0x5A13	WIN16 XSTART1	0x00	RW	Bit[7:0]: win16_xstart1[7:0] First horizontal start for 16-window function

table A-24 isp_win control registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x5A14	WIN16 XSTART2	0x02	RW	Bit[7:3]: Reserved Bit[2:0]: win16_xstart2[10:8] First horizontal start for 16-window function
0x5A15	WIN16 XSTART2	0x80	RW	Bit[7:0]: win16_xstart2[7:0] First horizontal start for 16-window function
0x5A16	WIN16 XSTART3	0x03	RW	Bit[7:3]: Reserved Bit[2:0]: win16_xstart3[10:8] First horizontal start for 16-window function
0x5A17	WIN16 XSTART3	0xC0	RW	Bit[7:0]: win16_xstart3[7:0] First horizontal start for 16-window function
0x5A18	WIN16 YSTART0	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: win16_ystart0[9:8] First horizontal start for 16-window function
0x5A19	WIN16 YSTART0	0x00	RW	Bit[7:0]: win16_ystart0[7:0] First horizontal start for 16-window function
0x5A1A	WIN16 YSTART1	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: win16_ystart1[9:8] First horizontal start for 16-window function
0x5A1B	WIN16 YSTART1	0x28	RW	Bit[7:0]: win16_ystart1[7:0] First horizontal start for 16-window function
0x5A1C	WIN16 YSTART2	0x01	RW	Bit[7:2]: Reserved Bit[1:0]: win16_ystart2[9:8] First horizontal start for 16-window function
0x5A1D	WIN16 YSTART2	0x90	RW	Bit[7:0]: win16_ystart2[7:0] First horizontal start for 16-window function
0x5A1E	WIN16 YSTART3	0x01	RW	Bit[7:2]: Reserved Bit[1:0]: win16_ystart3[9:8] First horizontal start for 16-window function
0x5A1F	WIN16 YSTART3	0x90	RW	Bit[7:0]: win16_ystart3[7:0] First horizontal start for 16-window function

table A-24 isp_win control registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x5A20	WIN16 XWIN0	0x05	RW	Bit[7:3]: Reserved Bit[2:0]: win16_xwindow0[10:8] First horizontal window for 16-window function
0x5A21	WIN16 XWIN0	0x00	RW	Bit[7:0]: win16_xwindow0[7:0] First horizontal window for 16-window function
0x5A22	WIN16 XWIN1	0x05	RW	Bit[7:3]: Reserved Bit[2:0]: win16_xwindow1[10:8] First horizontal window for 16-window function
0x5A23	WIN16 XWIN1	0x00	RW	Bit[7:0]: win16_xwindow1[7:0] First horizontal window for 16-window function
0x5A24	WIN16 XWIN2	0x02	RW	Bit[7:3]: Reserved Bit[2:0]: win16_xwindow2[10:8] First horizontal window for 16-window function
0x5A25	WIN16 XWIN2	0x80	RW	Bit[7:0]: win16_xwindow2[7:0] First horizontal window for 16-window function
0x5A26	WIN16 XWIN3	0x01	RW	Bit[7:3]: Reserved Bit[2:0]: win16_xwindow3[10:8] First horizontal window for 16-window function
0x5A27	WIN16 XWIN3	0x40	RW	Bit[7:0]: win16_xwindow3[7:0] First horizontal window for 16-window function
0x5A28	WIN16 YWIN0	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: win16_ywindow0[9:8] First horizontal window for 16-window function
0x5A29	WIN16 YWIN0	0x20	RW	Bit[7:0]: win16_ywindow0[7:0] First horizontal window for 16-window function
0x5A2A	WIN16 YWIN1	0x02	RW	Bit[7:2]: Reserved Bit[1:0]: win16_ywindow1[9:8] First horizontal window for 16-window function
0x5A2B	WIN16 YWIN1	0xD0	RW	Bit[7:0]: win16_ywindow1[7:0] First horizontal window for 16-window function

table A-24 isp_win control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x5A2C	WIN16 YWIN2	0x01	RW	Bit[7:2]: Reserved Bit[1:0]: win16_ywindow2[9:8] First horizontal window for 16-window function
0x5A2D	WIN16 YWIN2	0x68	RW	Bit[7:0]: win16_ywindow2[7:0] First horizontal window for 16-window function
0x5A2E	WIN16 YWIN3	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: win16_ywindow3[9:8] First horizontal window for 16-window function
0x5A2F	WIN16 YWIN3	0xB4	RW	Bit[7:0]: win16_ywindow3[7:0] First horizontal window for 16-window function

A.2.24 isp_dpc [0x5B00 - 0x5B12, 0x5B14 - 0x5B35]

table A-25 isp_dpc control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5B00	DPC CTRL00	0x1B	RW	Bit[7]: Tail enable Bit[6]: General tail enable Bit[5]: 3x3 cluster enable Bit[4]: Saturate cross cluster enable Bit[3]: Cross cluster enable Bit[2]: Manual mode enable Bit[1]: Black pixel correction enable Bit[0]: White pixel correction enable
0x5B01	DPC CTRL01	0x94	RW	Bit[7:6]: VNumList2 Bit[5:4]: VNumList1 Bit[3:2]: VNumList0 Bit[1]: Clip interpg enable Bit[0]: Share buffer enable
0x5B02	DPC CTRL02	0x2E	RW	Bit[7:6]: Reserved Bit[5:4]: Pixel order man Bit[3:2]: Edge option Bit[1:0]: VNumList3
0x5B03	DPC CTRL03	0x24	RW	Bit[7]: Reserved Bit[6:3]: WThresList0 Bit[2:0]: Max VNum

table A-25 isp_dpc control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5B04	DPC CTRL04	0x12	RW	Bit[7:4]: WThresList2 Bit[3:0]: WThresList1
0x5B05	DPC CTRL05	0x41	RW	Bit[7:4]: BThresRatio Bit[3:0]: WThresList3
0x5B06	DPC CTRL06	0x48	RW	Bit[7:4]: Status threshold Bit[3:0]: More connection case threshold
0x5B07	DPC CTRL07	0x84	RW	Bit[7:4]: Matching threshold Bit[3:0]: Status threshold step
0x5B08	DPC CTRL08	0x40	RW	Bit[7:4]: Adaptive pattern step Bit[3:0]: Adaptive pattern threshold
0x5B09	DPC CTRL09	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Saturate
0x5B0A	DPC CTRL0A	0x03	RW	Bit[7:0]: Gain list0
0x5B0B	DPC CTRL0B	0x0F	RW	Bit[7:0]: Gain list1
0x5B0C	DPC CTRL0C	0x3F	RW	Bit[7:3]: Gain list2 Bit[2:0]: Not used
0x5B0D	DPC CTRL0D	0x0F	RW	Bit[7:0]: DPC level list0
0x5B0E	DPC CTRL0E	0xFD	RW	Bit[7:0]: DPC level list1
0x5B0F	DPC CTRL0F	0xF5	RW	Bit[7:0]: DPC level list2
0x5B10	DPC CTRL10	0xF5	RW	Bit[7:0]: DPC level list3
0x5B11	DPC CTRL11	0x02	RW	Bit[7:2]: Reserved Bit[1]: Saturate option Bit[0]: Reserved
0x5B12	RSVD	–	–	Reserved
0x5B14	DPC CTRL14	0x00	RW	Bit[7]: Clock gate disable rec2 Bit[6]: Clock gate disable rec1 Bit[5]: Clock gate disable rec0 Bit[4]: Clock gate disable SRAM Bit[3]: Clock gate disable buffer Bit[2]: Clock gate disable SF Bit[1]: Clock gate disable Bit[0]: Manual pixel order enable
0x5B15~ 0x5B1D	RSVD	–	–	Reserved
0x5B1E	DPC STAT 1E	–	R	Bit[7]: Reserved Bit[6:0]: BThre
0x5B1F	DPC STAT 1F	–	R	Bit[7:5]: Reserved Bit[4:0]: WThre

table A-25 isp_dpc control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5B20	DPC STAT 20	–	R	Bit[7:5]: Reserved Bit[4:0]: Thre1
0x5B21	DPC STAT 21	–	R	Bit[7:0]: Thre2
0x5B22	DPC STAT 22	–	R	Bit[7]: Reserved Bit[6:0]: Thre3
0x5B23	DPC STAT 23	–	R	Bit[7]: Reserved Bit[6:0]: Thre4
0x5B24	DPC STAT 24	–	R	Bit[7:4]: Level Bit[3:0]: PConnected
0x5B25	DPC STAT 25	–	R	Bit[7:3]: Reserved Bit[2:0]: VNum
0x5B26	DPC STAT 26	–	R	Bit[7:0]: DPC_version[15:8]
0x5B27	DPC STAT 27	–	R	Bit[7:0]: DPC_version[7:0]
0x5B28~ 0x5B35	RSVD	–	–	Reserved

A.2.25 isp_otp_dpc [0x5C00 - 0x5C0D, 0x5C10 - 0x5C23]

table A-26 isp_otp_dpc control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5C00	OTP CTRL00	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Memory start address[9:8]
0x5C01	OTP CTRL01	0x00	RW	Bit[7:0]: Memory start address[7:0]
0x5C02	OTP CTRL02	0x01	RW	Bit[7:2]: Reserved Bit[1:0]: Memory end address[9:8]
0x5C03	OTP CTRL03	0x2F	RW	Bit[7:0]: Memory end address[7:0]

table A-26 isp_otp_dpc control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5C04	OTP CTRL04	0x42	RW	Bit[7]: Reserved Bit[6]: Mapping enable Bit[5]: Threshold function enable 0: Disable recover threshold in register 0x5B09 (can recover black cluster) 1: Enable recover threshold in register 0x5B09 (cannot recover black cluster) Bit[4]: Manual increase step enable Bit[3]: Disable mirror and flip Bit[2]: Disable OTP offset Bit[1]: Mirror option enable Bit[0]: Disable binning mode
0x5C05	OTP CTRL05	0x6C	RW	Bit[7]: Reserved Bit[6:5]: Recover method select 00: Left 1 neighbor pixel (on same channel) 01: Minimum of left 2 neighbor pixels 10: Average of left and right 1 neighbor pixel 11: Maximum between minimum of left 2 neighbor pixels and minimum of right 2 neighbor pixels Bit[4]: Use fixed pattern to recover cluster Bit[3]: Fixed pattern mode 0: Use 0x00 to recover cluster 1: Use 0x3FF to recover cluster Bit[2]: Flip option enable Bit[1]: Sensor exposure constrain enable Bit[0]: Sensor gain constrain enable
0x5C06	OTP CTRL06	0x00	RW	Bit[7]: Reserved Bit[6:5]: Constrain exposure threshold[9:8] Bit[4:0]: Reserved
0x5C07	OTP CTRL07	0x00	RW	Bit[7:0]: Constrain exposure threshold[7:0] Disable OTP function when sensor exposure is smaller than constrain exposure threshold
0x5C08	OTP CTRL08	0x07	RW	Bit[7:6]: Reserved Bit[5:0]: Constrain gain threshold Disable OTP function when sensor gain is smaller than constrain gain threshold

table A-26 isp_otp_dpc control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5C09	OTP CTRL09	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: Recover threshold Recover when high 8-bits of recovered data is bigger than original one by this threshold
0x5C0A	OTP CTRL0A	0x01	RW	Bit[7:5]: Reserved Bit[4:0]: Manual horizontal even increase step
0x5C0B	OTP CTRL0B	0x01	RW	Bit[7:5]: Reserved Bit[4:0]: Manual horizontal odd increase step
0x5C0C	OTP CTRL0C	0x01	RW	Bit[7:5]: Reserved Bit[4:0]: Manual vertical even increase step
0x5C0D	OTP CTRL0D	0x01	RW	Bit[7:5]: Reserved Bit[4:0]: Manual vertical odd increase step
0x5C10	OTP RO10	–	R	Bit[7:4]: Reserved Bit[3:0]: Horizontal offset[11:8]
0x5C11	OTP RO11	–	R	Bit[7:0]: Horizontal offset[7:0]
0x5C12	OTP RO12	–	R	Bit[7:4]: Reserved Bit[3:0]: Vertical offset[11:8]
0x5C13	OTP RO13	–	R	Bit[7:0]: Vertical offset[7:0]
0x5C14	OTP RO14	–	R	Bit[7:5]: Reserved Bit[4:0]: Horizontal even increase step
0x5C15	OTP RO15	–	R	Bit[7:5]: Reserved Bit[4:0]: Horizontal odd increase step
0x5C16	OTP RO16	–	R	Bit[7:5]: Reserved Bit[4:0]: Vertical even increase step
0x5C17	OTP RO17	–	R	Bit[7:5]: Reserved Bit[4:0]: Vertical odd increase step
0x5C18~ 0x5C1F	RSVD	–	–	Reserved
0x5C20	OTP CTRL20	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual X offset[11:8]
0x5C21	OTP CTRL21	0x00	RW	Bit[7:0]: Manual X offset[7:0]
0x5C22	OTP CTRL22	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual Y offset[11:8]
0x5C23	OTP CTRL23	0x00	RW	Bit[7:0]: Manual Y offset[7:0]

A.2.26 isp_gain_fmt [0x5D06 - 0x5D0B]

table A-27 isp_gain_fmt control registers

address	register name	default value	R/W	description
0x5D06	DIG GAIN MAN	0x02	RW	Bit[7:6]: Reserved Bit[5:0]: dig_gain_man[13:8] Manual digital gain
0x5D07	DIG GAIN MAN	0x00	RW	Bit[7:0]: dig_gain_man[7:0] Manual digital gain
0x5D08	MWB CTRL08	0x00	RW	Bit[7:3]: Reserved Bit[2]: blc_target_man_en Bit[1]: dig_gain_man_en Bit[0]: cfa_pattern_man_en
0x5D09	CFA PATTERN MAN	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: cfa_pattern_man
0x5D0A	BLC TARGET MAN	0x02	RW	Bit[7:4]: Reserved Bit[3:0]: blc_target_man[11:8]
0x5D0B	BLC TARGET MAN	0x00	RW	Bit[7:0]: blc_target_man[7:0]

A.2.27 isp_pre [0x5E00 - 0x5E2E]

table A-28 isp_pre control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5E00	PRE CTRL00	0x00	RW	Bit[7]: Test pattern enable Bit[6]: Rolling bar function enable Bit[5]: Transparent enable Bit[4]: Square mode 0: Gray scale squares 1: Black-white squares Bit[3:2]: Test pattern bar style 00: Standard test pattern bar 01: Top-bottom darker test pattern bar 10: Right-left darker test pattern bar 11: Bottom-top darker test pattern bar Bit[1:0]: Test pattern mode 00: Test pattern bar 01: Random data 10: Square 11: Black image

table A-28 isp_pre control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5E01	PRE CTRL01	0x41	RW	Bit[7]: Reserved Bit[6]: Window cut enable Bit[5]: two_lsb_0_en Set lowest two bits to 0 Bit[4]: Same seed enable Reset seed to 0x5E01[3:0] each frame Bit[3:0]: Random seed Seed used in generating random data
0x5E02	PRE CTRL02	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Line number interrupt[11:8]
0x5E03	PRE CTRL03	0x01	RW	Bit[7:0]: Line number interrupt[7:0]
0x5E04	PRE CTRL04	0x00	RW	Bit[7:0]: Scale X input manual size[15:8]
0x5E05	PRE CTRL05	0x00	RW	Bit[7:0]: Scale X input manual size[7:0]
0x5E06	PRE CTRL06	0x01	RW	Bit[7:0]: Scale Y input manual size[15:8]
0x5E07	PRE CTRL07	0x00	RW	Bit[7:0]: Scale Y input manual size[7:0]
0x5E08	PRE CTRL08	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Horizontal manual offset[11:8]
0x5E09	PRE CTRL09	0x00	RW	Bit[7:0]: Horizontal manual offset[7:0]
0x5E0A	PRE CTRL0A	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Vertical manual offset[11:8]
0x5E0B	PRE CTRL0B	0x00	RW	Bit[7:0]: Vertical manual offset[7:0]
0x5E0C	PRE RO0C	–	R	Bit[7:4]: Reserved Bit[3:0]: Input image pixel number[11:8]
0x5E0D	PRE RO0D	–	R	Bit[7:0]: Input image pixel number[7:0]
0x5E0E	PRE RO0E	–	R	Bit[7:4]: Reserved Bit[3:0]: Input image line number[11:8]
0x5E0F	PRE RO0F	–	R	Bit[7:0]: Input image line number[7:0]

table A-28 isp_pre control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x5E10	PRE CTRL10	0x3C	RW	Bit[7]: Window X offset option Bit[6]: Window Y offset option Bit[5]: Take first pixel in same position with no mirror image enable Bit[4]: Take first pixel in same position with no flip image enable Bit[3]: Mirror option from window 0: First pixel is P2 or P4 with window output 1: First pixel is P1 or P3 with window output Bit[2]: Flip option from window 0: First line is P3P4 with window output 1: First line is P1P2 with window output Bit[1]: Offset manual enable Bit[0]: Scale size manual enable
0x5E11	PRE CTRL11	0x00	RW	Bit[7]: Manual clock/valid ratio enable Bit[6:4]: Manual dummy line number Bit[3]: Reduce HREF low length by half Bit[2:0]: Manual clock/valid ratio for dummy line
0x5E12	PRE RO12	–	R	Bit[7:0]: HREF blank length for dummy line[15:8]
0x5E13	PRE RO13	–	R	Bit[7:0]: HREF blank length for dummy line[7:0]
0x5E14	PRE RO14	–	R	Bit[7:0]: HREF length for dummy line[15:8]
0x5E15	PRE RO15	–	R	Bit[7:0]: HREF length for dummy line[7:0]
0x5E16	PRE RO16	–	R	Bit[7:5]: Reserved Bit[4]: Dummy error indicating signal Bit[3]: Reserved Bit[2:0]: Dummy line clock ratio output
0x5E17	PRE RO17	–	R	Bit[7:4]: Horizontal odd increase step Bit[3:0]: Vertical odd increase step
0x5E18	PRE RO18	–	R	Bit[7:4]: Reserved Bit[3:0]: Horizontal sensor offset[11:8]
0x5E19	PRE RO19	–	R	Bit[7:0]: Horizontal sensor offset[7:0]
0x5E1A	PRE RO1A	–	R	Bit[7:4]: Reserved Bit[3:0]: Vertical sensor offset[11:8]
0x5E1B	PRE RO1B	–	R	Bit[7:0]: Vertical sensor offset[7:0]

table A-28 isp_pre control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x5E1C	PRE RO1C	–	R	Bit[7:4]: Reserved Bit[3:0]: Horizontal window offset[11:8]
0x5E1D	PRE RO1D	–	R	Bit[7:0]: Horizontal window offset[7:0]
0x5E1E	PRE RO1E	–	R	Bit[7:4]: Reserved Bit[3:0]: Vertical window offset[11:8]
0x5E1F	PRE RO1F	–	R	Bit[7:0]: Vertical window offset[7:0]
0x5E20	PRE RO20	–	R	Bit[7:5]: Reserved Bit[4:0]: Horizontal window output size[12:8]
0x5E21	PRE RO21	–	R	Bit[7:0]: Horizontal window output size[7:0]
0x5E22	PRE RO22	–	R	Bit[7:4]: Reserved Bit[3:0]: Vertical window output size[11:8]
0x5E23	PRE RO23	–	R	Bit[7:0]: Vertical window output size[7:0]
0x5E24	PRE RO24	–	R	Bit[7:6]: Reserved Bit[5:4]: Horizontal skip Bit[3:2]: Reserved Bit[1:0]: Vertical skip
0x5E25	PRE RO25	–	R	Bit[7:4]: Horizontal even increase step Bit[3:0]: Vertical even increase step
0x5E26	RSVD	–	–	Reserved
0x5E27	PRE RO27	–	R	Bit[7:4]: Reserved Bit[3:0]: Cut top offset for bi-linear BLC[11:8]
0x5E28	PRE RO28	–	R	Bit[7:0]: Cut top offset for bi-linear BLC[7:0]
0x5E29	PRE RO29	–	R	Bit[7:4]: Reserved Bit[3:0]: Cut bottom offset for bi-linear BLC[11:8]
0x5E2A	PRE RO2A	–	R	Bit[7:0]: Cut bottom offset for bi-linear BLC[7:0]
0x5E2B	PRE CTRL2B	0x09	RW	Bit[7:4]: Reserved Bit[3:0]: Array height for bi-linear BLC[11:8]
0x5E2C	PRE CTRL2C	0xB0	RW	Bit[7:0]: Array height for bi-linear BLC[7:0]
0x5E2D	PRE CTRL2D	0x00	RW	Bit[7:6]: Reserved Bit[5]: Manual horizontal skip enable Bit[4:0]: Reserved
0x5E2E	PRE CTRL2E	0x00	RW	Bit[7:6]: Reserved Bit[5]: Manual vertical skip enable Bit[4:0]: Reserved

A.2.28 isp_dgc_comp [0x5F00 - 0x5F05]

table A-29 isp_dgc_comp control registers

address	register name	default value	R/W	description
0x5F00	DIG_COMP_CTRL00	0x00	RW	Bit[7:5]: Reserved Bit[4]: dither_en Bit[3]: dig_comp_blc_off Bit[2]: dig_comp_bypass Bit[1]: man_opt Bit[0]: man_en
0x5F01	RSVD	–	–	Reserved
0x5F02	DIG_COMP_CTRL02	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: dig_comp_man[9:8]
0x5F03	DIG_COMP_CTRL03	0x00	RW	Bit[7:0]: dig_comp_man[7:0]
0x5F04	DIG_COMP_CTRL04	–	R	Bit[7:2]: Reserved Bit[1:0]: dig_comp_i[9:8]
0x5F05	DIG_COMP_CTRL05	–	R	Bit[7:0]: dig_comp_i[7:0]

revision history

version 1.0 11.14.2018

- initial release

version 2.0 02.12.2019

- changed datasheet from Preliminary Specification to Product Specification
- in ordering information, removed "-Z" from ordering part number
- in section 1.2, updated figure 1-1
- in table 1-1, changed signal name and description of pin A7 to TMO and test mode output, respectively
- in table 1-2, changed signal name for pin A7 to TMO
- in table 1-3, changed symbol in second row to SDA, TMO
- in section 1.3, updated figures 1-2 and 1-3
- in chapter 2, updated figure 2-1
- in section 3.8, updated figure 3-9 and updated strobe control example setting code
- in section 5.3, added fourth and fifth sentences to second paragraph, added two lines of code to beginning and one line of code to end of Example 1 – embedded line with RAW10 output, and added two lines of code to beginning and one line of code to end of Example 2 – embedded line with RAW8 output

version 2.01 08.29.2019

- in figure 1-2, added TMCLK with ground, added TMCLK to note 2, and removed TMCLK from note 3
- in figure 1-3, added TMCLK with ground, added TMCLK to note 2, and removed TMCLK from note 3

version 2.02 10.30.2019

- in figure 9-1, added L1 and L2 symbols

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