SONY

Diagonal 6.3 mm (Type 1 / 2.9) CMOS solid-state Image Sensor with Square Pixel for Color Cameras

IMX296LQR-C

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Pregius

Description

The IMX296LQR-C is a diagonal 6.3 mm (Type 1 / 2.9) CMOS active pixel type solid-state image sensor with a square pixel array and 1.58 M effective pixels. This chip features a global shutter with variable charge-integration time. This chip operates with analog 3.3 V, digital 1.2 V, and interface 1.8 V triple power supply, and has low power consumption. High sensitivity, low dark current and low PLS characteristics are achieved.
(Applications: Sensing)

Features

- CMOS active pixel type dots
- Built-in timing adjustment circuit, H/V driver and serial communication circuit
- Global shutter function
- Input frequency
  37.125 MHz / 74.25 MHz / 54 MHz
- Number of recommended recording pixels: 1440 (H) × 1080 (V) approx. 1.55 M pixels

  Readout mode
  All-pixel scan mode
  ROI mode
  Vertical / Horizontal - Normal / Inverted readout mode
- Readout rate
  Maximum frame rate in

  All-pixel scan mode: 10 bit: 60.3 frame/s
- Variable-speed shutter function (resolution 1 H units)
- 10-bit A/D converter
- CDS / PGA function
  0 dB to 24 dB: Analog Gain (0.1 dB step)
  24.1 dB to 48 dB: Analog Gain: 24 dB + Digital Gain: 0.1 dB to 24 dB (0.1 dB step)
- I/O interface
  CSI-2 serial data output (1 Lane) RAW10 output
- Recommended lens F number: 2.8 or more (Close side)
- Recommended exit pupil distance: –100 mm to -∞

Device Structure

- ◆ CMOS image sensor
- ◆ Image size
  Diagonal 6.3 mm (Type 1 / 2.9) Approx. 1.58 M pixels All-pixel
- ◆ Total number of pixels
  1456 (H) × 1098 (V) Approx. 1.60 M pixels
- ◆ Number of effective pixels
  1456 (H) × 1088 (V) Approx. 1.58 M pixels
- ◆ Number of active pixels
  1456 (H) × 1088 (V) Approx. 1.58 M pixels
- ◆ Number of recommended recording pixels
  1440 (H) × 1080 (V) Approx. 1.56 M pixels All-pixel
- ◆ Unit cell size
  3.45 µm (H) × 3.45 µm (V)
- ◆ Optical black
  Horizontal (H) direction: Front 0 pixels, rear 0 pixels
  Vertical (V) direction: Front 10 pixels, rear 0 pixels
- ◆ Substrate material
  Silicon

Absolute Maximum Ratings

Item	Symbol	Rating			Unit	Remarks
Supply voltage (Analog 3.3 V)	AV_{DD}	–0.3	to	+4.0	V	
Supply voltage (Interface 1.8 V)	OV_{DD}	–0.3	to	+3.3	V	
Supply voltage (Digital 1.2 V)	DV_{DD}	–0.3	to	+2.0	V	
Input voltage	VI	–0.3	to	OV_{DD} +0.3	V	Not exceed 3.3 V
Output voltage	VO	–0.3	to	OV_{DD} +0.3	V	Not exceed 3.3 V
Operating temperature	Topr	-30	to	+75	˚C	
Storage temperature	Tstg	-40	to	+85	˚C	
Performance guarantee temperature	Tspec	-10	to	+60	˚C	

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (Analog 3.3 V)	AV_{DD}	3.15	3.30	3.45	V
Supply voltage (Interface 1.8 V)	OV_{DD}	1.70	1.80	1.90	V
Supply voltage (Digital 1.2 V)	DV_{DD}	1.10	1.20	1.30	V

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General-0.0.9

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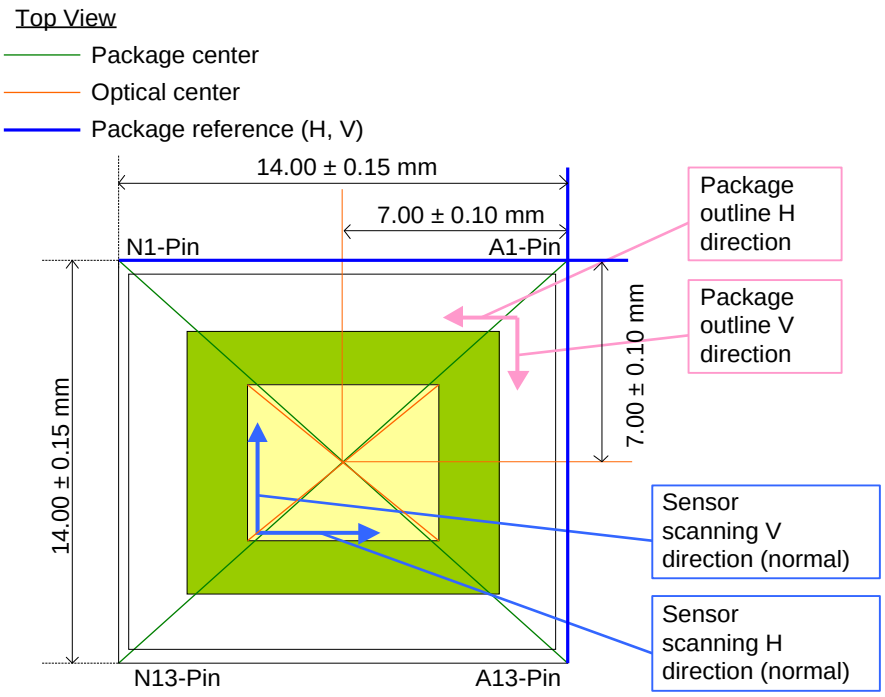
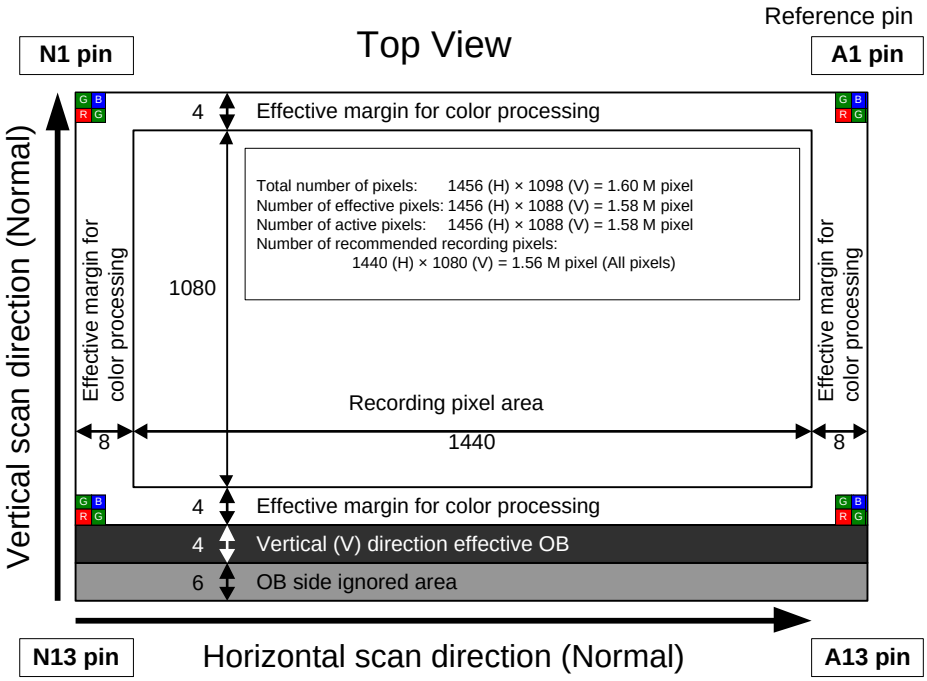
Chip Center and Optical Center



Optical Center

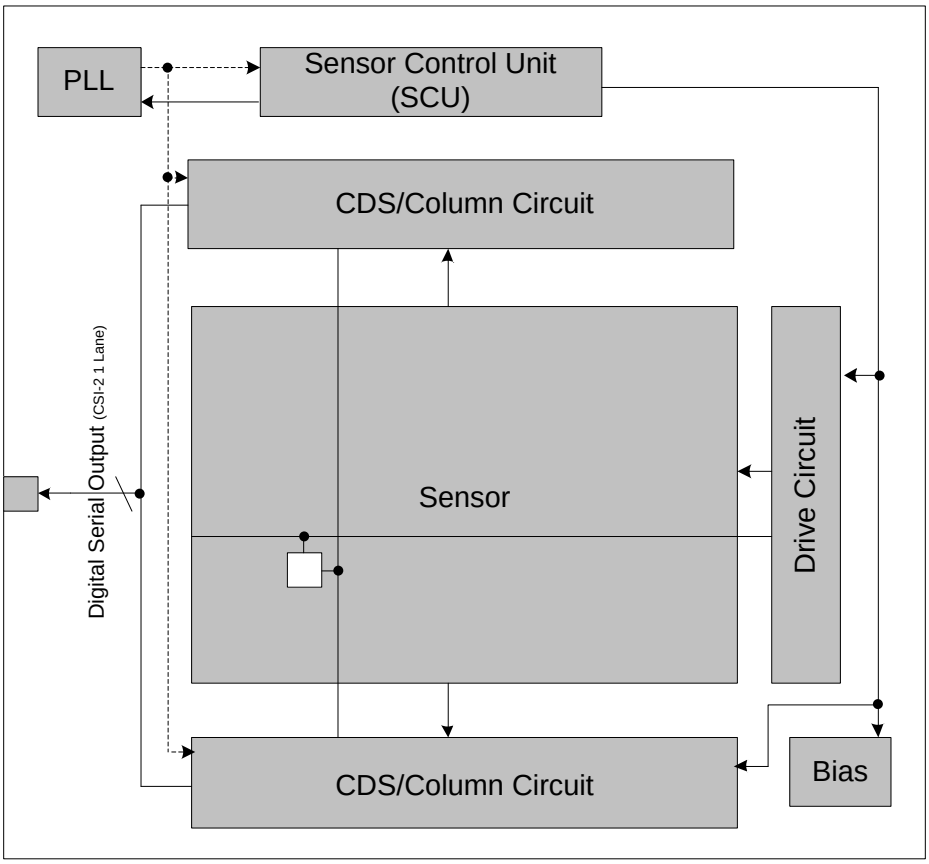
Pixel Arrangement



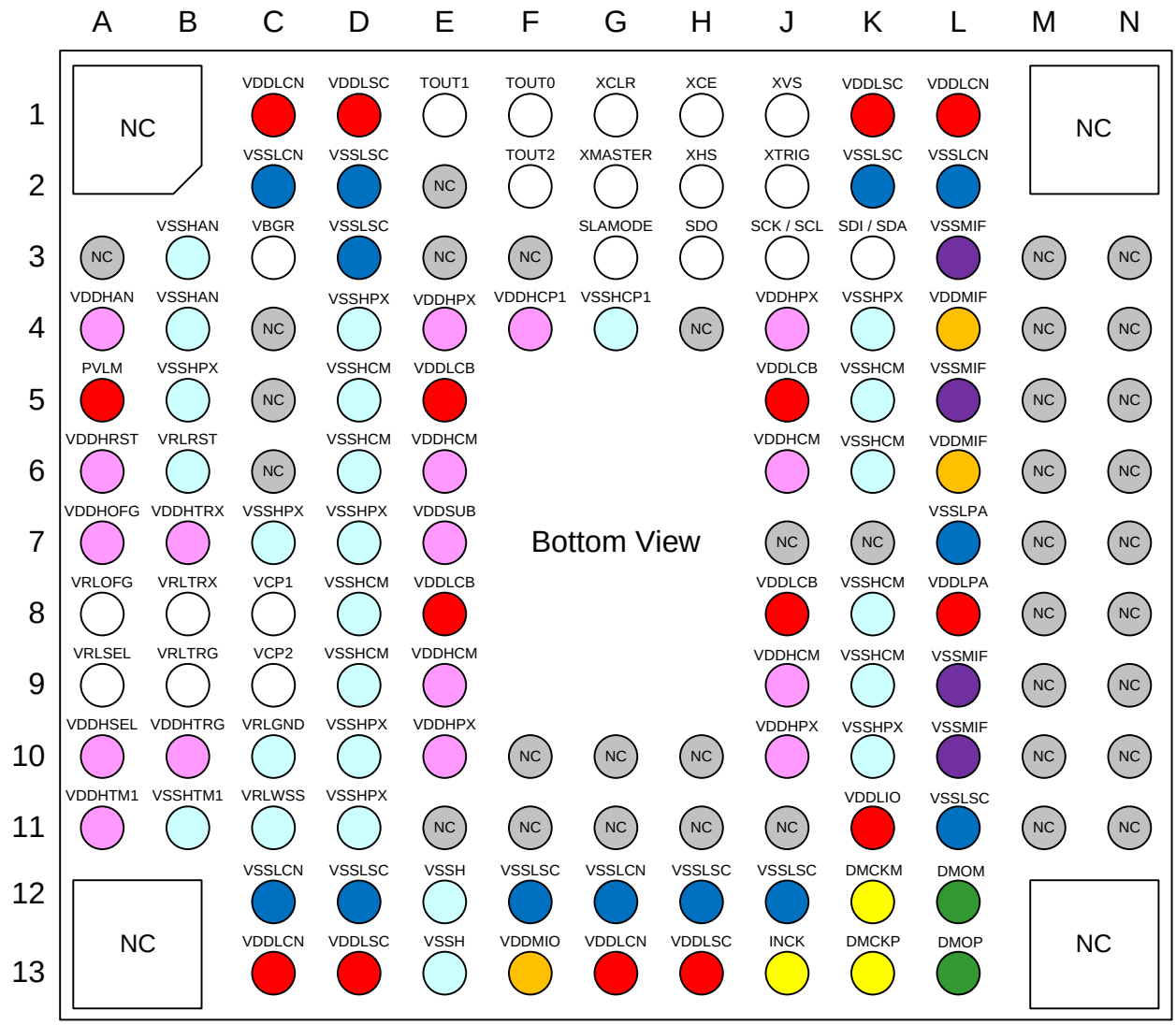
Pixel Arrangement

Block Diagram and Pin Configuration

(Top View)



Block Diagram



Pin Configuration

Pin Description

No.	Pin No.	I/O	Analog / Digital	Symbol	Description
1	A1	—	—	N.C.	—
2	A3	—	—	N.C.	—
3	A4	Power	A	VDDHAN	3.3 V power supply
4	A5	Power	A	PVLM	1.2 V power supply
5	A6	Power	A	VDDHRST	3.3 V power supply
6	A7	Power	A	VDDHOFG	3.3 V power supply
7	A8	I	A	VRLOFG	Connect to VCP1
8	A9	I	A	VRLSEL	Connect to VCP1
9	A10	Power	A	VDDHSEL	3.3 V power supply
10	A11	Power	A	VDDHTM1	3.3 V power supply
11	A13	—	—	N.C.	—
12	B3	GND	A	VSSHAN	3.3 V GND
13	B4	GND	A	VSSHAN	3.3 V GND
14	B5	GND	A	VSSHPX	3.3 V GND
15	B6	GND	A	VRLRST	3.3 V GND
16	B7	Power	A	VDDHTRX	3.3 V power supply
17	B8	I	A	VRLTRX	Connect to VCP1
18	B9	I	A	VRLTRG	Connect to VCP2
19	B10	Power	A	VDDHTRG	3.3 V power supply
20	B11	GND	A	VSSHTM1	3.3 V GND
21	C1	Power	D	VDDLCN	1.2 V power supply
22	C2	GND	D	VSSLCN	1.2 V GND
23	C3	O	A	VBGR	Connect to 0.22 µF to GND
24	C4	—	—	N.C.	—
25	C5	—	—	N.C.	—
26	C6	—	—	N.C.	—
27	C7	GND	A	VSSHPX	3.3 V GND
28	C8	O	A	VCP1	Connect to VRLSEL, VRLTRX, VRLOFG (Connect to 4.7 µF × 2 to GND)
29	C9	O	A	VCP2	Connect to VRLTRG (Connect to 4.7 µF × 2 to GND)
30	C10	GND	A	VRLGND	3.3 V GND
31	C11	GND	A	VRLWSS	3.3 V GND
32	C12	GND	D	VSSLCN	1.2 V GND
33	C13	Power	D	VDDLCN	1.2 V power supply
34	D1	Power	D	VDDLSC	1.2 V power supply
35	D2	GND	D	VSSLSC	1.2 V GND
36	D3	GND	D	VSSLSC	1.2 V GND
37	D4	GND	A	VSSHPX	3.3 V GND
38	D5	GND	A	VSSHCM	3.3 V GND
39	D6	GND	A	VSSHCM	3.3 V GND
40	D7	GND	A	VSSHPX	3.3 V GND
41	D8	GND	A	VSSHCM	3.3 V GND
42	D9	GND	A	VSSHCM	3.3 V GND
43	D10	GND	A	VSSHPX	3.3 V GND
44	D11	GND	A	VSSHPX	3.3 V GND
45	D12	GND	D	VSSLSC	1.2 V GND
46	D13	Power	D	VDDLSC	1.2 V power supply
47	E1	O	D	TOUT1	Pulse1 output pin
48	E2	—	—	N.C.	—
49	E3	—	—	N.C.	—
50	E4	Power	A	VDDHPX	3.3 V power supply
51	E5	Power	A	VDDLCB	1.2 V power supply
52	E6	Power	A	VDDHCM	3.3 V power supply
53	E7	Power	A	VDDSUB	3.3 V power supply
54	E8	Power	A	VDDLCB	1.2 V power supply
55	E9	Power	A	VDDHCM	3.3 V power supply
56	E10	Power	A	VDDHPX	3.3 V power supply
57	E11	—	—	N.C.	—
58	E12	GND	A	VSSH	3.3 V GND
59	E13	GND	A	VSSH	3.3 V GND
60	F1	O	D	TOUT0	Pulse0 output pin
61	F2	O	D	TOUT2	Pulse2 output pin
62	F3	—	—	N.C.	—

No.	Pin No.	I/O	Analog / Digital	Symbol	Description
63	F4	Power	A	VDDHCP1	3.3 V power supply
64	F10	—	—	N.C.	—
65	F11	—	—	N.C.	—
66	F12	GND	D	VSSLSC	1.2 V GND
67	F13	Power	D	VDDMIO	1.8 V power supply
68	G1	I	D	XCLR	System clear (Normal : High, Clear : Low)
69	G2	I	D	XMASTER	Master / Slave select (Slave Mode : High, Master Mode : Low)
70	G3	I	D	SLAMODE	Slave address select (37 : High, 36 : Low, 1A : both polarities)
71	G4	GND	A	VSSHCP1	3.3 V GND
72	G10	—	—	N.C.	—
73	G11	—	—	N.C.	—
74	G12	GND	D	VSSLCN	1.2 V GND
75	G13	Power	D	VDDLCN	1.2 V power supply
76	H1	I	D	XCE	4-wire : Serial communication I/F XCE pin I^2C : Fixed to High
77	H2	I/O	D	XHS	Horizontal sync signal
78	H3	O	D	SDO	4-wire : Serial communication I/F SDO pin I^2C : OPEN
79	H4	—	—	N.C.	—
80	H10	—	—	N.C.	—
81	H11	—	—	N.C.	—
82	H12	GND	D	VSSLSC	1.2 V GND
83	H13	Power	D	VDDLSC	1.2 V power supply
84	J1	I/O	D	XVS	Vertical sync signal
85	J2	I	D	XTRIG	Trigger input
86	J3	I	D	SCK / SCL	4-wire : Serial communication I/F SCK pin I^2C : Serial clock line
87	J4	Power	A	VDDHPX	3.3 V power supply
88	J5	Power	A	VDDLCB	1.2 V power supply
89	J6	Power	A	VDDHCM	3.3 V power supply
90	J7	—	—	N.C.	—
91	J8	Power	A	VDDLCB	1.2 V power supply
92	J9	Power	A	VDDHCM	3.3 V power supply
93	J10	Power	A	VDDHPX	3.3 V power supply
94	J11	—	—	N.C.	—
95	J12	GND	D	VSSLSC	1.2 V GND
96	J13	I	D	INCK	Maser clock input
97	K1	Power	D	VDDLSC	1.2 V power supply
98	K2	GND	D	VSSLSC	1.2 V GND
99	K3	I/O	D	SDI / SDA	4-wire : Serial communication I/F SDI pin I^2C : Serial data line
100	K4	GND	A	VSSHPX	3.3 V GND
101	K5	GND	A	VSSHCM	3.3 V GND
102	K6	GND	A	VSSHCM	3.3 V GND
103	K7	—	—	N.C.	—
104	K8	GND	A	VSSHCM	3.3 V GND
105	K9	GND	A	VSSHCM	3.3 V GND
106	K10	GND	A	VSSHPX	3.3 V GND
107	K11	Power	D	VDDLIO	1.2 V power supply
108	K12	O	D	DMCKM	CSI-2 output (Clock)
109	K13	O	D	DMCKP	CSI-2 output (Clock)
110	L1	Power	D	VDDLCN	1.2 V power supply
111	L2	GND	D	VSSLCN	1.2 V GND
112	L3	GND	D	VSSMIF	1.8 V GND
113	L4	Power	D	VDDMIF	1.8 V power supply
114	L5	GND	D	VSSMIF	1.8 V GND
115	L6	Power	D	VDDMIF	1.8 V power supply
116	L7	GND	D	VSSLPA	1.2 V GND
117	L8	Power	D	VDDLPA	1.2 V power supply
118	L9	GND	D	VSSMIF	1.8 V GND
119	L10	GND	D	VSSMIF	1.8 V GND
120	L11	GND	D	VSSLSC	1.2 V GND
121	L12	O	D	DMOM	CSI-2 output (Data)
122	L13	O	D	DMOP	CSI-2 output (Data)

No.	Pin No.	I/O	Analog / Digital	Symbol	Description
123	M3	—	—	N.C.	—
124	M4	—	—	N.C.	—
125	M5	—	—	N.C.	—
126	M6	—	—	N.C.	—
127	M7	—	—	N.C.	—
128	M8	—	—	N.C.	—
129	M9	—	—	N.C.	—
130	M10	—	—	N.C.	—
131	M11	—	—	N.C.	—
132	N1	—	—	N.C.	—
133	N3	—	—	N.C.	—
134	N4	—	—	N.C.	—
135	N5	—	—	N.C.	—
136	N6	—	—	N.C.	—
137	N7	—	—	N.C.	—
138	N8	—	—	N.C.	—
139	N9	—	—	N.C.	—
140	N10	—	—	N.C.	—
141	N11	—	—	N.C.	—
142	N13	—	—	N.C.	—

* N.C. pins in the table above should be left open on the board.

Electrical Characteristics

DC Characteristics

Item		Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Analog	V_{DD}Hx	AV_{DD}	—	3.15	3.30	3.45	V
	Interface	V_{DD}Mx	OV_{DD}	—	1.70	1.80	1.90	V
	Digital	V_{DD}Lx	DV_{DD}	—	1.10	1.20	1.30	V
Digital input voltage		XHS XVS XCLR INCK XMASTER SLAMODE SCK SDI XCE XTRIG	VIH	XVS / XHS in Slave mode	0.8 × OV_{DD}	—	—	V
			VIL		—	—	0.2 × OV_{DD}	V
Digital output voltage		XHS XVS SDO TOUT1 TOUT2	VOH	XVS / XHS in Master mode	OV_{DD} -0.4	—	—	V
			VOL		—	—	0.4	V

Power Consumption

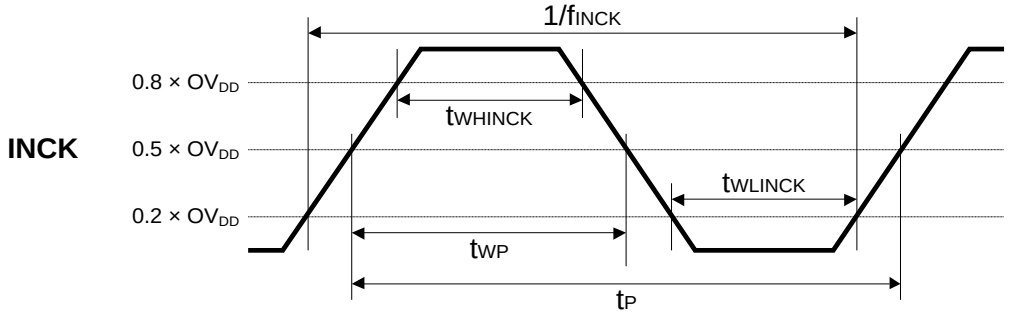
Item	Pins	Symbol	Typ.	Max.	Unit
Operating current MIPI CSI-2 1 lane 10 bit 60.3 frame/s	V_{DD}H	IAV_{DD}	140	200	mA
	V_{DD}M	IOV_{DD}	0.1	10	mA
	V_{DD}L	IDV_{DD}	71	130	mA
Standby current	V_{DD}H	IAV_{DD}_STB	—	0.6	mA
	V_{DD}M	IOV_{DD}_STB	—	0.5	mA
	V_{DD}L	IDV_{DD}_STB	—	20	mA

Operating current:
(Typical value condition) : Supply voltage: 3.30 V / 1.80 V / 1.20 V, Tj = 25 ˚C
(Maximum value condition) : Supply voltage: 3.45 V / 1.90 V / 1.30 V, Tj = 60 ˚C
Worst state of internal circuit operating current consumption.

Standby current:
(Maximum value condition) : Supply voltage: 3.45 V / 1.90 V / 1.30 V, Tj = 60 ˚C, INCK = 0 V,
The device in the light-obstructed state.

AC Characteristics

Master Clock (INCK) Waveform Diagram

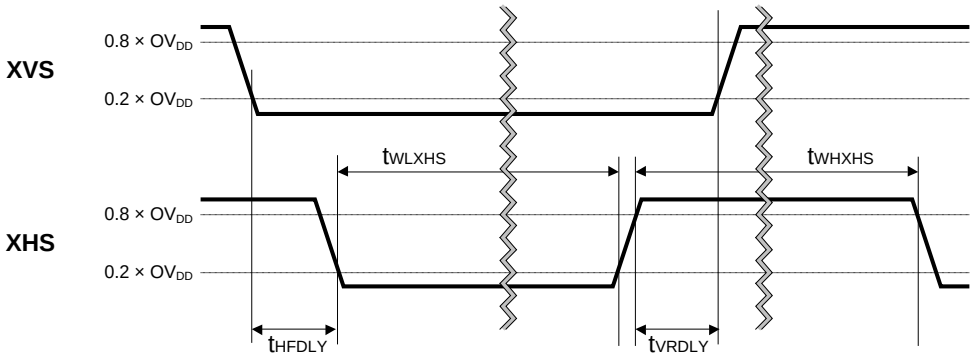


Duty Ratio = t_{WP} / t_P × 100

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	f_{INCK} × 0.96	f_{INCK}	f_{INCK} × 1.02	MHz	f_{INCK} = 37.125 MHz, 74.25 MHz, 54 MHz
INCK Low level pulse width	t_{WLINCK}	4	—	—	ns	
INCK High level pulse width	t_{WHINCK}	4	—	—	ns	
INCK clock duty	—	45.0	50.0	55.0	%	Define with 0.5 × OV_{DD}

* The INCK fluctuation affects the frame rate.

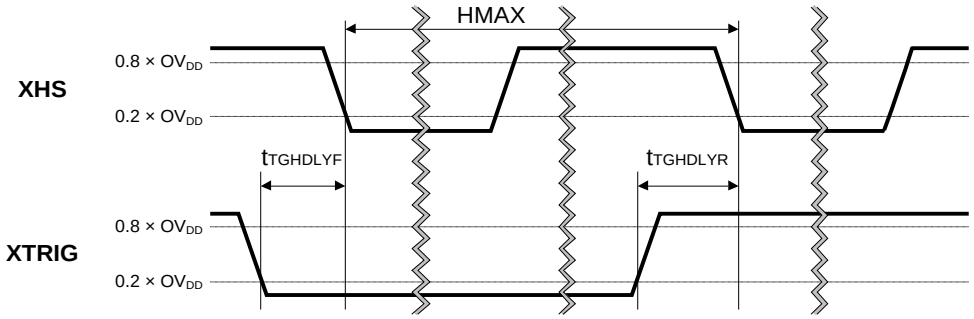
XVS / XHS Input Characteristics in Slave Mode (XMASTER = High)



Item	Symbol	Min.	Typ.	Max.	Unit
XHS Low level pulse width	t_{WLXHS}	$4/f_{INCK}$	—	—	ns
XHS High level pulse width	t_{WHXHS}	$4/f_{INCK}$	—	—	ns
XVS - XHS fall width	t_{HFDLY}	$1/f_{INCK}$	—	—	ns
XHS - XVS rise width	t_{VRDLY}	$1/f_{INCK}$	—	—	ns

Synchronization cannot be performed from XVS and XHS signal in mater mode. Detect the sync code.

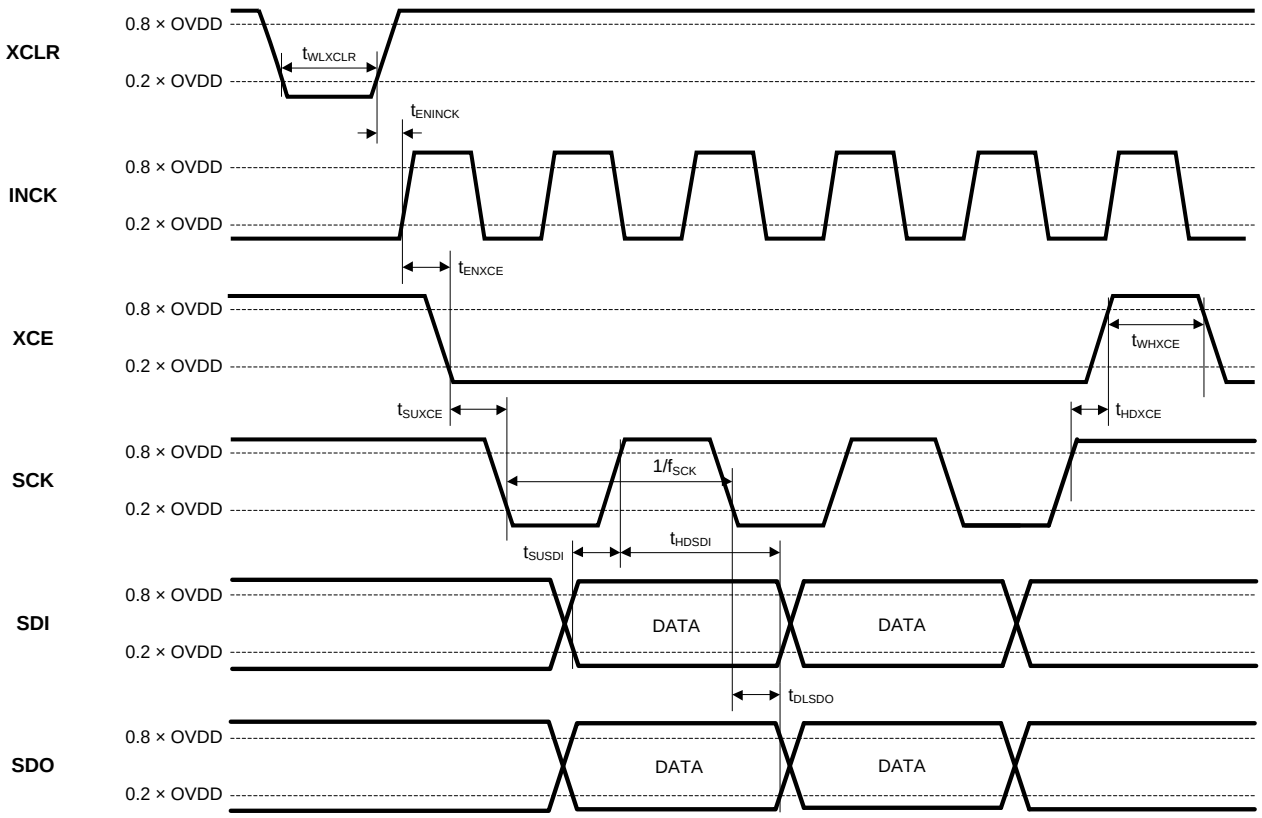
XTRIG Input Characteristics in Slave Mode (XMASTER = High) only



Item	Symbol	Min.	Typ.	Max.	Unit
XTRIG fall - XHS fall width	$t_{TGHDLYF}$	10	—	HMAX-10	INCK
XTRIG rise - XHS fall width	$t_{TGHDLYR}$	10	—	HMAX-10	INCK

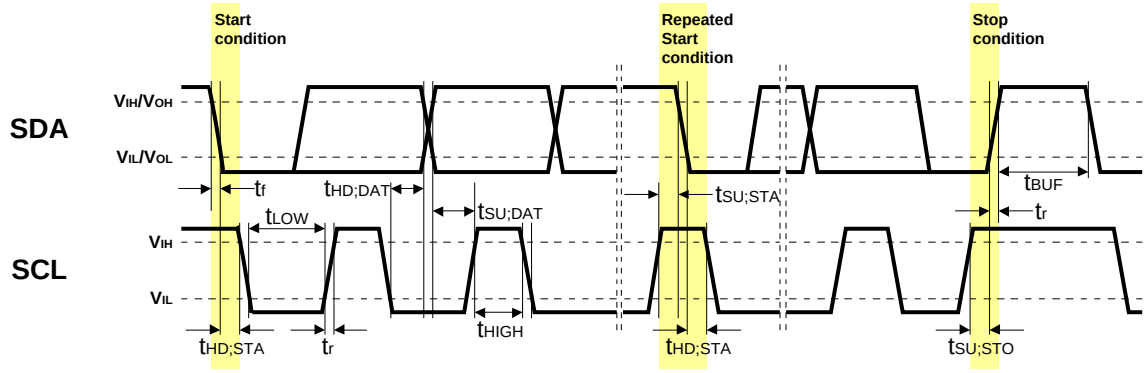
Serial Communication

4-wire



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCK clock frequency	f_{SCK}	—	—	13.5	MHz	
XCLR Low level pulse width	t_{WLXCLR}	$4/f_{INCK}$	—	—	ns	
INCK effective margin	t_{ENINCK}	1	—	—	µs	
XCE effective margin	t_{ENXCE}	20	—	—	µs	
XCE input setup time	t_{SUXCE}	20	—	—	ns	
XCE input hold time	t_{HDXCE}	20	—	—	ns	
XCE High level pulse width	t_{WHXCE}	20	—	—	ns	
SDI input setup time	t_{SUSDI}	10	—	—	ns	
SDI input hold time	t_{HDSDI}	10	—	—	ns	
SDO output delay time	t_{DLSDO}	0	—	25	ns	Output load capacitance: 20 pF

I²C



I²C Specification

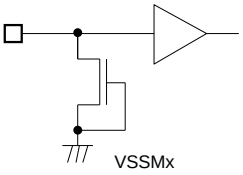
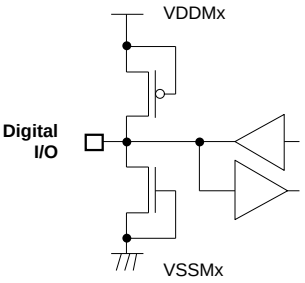
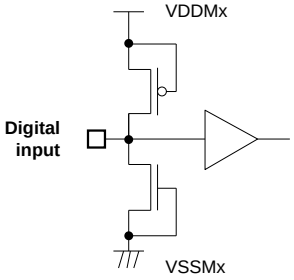
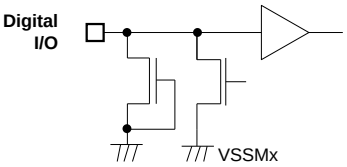
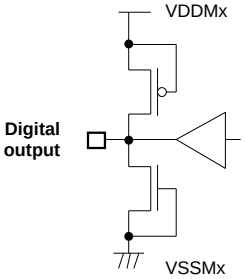
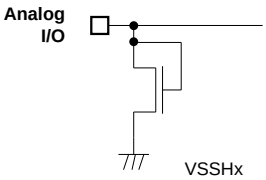
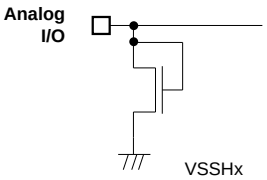
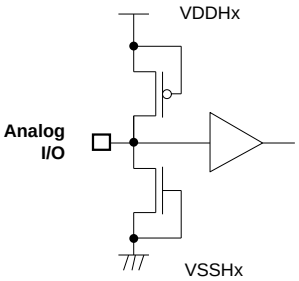
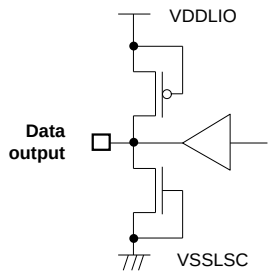
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Low level input voltage	V_{IL}	-0.3	—	0.3 × OV_{DD}	V	
High level input voltage	V_{IH}	0.7 × OV_{DD}	—	1.9	V	
Low level output voltage	V_{OL}	0	—	0.2 × OV_{DD}	V	OV_{DD} < 2 V, Sink 3 mA
High level output voltage	V_{OH}	0.8 × OV_{DD}	—	—	V	
Output fall time	tof	—	—	250	ns	Load 10 pF – 400 pF, 0.7 × OV_{DD} – 0.3 × OV_{DD}
Input current	Ii	-10	—	10	µA	0.1 × OV_{DD} – 0.9 × OV_{DD}
Capacitance for SCK (/SCL) , SDI (/SDA)	Ci	—	—	10	pF	

I²C AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	400	kHz
Hold time (Start Condition)	t_{HDSTA}	0.6	—	—	µs
Low period of the SCL clock	t_{LOW}	1.3	—	—	µs
High period of the SCL clock	t_{HIGH}	0.6	—	—	µs
Set-up time (Repeated Start Condition)	t_{SUSTA}	0.6	—	—	µs
Data hold time	t_{HDDAT}	0	—	0.9	µs
Data set-up time	t_{SUDAT}	100	—	—	ns
Rise time of both SDA and SCL signals	t_R	—	—	300	ns
Fall time of both SDA and SCL signals	t_F	—	—	300	ns
Set-up time (Stop Condition)	t_{SUSTO}	0.6	—	—	µs
Bus free time between a Stop and Start Condition	t_{BUF}	1.3	—	—	µs

I/O Equivalent Circuit Diagram

□ : External pin

Symbol	Equivalent circuit	Symbol	Equivalent circuit
INCK		XVS XHS	
XCLR XCE XMASTER XTRIG SLAMODE		SDI / SDA SCK / SCL	
SDO			
VCP1 VCP2		VRLOFG VRLTRX VRLSEL VRLTRG	
VBGR		DMCKP DMCKM DMOP DMOM	

Spectral Sensitivity Characteristics

(Excludes lens characteristics and light source characteristics.)

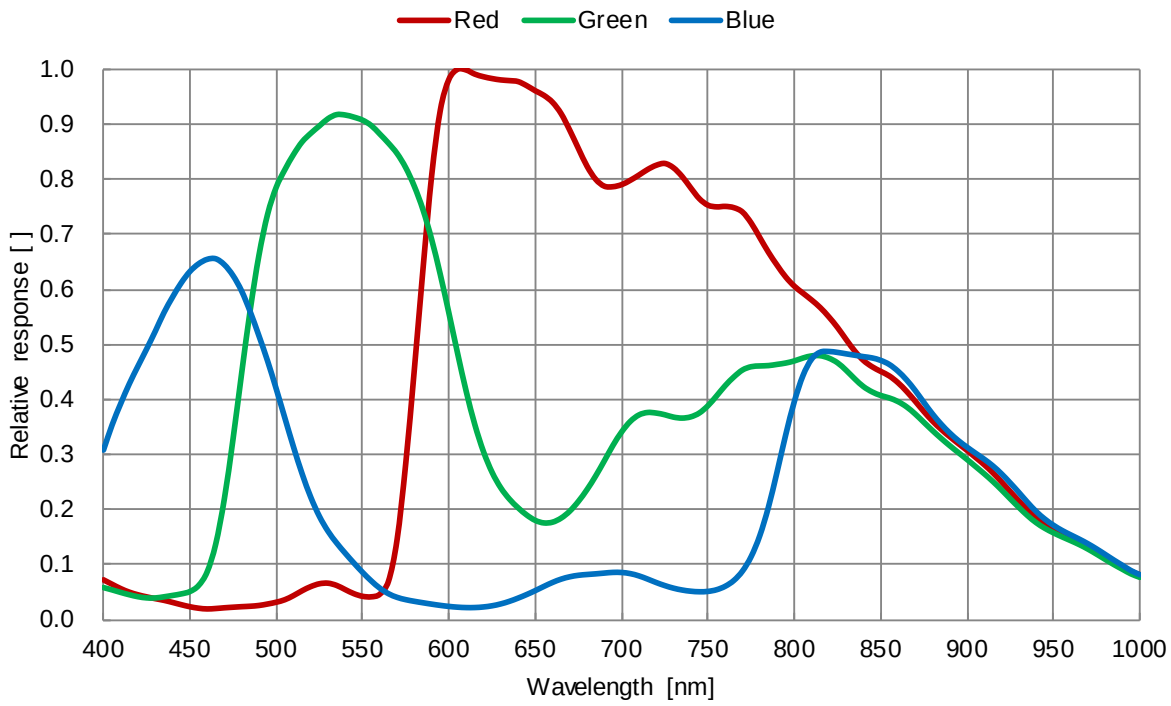


Image Sensor Characteristics

(AV_{DD} = 3.3 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, All-pixel scan mode, AD: 10 bit, Tj = 60 ˚C, Gain = 0 dB)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity		S	991 (970)	1171 (1146)	—	Digit (mV)	1	1/30 s storage
Sensitivity ratio	R / G	RG	0.47	—	0.62	—	2	
	B / G	BG	0.29	—	0.44	—		
Saturation signal		Vsat2D	1023 (1001)	—	—	Digit (mV)	3	Zone 0 to II'
Video signal shading		SH01	—	—	20	%	4	Zone 0, I
		SH2D	—	—	25	%		Zone 0 to II'
Dark signal		Vdt	—	—	0.19 (0.19)	Digit (mV)	5	1/30 s storage
Dark signal shading		ΔVdt	—	—	0.26 (0.25)	Digit (mV)	6	1/30 s storage
PLS (Parasitic Light Sensitivity)		Sm	—	—	-93.9	dB	7	Zone II'

Note) 1. Converted value into mV using 1Digit = 0.9779 mV.
2. The video signal shading is the measured value in the wafer status and does not include characteristics of the seal glass.

Zone Definition of Video Signal Shading

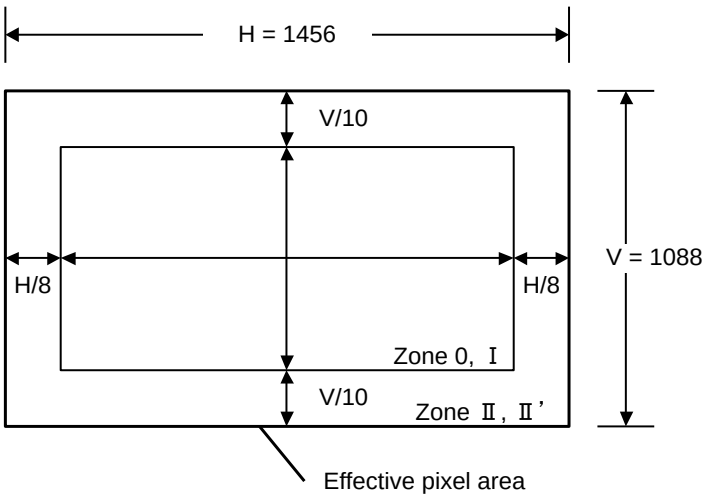


Image Sensor Characteristics Measurement Method

Measurement Conditions

In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the signal output of the measurement system.

Color Coding of Physical Pixel Array

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb represent the G signal on the same line as the R and B signals, respectively. The Gb signal and B signal lines and the R signal and Gr signal lines are output successively.

Gb	B	Gb	B
R	Gr	R	Gr
Gb	B	Gb	B
R	Gr	R	Gr

Color Coding Diagram

Definition of standard imaging conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706 cd/m^2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard image condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard image condition III:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens (exit pupil distance -100 mm) with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

Measurement Method

1. Sensitivity
   Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100 s, measure the Gr and Gb signal outputs (VGr, VGb) at the center of the screen, and substitute the values into the following formula.

   $$S = (VGr + VGb) / 2 \times 100 / 30 \text{ [mV]}$$

2. Sensitivity ratio
   Set the measurement condition to the standard imaging condition II. After adjusting the average value of the Gr and Gb signal outputs to 580 mV, measure the R signal output (VR [mV]), the Gr and Gb signal outputs (VGr, VGb [mV]) and the B signal output (VB [mV]) at the center of the screen in frame readout mode, and substitute the values into the following formulas.

   $$VG = (VGr + VGb) / 2$$
   $$RG = VR / VG$$
   $$BG = VB / VG$$

3. Saturation signal
   Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr and Gb signal outputs, 580 mV, measure the minimum values of the Gr, Gb, R and B signal outputs.

4. Video signal shading
   Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs are 580 mV. Then measure the maximum value (Gmax [mV]) and the minimum value (Gmin [mV]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

   $$SH = (Gmax - Gmin) / 580 \times 100 \text{ [\%]}$$

5. Dark signal
   With the device junction temperature of 60 ˚C and the device in the light-obstructed state, divide the output difference between 1/3 s integration at 3 frame/s and 1/30 s integration at 30 frame/s by 9, and calculate the signal output converted to 1/30 s integration. Measure the average value of this output (Vdt [mV]).

6. Dark signal shading
   Measure the maximum value (Vdmax [mV]) and the minimum value (Vdmin [mV]) of the dark signal output with the device junction temperature of 60 ˚C and the device in the light-obstructed state and 1/30 s integration. The measuring values substitute into the following formula.

   $$\Delta Vdt = Vdmax - Vdmin \text{ [mV]}$$

7. PLS
   Set the measurement condition to the standard imaging condition II, the Gr and Gb output signal Vave measured by standard image condition. Then, adjust the luminous intensity to 500 times the intensity with average value of the Gr and Gb signal output, Vave. When the charge drain is executed be the electronic shutter and the condition that not be readout from photo diode to analog memory, readout by dropping to 1/113 frame rate.

   $$Sm = 20 \times \log ((Vsm / Vave) \times (1 / 500) \times (1 / 113)) \text{ [dB]}$$

Setting Registers Using Serial Communication

Description of Setting Registers (4-wire)

The serial data input order is LSB-first transfer. The table below shows the various data types and descriptions.

Serial Data Transfer Order

Chip ID	Start address	Data	Data	Data	…
(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)

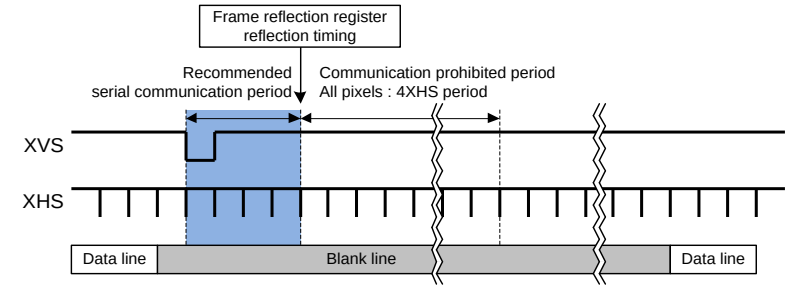
Type and Description

Type	Description
Chip ID	Chip ID: 02 Write: 02h / Read: 82h
	Chip ID: 03 Write: 03h / Read: 83h
	Chip ID: 04 Write: 04h / Read: 84h
	Chip ID: 05 Write: 05h / Read: 85h
	Chip ID: 06 Write: 06h / Read: 86h
	Chip ID: 07 Write: 07h / Read: 87h
	Chip ID: 08 Write: 08h / Read: 88h
	Chip ID: 09 Write: 09h / Read: 89h
	Chip ID: 0A Write: 0Ah / Read: 8Ah
	Chip ID: 0B Write: 0Bh / Read: 8Bh
	Chip ID: 0C Write: 0Ch / Read: 8Ch
	Chip ID: 0D Write: 0Dh / Read: 8Dh
	Chip ID: 0E Write: 0Eh / Read: 8Eh
	Chip ID: 0F Write: 0Fh / Read: 8Fh
	Chip ID: 10 Write: 10h / Read: 90h
	Chip ID: 11 Write: 11h / Read: 91h
	Chip ID: 12 Write: 12h / Read: 92h
	Chip ID: 13 Write: 13h / Read: 93h
Address	Designate the address according to the Register Map. When using a communication method that designates continuous addresses, the address is automatically incremented from the previously transmitted address.
Data	Input the setting values according to the Register Map.

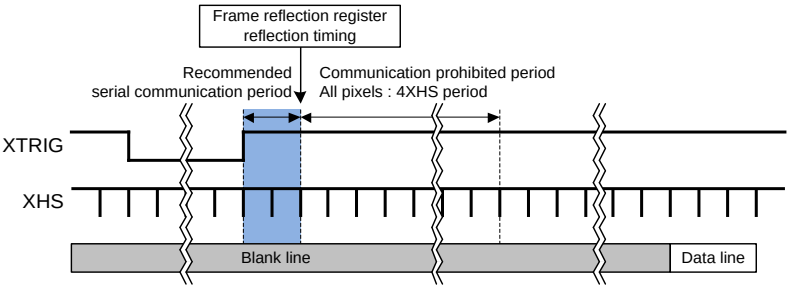
Register Communication Timing (4-wire)

Perform serial communication in sensor standby mode or within communication period. For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by frame reflection timing. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed.

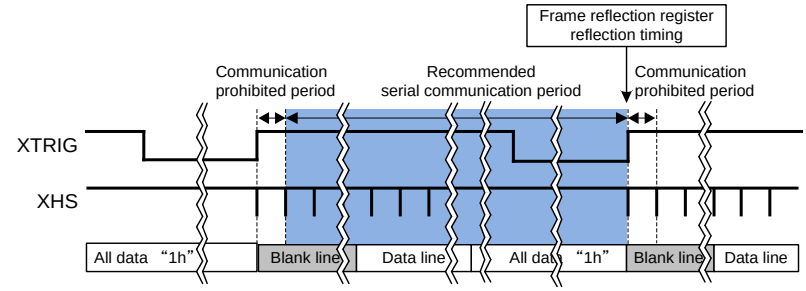
Global Shutter (Normal mode)



Global Shutter (Sequential Trigger mode)



Global Shutter (Fast Trigger mode)



Register Write and Read (4-wire)

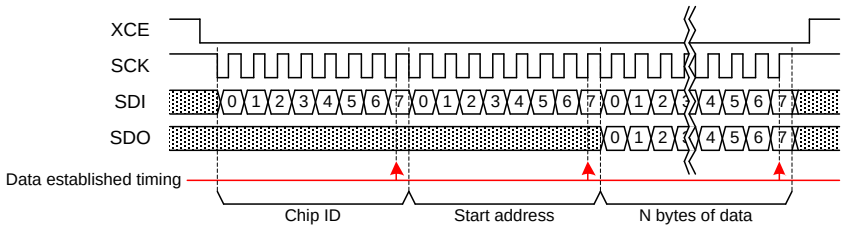
◆ Follow the communication procedure below when writing registers.

(1) Set XCE Low to enable the chip's communication function. Serial data input is executed using SCK and SDI.
(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
(3) Input the Chip ID (CID = 02h to 13h) to the first byte. If the Chip ID differs, subsequent data is ignored.
(4) Input the start address to the second byte. The address is automatically incremented.
(5) Input the data to the third and subsequent bytes. The data in the third byte is written to the register address designated by the second byte, and the register address is automatically incremented thereafter when writing the data for the fourth and subsequent bytes. Normal register data is loaded to the inside of the sensor and established in 8-bit units.
(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The register values before the write operation are output. The actual register values are the input data.
(7) Set XCE High to end communication.

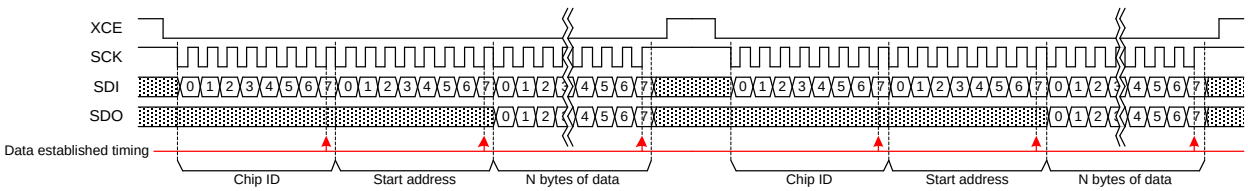
◆ Follow the communication procedure below when reading registers.

(1) Set XCE Low to enable the chip's communication function. Serial data input is executed using SCK and SDI.
(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
(3) Input Chip ID (CID = 82h to 93h) to the first byte. If the Chip ID differs, subsequent data is ignored.
(4) Input the start address to the second byte. The address is automatically incremented.
(5) Input data to the third and subsequent bytes. Input dummy data in order to read the registers. The dummy data is not written to the registers. To read continuous data, input the necessary number of bytes of dummy data.
(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The input data is not written, so the actual register values are output.
(7) Set XCE High to end communication.

Note) When writing data to multiple registers with discontinuous addresses, access to undesired registers can be avoided by repeating the above procedure multiple times.



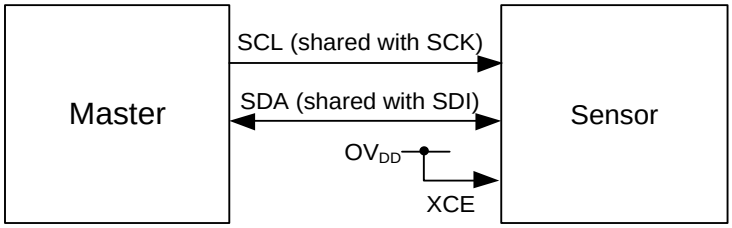
Serial Communication (Continuous Addresses)



Serial Communication (Discontinuous Addresses)

Description of Setting Registers (I^2C)

The serial data input order is MSB-first transfer. The table below shows the various data types and descriptions.



Pin connection of serial communication

The sensor can use two kinds of slave addresses by switching the polarity of SLAMODE Pin for one I^2C bus, and can use a common slave address in both polarities of SLAMODE Pin for one I^2C bus.

SLAVE Address (SLAMODE = 0)

MSB							LSB
0	1	1	0	1	1	0	R / W

SLAVE Address (SLAMODE = 1)

MSB							LSB
0	1	1	0	1	1	1	R / W

SLAVE Address (SLAMODE = 0 / 1)

MSB							LSB
0	0	1	1	0	1	0	R / W

* R/W is data direction bit

R/W

R / W bit	Data direction
0	Write (Master → Sensor)
1	Read (Sensor → Master)

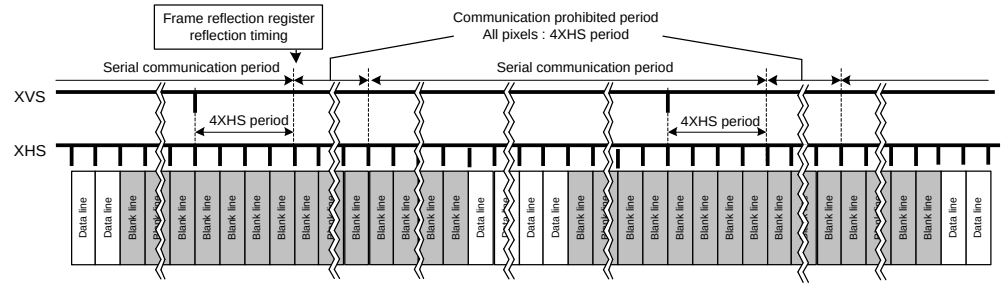
I^2C pin description

Symbol	Pin No.	Description
SCL (common to SCK)	J3	Serial clock input
SDA (common to SDI)	K3	Serial data communication

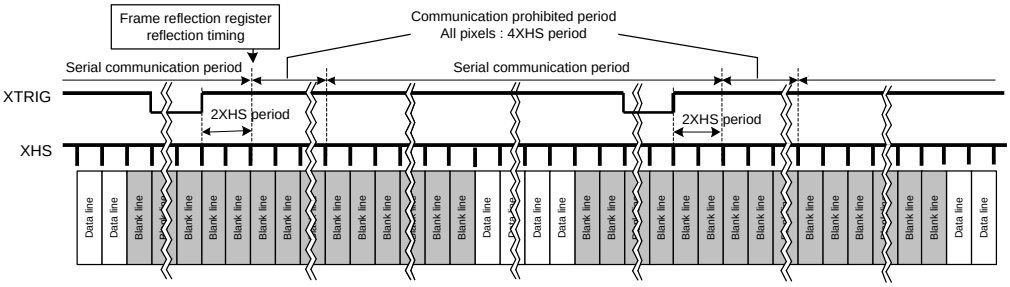
Register Communication Timing (I^2C)

In I^2C communication system, communication can be performed excluding during the period when communication is prohibited from the falling edge of XVS to 4H after.
For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by frame reflection timing. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed. Using REGHOLD function is recommended for register setting using I^2C communication. For REGHOLD function, see “Register Transmission Setting” in “Description of Functions”.

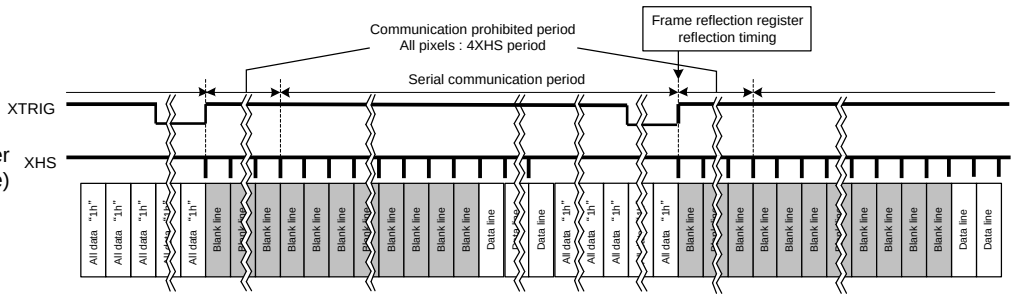
Global Shutter (Normal mode)



Global Shutter (Sequential Trigger mode)

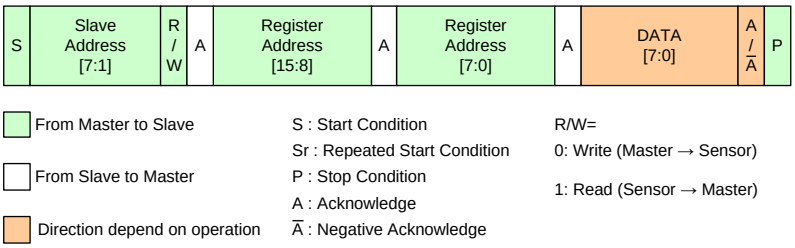


Global Shutter (Fast Trigger mode)



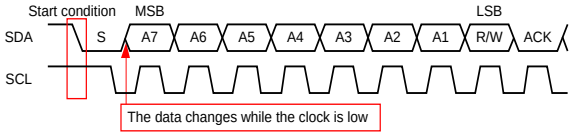
I²C Communication Protocol

I²C serial communication supports a 16-bit register address and 8-bit data message type.

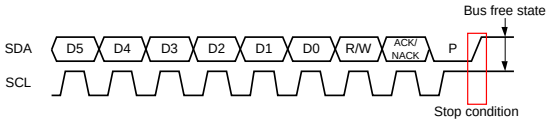


Communication protocol

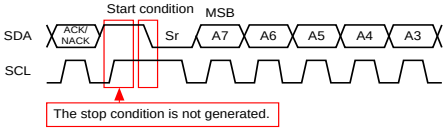
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) / Ā (Negative Acknowledge) is transferred. Data (SDA) is transferred at the clock (SCL) cycle. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start Condition is defined by SDA changing from High to Low while SCL is High. When the Stop Condition is not generated in the previous communication phase and Start Condition for the next communication is generated, that Start Condition is recognized as a Repeated Start Condition.



Start Condition

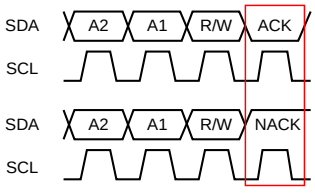


Stop Condition



Repeated Start Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge / Negative Acknowledge and release (does not drive) SDA. When Negative Acknowledge is generated, the Master must immediately generate the Stop Condition and end the communication.



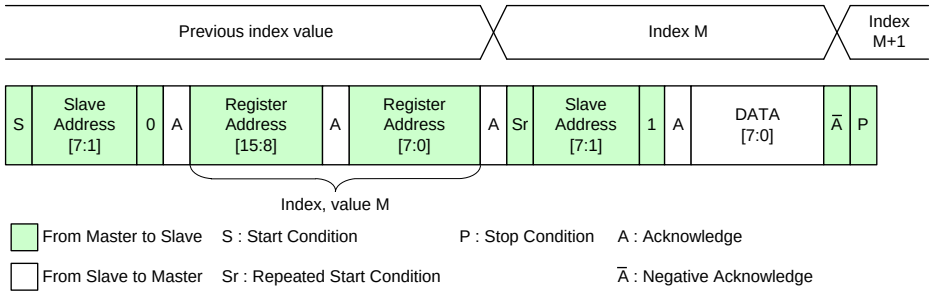
Acknowledge and Negative Acknowledge

I²C Serial Communication Read/Write Operation

This sensor supports the following four read operations and two write operations.

Single Read from Random Location

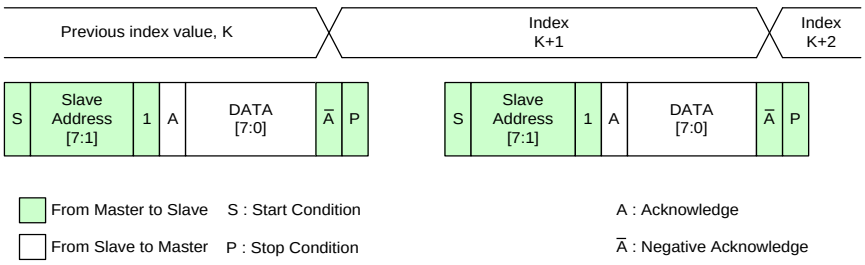
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the Start Condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop Condition to end the communication.



Single Read from Random Location

Single Read from Current Location

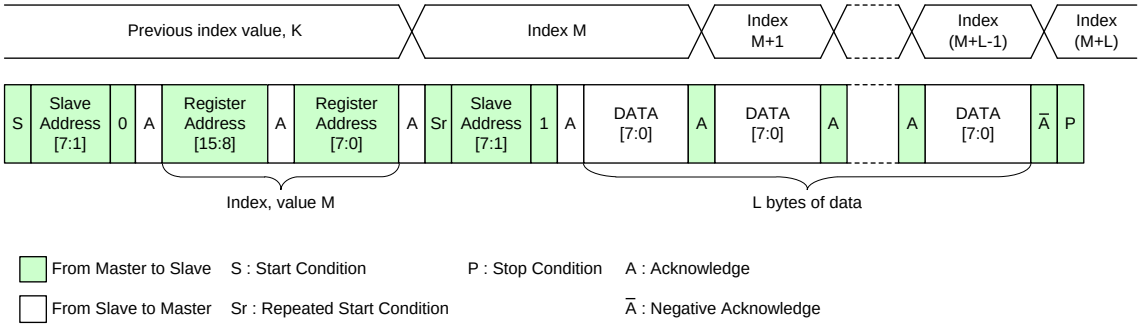
After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read/write is performed, the index is incremented by the subsequent Acknowledge/Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.



Single Read from Current Location

Sequential Read Starting from Random Location

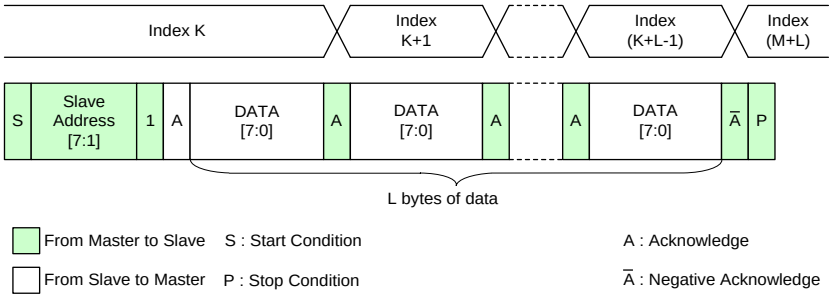
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Random Location

Sequential Read Starting from Current Location

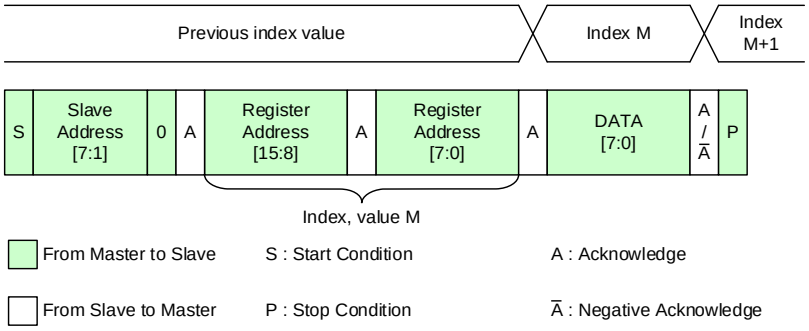
When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Current Location

Single Write to Random Location

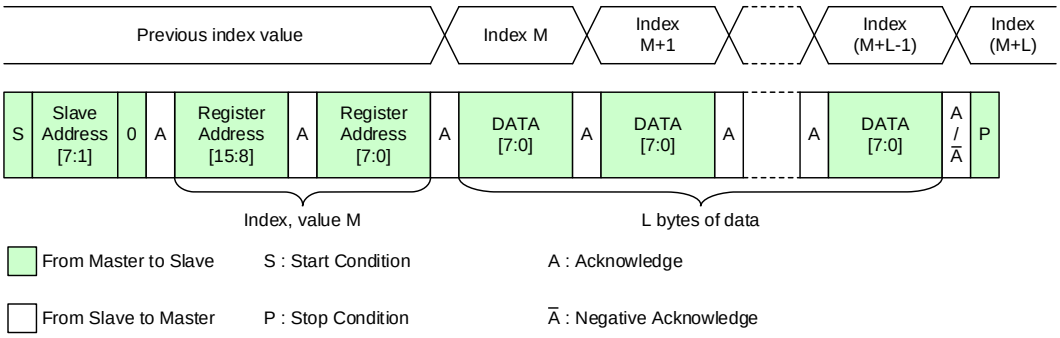
The Master sets the sensor index value to M by designating the sensor slave address with a write request, and designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop Condition to end the communication.



Single Write to Random Location

Sequential Write Starting from Random Location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop Condition to end the communication.



Sequential Write Starting from Random Location

Register Map

This sensor has a total of 4608 bytes of registers, composed of registers with address 00h to FFh that correspond to Chip ID = 02h to 13h. Use the initial values for empty address. Some registers must be change from the initial values, so the sensor control side should be capable of setting 4608 bytes.

There are three different register reflection timings.
About the Reflection timing column of the Register Map, registers noted as "I" are reflected immediately after writing to register, registers noted as "S" are set during standby mode and reflected after standby canceled, registers noted as "V" are reflected at “Fame reflection register reflection timing” on the figure described in the section of “Setting Registers with Serial Communication”.

Do not perform communication to addresses not listed in the Register Map. Doing so may result in operation errors.

Chip ID = 02 (Write: Chip ID = 02h, Read: Chip ID = 82h, I²C: 30**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
00h	3000h	0	STANDBY [0]	Standby mode 0: Normal operation 1: Standby	1	01h	I
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
08h	3008h	0	REGHOLD [0]	Register hold (Function not to update V reflection registers) 0: Invalid 1: Valid	0	00h	I
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
0A	300Ah	0	XMSTA [0]	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop	1	01h	I
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
0Bh	300Bh	0	TRIGEN [0]	Global shutter mode setting 0: Normal mode 1: Trigger mode	0	00h	S
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
0Eh	300Eh	0	VREVERSE [0]	Vertical (V) direction readout inversion control 0: Normal 1: Inverted	0	00h	V
		1	HREVERSE [0]	Horizontal (H) direction readout inversion control 0: Normal 1: Inverted	0		V
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
10h	3010h	0	VMAX [19:0]	LSB	0046Ah	6Ah	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
11h	3011h	0				04h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
12h	3012h	0				00h	
		1					
		2					
		3		MSB			
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
14h	3014h	0	HMAX [15:0]	LSB	0122h	22h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7		When sensor master mode horizontal span setting. (Number of operation clocks count from 1)			
15h	3015h	0				01h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
26h	3026h	0	TOUT1SEL [1:0]	TOUT1 pin setting 0h: Low fixed 3h: Pulse output	0h	00h	S
		1					
		2	TOUT2SEL [1:0]	TOUT2 pin setting 0h: Low fixed 3h: Pulse output	0h		S
		3					
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
29h	3029h	0	TRIG_TOUT1_SEL [2:0]	TOUT1 pin setting 0h: Low fixed 1h: Pulse1 output	0h	00h	S
		1					
		2					
		3		Fixed to 0	0		—
		4	TRIG_TOUT2_SEL [2:0]	TOUT2 pin setting 0h: Low fixed 2h: Pulse2 output	0h		S
		5					
		6					
		7		Fixed to 0	0		—
36h	3036h	0		Fixed to 0	0	C0h	—
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4	SYNCSEL	XHS, XVS pin setting 0h: Normal Output 3h: Hi-Z	0h		S
		5					
		6		Fixed to 1	1		—
		7		Fixed to 1	1		—
6Dh	306Dh	0	PULSE1_EN_NOR [0]	Pulse1 output in normal mode 0: Disable 1: Enable	0	00h	S
		1	PULSE1_EN_TRIG [0]	Pulse1 output in trigger mode 0: Disable 1: Enable	0		S
		2	PULSE1_POL	Pulse1 polarity selection 0: High active 1: Low active	0		S
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
70h	3070h	0	PULSE1_UP [19:0]	LSB	00000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
71h	3071h	0		Pulse1 active period start timing setting Designated in line units from reference point (For details, see the “Pulse Output Function”)		00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
72h	3072h	0				00h	
		1					
		2					
		3		MSB			
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
74h	3074h	0	PULSE1_DN [19:0]	LSB	00000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
75h	3075h	0		Pulse1 active period end timing setting Designated in line units from readout start (For details, see the “Pulse Output Function”)		00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
76h	3076h	0				00h	
		1					
		2					
		3		MSB			
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
79h	3079h	0	PULSE2_EN_NOR [0]	Pulse2 output in normal mode 0: Disable 1: Enable	0	00h	S
		1	PULSE2_EN_TRIG [0]	Pulse2 output in trigger mode 0: Disable 1: Enable	0		S
		2	PULSE2_POL [0]	Pulse2 polarity selection 0: High active 1: Low active	0		S
		3		Fixed to 1	0		S
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
7Ch	307Ch	0	PULSE2_UP [19:0]	LSB	00000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
7Dh	307Dh	0		Pulse2 active period start timing setting Designated in line units from reference point (For details, see the “Pulse Output Function”)		00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
7Eh	307Eh	0				00h	
		1					
		2					
		3		MSB			
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
80h	3080h	0	PULSE2_DN [19:0]	LSB	00000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
81h	3081h	0		Pulse2 active period end timing setting Designated in line units from reference point (For details, see the “Pulse Output Function”)		00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
82h	3082h	0				00h	
		1					
		2					
		3		MSB			
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
89h	3089h	[7:0]	INCKSEL0 [7:0]	Set according to INCK frequency and drive mode.	80h	80h	S
8Ah	308Ah	[7:0]	INCKSEL1 [7:0]	Set according to INCK frequency and drive mode.	0Fh	0Fh	S
8Bh	308Bh	[7:0]	INCKSEL2 [7:0]	Set according to INCK frequency and drive mode.	80h	80h	S
8Ch	308Ch	[7:0]	INCKSEL3 [7:0]	Set according to INCK frequency and drive mode.	0Ch	0Ch	S
8Dh	308Dh	0	SHS [19:0]	LSB	0000Eh	0Eh	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
8Eh	308Eh	0		Storage time adjustment Designated in line unit		00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
8Fh	308Fh	0				00h	
		1					
		2					
		3		MSB			
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
AAh	30AAh	0	VINT_EN	Setting of Interrupt mode in Trigger Mode 0: V interrupt is disable 1: V interrupt is enable	1	01h	S
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
AEh	30AEh	0	LOWLAGTRG	Selection of trigger mode 0: Except for Fast trigger mode 1: Fast trigger mode	0	00h	S
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Chip ID = 03 (Write: Chip ID = 03h, Read: Chip ID = 83h, I^2C: 31h)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 04 (Write: Chip ID = 04h, Read: Chip ID = 84h, I²C: 32**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
04h	3204h	0	GAIN [8:0]	LSB Gain setting 0 dB (000d) to 48 dB (480d) 0.1 dB Step (Refer to Adderss 12h about detail of Reflection Timing.)	000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
05h	3205h	0		MSB		00h	
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
12h	3212h	[7:0]	GAINDLY	Setting of Gain Reflection Timing at Nomal mode. 08h: Gain reflect at the frame 09h: Gain reflect at the next frame (Same timing as SHS reflecting output.) Others: Setting prohibited	00h	00h	S
54h	3254h	0	BLKLEVEL [11:0]	LSB Black level offset value setting Recommended value. 03Ch: 10 bit	03Ch	3Ch	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
55h	3255h	0				00h	
		1					
		2					
		3		MSB			
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Chip ID = 05 (Write: Chip ID = 05h, Read: Chip ID = 85h, I²C: 33**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
00h	3300h	0	FID0_ROIH1ON [0]	The horizontal setting of FID0 ROI area (1, 1) 0: Disable 1: Enable	0	00h	V
		1	FID0_ROIV1ON [0]	The vertical setting of FID0 ROI area (1, 1) 0: Disable 1: Enable	0		I
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
10h	3310h	[7:0]	FID0_ROIPH1 [12:0]	Designation of horizontal cropping position for FID0 on area (1, 1) *Set the value of multiple of 4	0000h	00h	V
11h	3311h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
12h	3312h	[7:0]	FID0_ROIPV1 [11:0]	Designation of vertical cropping position for FID0 on area (1, 1) *Set the value of multiple of 4	000h	00h	I
13h	3313h	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
14h	3314h	[7:0]	FID0_ROIWH1 [12:0]	Designation of horizontal cropping size for FID0 on area (1, 1) *Set the value of multiple of 4	0000h	00h	V
15h	3315h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
16h	3316h	[7:0]	FID0_ROIWV1 [11:0]	Designation of vertical cropping size for FID0 on area (1, 1) *Set the value of multiple of 4	000h	00h	I
17h	3317h	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—

Chip ID = 06 (Write: Chip ID = 06h, Read: Chip ID = 86h, I²C: 34**h)

Please refer to the other register map file for the register that has not been described.

Chip ID = 07 (Write: Chip ID = 07h, Read: Chip ID = 87h, I²C: 35**h)

Please refer to the other register map file for the register that has not been described.

Chip ID = 08 (Write: Chip ID = 08h, Read: Chip ID = 88h, I²C: 36**h)

Please refer to the other register map file for the register that has not been described.

Chip ID = 09 (Write: Chip ID = 09h, Read: Chip ID = 89h, I²C: 37**h)

Please refer to the other register map file for the register that has not been described.

Chip ID = 0A (Write: Chip ID = 0Ah, Read: Chip ID = 8Ah, I²C: 38**h)

Please refer to the other register map file for the register that has not been described.

Chip ID = 0B (Write: Chip ID = 0Bh, Read: Chip ID = 8Bh, I²C: 39**h)

Please refer to the other register map file for the register that has not been described.

Chip ID = 0C (Write: Chip ID = 0Ch, Read: Chip ID = 8Ch, I²C: 3A**h)

Please refer to the other register map file for the register that has not been described.

Chip ID = 0D (Write: Chip ID = 0Dh, Read: Chip ID = 8Dh, I²C: 3B**h)

Please refer to the other register map file for the register that has not been described.

Chip ID = 0E (Write: Chip ID = 0Eh, Read: Chip ID = 8Eh, I²C: 3C**h)

Please refer to the other register map file for the register that has not been described.

Chip ID = 0F (Write: Chip ID = 0Fh, Read: Chip ID = 8Fh, I²C: 3D**h)

Please refer to the other register map file for the register that has not been described.

Chip ID = 10 (Write: Chip ID = 10h, Read: Chip ID = 90h, I²C: 3E**h)

Please refer to the other register map file for the register that has not been described.

Chip ID = 11 (Write: Chip ID = 11h, Read: Chip ID = 91h, I²C: 3F**h)

Please refer to the other register map file for the register that has not been described.

Chip ID = 12 (Write: Chip ID = 12h, Read: Chip ID = 92h, I²C: 40**h)

Please refer to the other register map file for the register that has not been described.

Chip ID = 13 (Write: Chip ID = 13h, Read: Chip ID = 93h, I²C: 41**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
14h	4114h	0	GTTABLENUM	MIPI Global Timing setting	05h	C5h	S
		1					
		2					
		3					
		4					
		5					
		6		Fixed to 1	1		—
		7		Fixed to 1	1		—
8Ch	418Ch	[7:0]		INCK = 74.25MHz : E8h (232d) INCK = 54MHz : A8h (168d) INCK = 37.125MHz : 74h (116d)	E8h	E8h	S

Readout Drive Modes

The table below lists the operating modes available with this sensor. (The value is the Max. frame rate.)

Drive mode	Frame rate [frame/s]	Data rate [Gbps]	CSI-2 Lane[*1]	A/D conversion	Number of recording pixels		Total number[*2] of pixels		Number of INCK in 1H		
					H	V	H	V	INCK: 37.125 MHz	INCK: 74.25 MHz	INCK: 54 MHz
All pixel	60.3	1.188	1	10	1440	1080	1760	1118	550.0	1100.0	800.0
ROI	[*4]	1.188	1	10	[*3]	[*3]	1760	[*4]	550.0	1100.0	800.0

[*1] The data rate of the output lane is value that is obtained by total data rate divided by the number of lane.
Example) In All-pixel 60.3 [frame/s] mode: 1.118 [Gbps] / 1 = 1188 [Mbps]

[*2] For the setting value to register HMAX / VMAX, see the section of each drive mode settings

[*3] Designated cropping area (ROI)

[*4] See the section of “ROI mode”

Image Data Output Format (CSI-2 output)

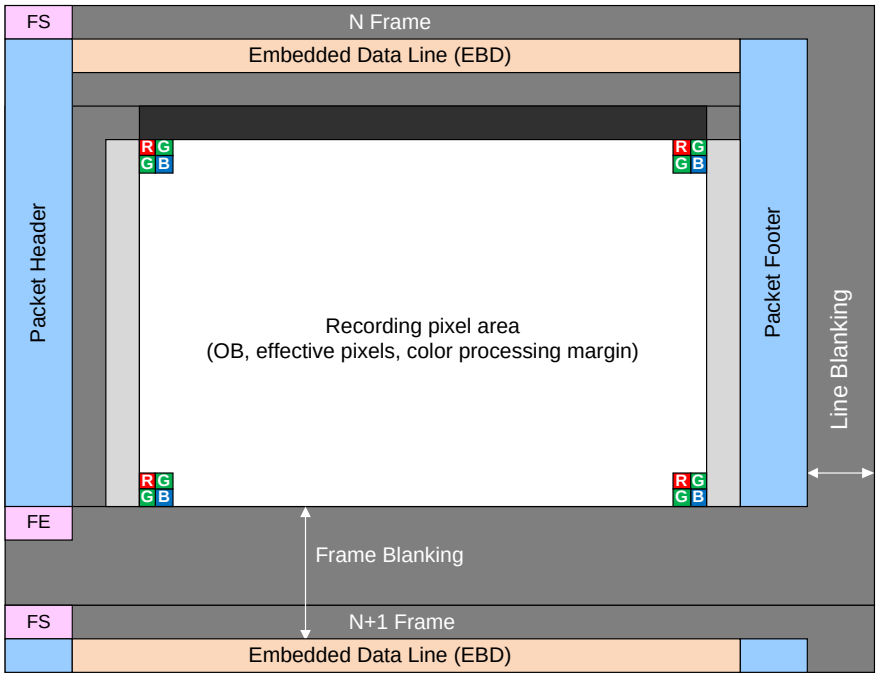
Frame Format

Each line of each image frame is output like the General Frame Format of CSI-2. The settings for each packet header are shown below.

DATA Type

Header [5:0]	Name	Description
00h	Frame Start Code	FS
01h	Frame End Code	FE
10h	NULL	Invalid data
12h	Embedded Data	Embedded data
2Bh	RAW10	0A0Ah
37h	OB Data	Vertical OB line data

Frame Structure



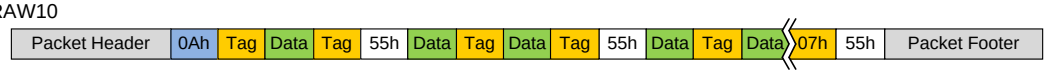
Frame Structure of CSI-2 output

Embedded Data Line

The Embedded data line is output in a line following the sync code FS.

Embedded Data Format

RAW10



The end of the address and the register value is determined according to the tags embedded in the data.

Embedded Data Line Tag

Tag	Data Byte Description
00h	Illegal Tag. If found; treat as end of Data.
07h	End of Data.
AAh	CCI Register Index MSB [15:8]
A5h	CCI Register Index LSB [7:0]
5Ah	Auto increment the CCI index after the data byte – valid data Data byte contains valid CCI register data.
55h	Auto increment the CCI index after the data byte – null data A CCI register does not exist for the current CCI index. The data byte value is the 07h.
FFh	Illegal Tag. If found; treat as end of Data.

Specific output examples are shown below. The embedded data is first line. (4-wire: Chip ID = 13h)

Pixel	Address [HEX]		Data Byte Description	Value
	4-wire	I²C		
1	-		Data Format	0Ah
2			CCI Register Index MSB [15:8]	AAh
3				41h
4			CCI Register Index LSB [7:0]	A5h
5				A8h
6	A8h	41A8h	Frame count	5Ah
7				[7:0]*
8	A9h	41A9h	Fixed to "00h"	5Ah
9				00h
10	AAh	41AAh	Black level setting value	5Ah
11				[7:0]*
12	ABh	41ABh		5Ah
13				[15:8]*
14	ACh	41ACh	Fixed to "07h"	5Ah
15				07h
16	ADh	41ADh	HREVERSE setting value	5Ah
17			VREVERSE setting value	[7:0]*
18	AEh	41AEh	Fixed to "00h"	5Ah
19				00h
20	AFh	41AFh	Fixed to "00h"	5Ah
21				00h
22	B0h	41B0h	Fixed to "00h"	5Ah
23				00h
24	B1h	41B1h	TRIGEN setting value	5Ah
25				[7:0]*
26	B2h	41B2h	Fixed to "07h"	5Ah
27				07h
28	B3h	41B3h	Fixed to "07h"	5Ah
29				07h
30	B4h	41B4h	Shutter setting value	5Ah
31				[7:0]*
32	B5h	41B5h		5Ah
33				[15:8]*
34	B6h	41B6h		5Ah
35				[23:16]*
36	B7h	41B7h	Fixed to "07h"	5Ah
37				07h
38	B8h	41B8h	Gain Setting Value	5Ah
39				[7:0]*
40	B9h	41B9h		5Ah
41				[15:8]*
42	BAh	41BAh		5Ah
43				[23:16]*
44	BBh	41BBh		5Ah
45				[31:24]*
46	BCh	41BCh	Fixed to "07h"	5Ah
47				07h
48	BDh	41BDh	Fixed to “07h”	5Ah
49				07h
50	BEh	41BEh	Fixed to “07h”	5Ah
51				07h
52	BFh	41BFh	Fixed to “07h”	5Ah
53				07h

Pixel	Address [HEX]		Data Byte Description	Value
	4-wire	I²C		
54	C0h	41C0h	Fixed to “07h”	5Ah
55				07h
56	C1h	41C1h	Fixed to “07h”	5Ah
57				07h
58	C2h	41C2h	Fixed to “07h”	5Ah
59				07h
60	C3h	41C3h	Fixed to “07h”	5Ah
61				07h
62	C4h	41C4h	Fixed to “07h”	5Ah
63				07h
64	C5h	41C5h	Fixed to “07h”	5Ah
65				07h
66	C6h	41C6h	Fixed to “07h”	5Ah
67				07h
68	C7h	41C7h	Fixed to “07h”	5Ah
69				07h
70	C8h	41C8h	Fixed to “07h”	5Ah
71				07h
72	C9h	41C9h	Fixed to “07h”	5Ah
73				07h
74	CAh	41CAh	Fixed to “07h”	5Ah
75				07h
76	CBh	41CBh	Fixed to “07h”	5Ah
77				07h
78	—	—	End of Data.	07h
79				07h
80				07h

* The value that shown in Data Byte Description is output.

Specific output examples are shown below. The embedded data is second line (4-wire: Chip ID = 13h)

Pixel	Address [HEX]		Data Byte Description	Value
	4-wire	I²C		
1	-		Data Format	0Ah
2			CCI Register Index MSB [15:8]	AAh
3				41h
4			CCI Register Index LSB [7:0]	A5h
5				CCh
6	CCh	41CCh	Vertical line value (VMAX)	5Ah
7				[7:0]*
8	CDh	41CDh		5Ah
9				[15:8]*
10	CEh	41CEh		5Ah
11				[23:16]*
12	CFh	41CFh	Fixed to “07h”	5Ah
13				07h
14	D0h	41D0h	Horizontal clock value (HMAX)	5Ah
15				[7:0]*
16	D1h	41D1h		5Ah
17				[15:8]*
18	D2h	41D2h	Fixed to “07h”	5Ah
19				07h
20	D3h	41D3h	FID0_ROIH1ON setting value	5Ah
21			FID0_ROIV1ON setting value	[7:0]*
22	D4h	41D4h	FID0_ROIPH1 setting value	5Ah
23				[7:0]*
24	D5h	41D5h		5Ah
25				[15:8]*
26	D6h	41D6h	FID0_ROIPV1 setting value	5Ah
27				[7:0]*
28	D7h	41D7h		5Ah
29				[15:8]*
30	D8h	41D8h	FID0_ROIWH1 setting value	5Ah
31				[7:0]*
32	D9h	41D9h		5Ah
33				[15:8]*
34	DAh	41DAh	FID0_ROIWV1 setting value	5Ah
35				[7:0]*
36	DBh	41DBh		5Ah
37				[15:8]*
38	DCh	41DCh	Fixed to “07h”	5Ah
39				07h
40	DDh	41DDh	Fixed to “07h”	5Ah
41				07h
42	DEh	41DEh	Fixed to “07h”	5Ah
43				07h
44	DFh	41DFh	Fixed to “07h”	5Ah
45				07h
46	E0h	41E0h	Fixed to “07h”	5Ah
47				07h
48	E1h	41E1h	Fixed to “07h”	5Ah
49				07h
50	E2h	41E2h	Fixed to “07h”	5Ah
51				07h
52	BFh	41E3h	Fixed to “07h”	5Ah
53				07h
54	E4h	41E4h	Fixed to “07h”	5Ah
55				07h
56	E5h	41E5h	Fixed to “07h”	5Ah
57				07h
58	E6h	41E6h	Fixed to “07h”	5Ah
59				07h
60	E7h	41E7h	Fixed to “07h”	5Ah
61				07h
62	E8h	41E8h	Fixed to “07h”	5Ah
63				07h
64	E9h	41E9h	Fixed to “07h”	5Ah
65				07h
66	EAh	41EAh	Fixed to “07h”	5Ah
67				07h
68	EBh	41EBh	Fixed to “07h”	5Ah
69				07h
70	ECh	41ECh	Fixed to “07h”	5Ah
71				07h
72	EDh	41EDh	Fixed to “00h”	5Ah
73				00h
74	—	—	End of Data.	07h
75				07h
76				07h

* The value that shown in Data Byte Description is output.

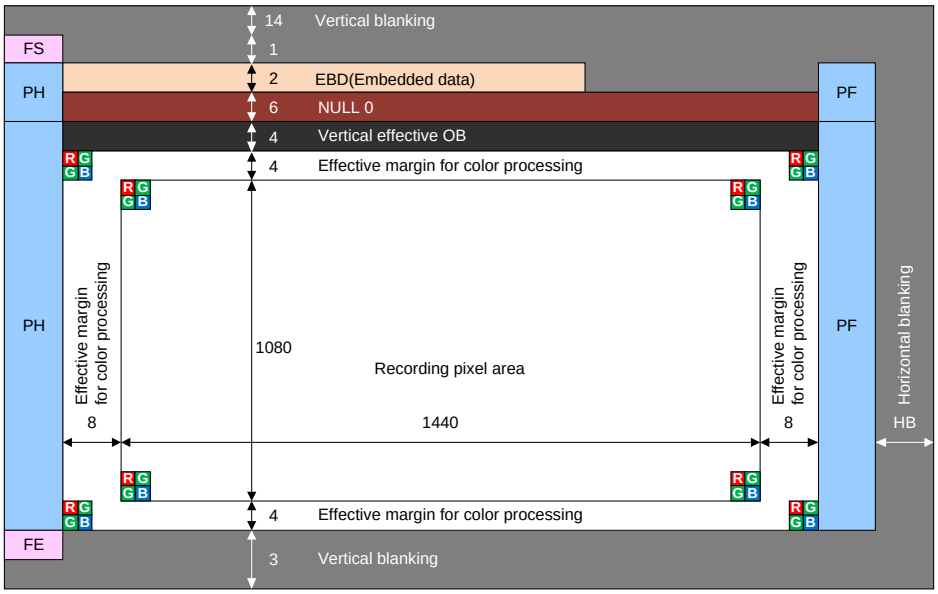
Image Data Output Format

All-pixel scan

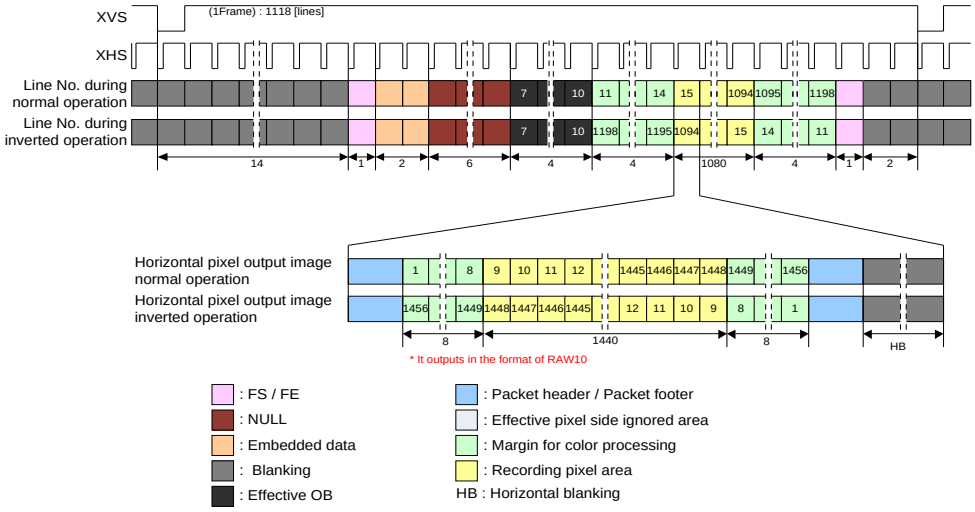
Register List of All-pixel scan mode

Please refer to the other register map file for the register that has not been described.

Address	bit	Register name	Initial Value	Setting value AD = 10 bit 60.3 [frame/s]	Remarks
Chip ID = 02h					
10h	[7:0]	VMAX	46Ah	45Eh	1118 line
11h	[7:0]				
12h	[3:0]				
14h	[7:0]	HMAX	122h	44Ch	
15h	[7:0]				
89h	[7:0]	INCKSEL0	80h	INCK = 37.125 MHz: 80h INCK = 54 MHz: B0h INCK = 74.25 MHz: 80h	
8Ah	[7:0]	INCKSEL1	0Fh	INCK = 37.125 MHz: 0Bh INCK = 54 MHz: 0Fh INCK = 74.25 MHz: 0Fh	
8Bh	[7:0]	INCKSEL2	80h	INCK = 37.125 MHz: 80h INCK = 54 MHz: B0h INCK = 74.25 MHz: 80h	
8Ch	[7:0]	INCKSEL3	0Ch	INCK = 37.125 MHz: 08h INCK = 54 MHz: 0Ch INCK = 74.25 MHz: 0Ch	
Chip ID = 04h					
54h	[7:0]	BLKLEVEL	03Ch	03Ch	Recommended value
55h	[3:0]				
Chip ID = 13h					
8Ch	[7:0]		E8h	INCK = 74.25MHz : E8h (232d) INCK = 54MHz : A8h (168d) INCK = 37.125MHz : 74h (116d)	



Pixel Array Image Drawing in All-pixel scan Mode



Drive Timing Chart for Serial Output in All-pixel Scan Mode

ROI mode

This Sensor has ROI function that signals are cut out and read out in multi arbitrary positions.
Cropping position can set maximum 1 areas that specified by horizontal 1 points and vertical 1 points, regarding effective pixel start position as origin (0, 0) in all pixel scan mode. Cropping is available from All-pixel scan mode and horizontal period are fixed to the value for this mode.
This cropped area by horizontal cropping setting (ROI (1, 1)) is output with left justified and that extends the horizontal blanking period. In vertical cropping area (ROI (1, 1)), the number of image data is also output from cropping start line and the frame rate can be adjusted by changing the number of input XVS lines in slave mode or changing register VMAX in master mode.
One invalid frame is generated when the ROI area changing size or cropping address.
ROI image is shown in the figure below.
This section is written in case of all-pixel scan mode for example on this document.

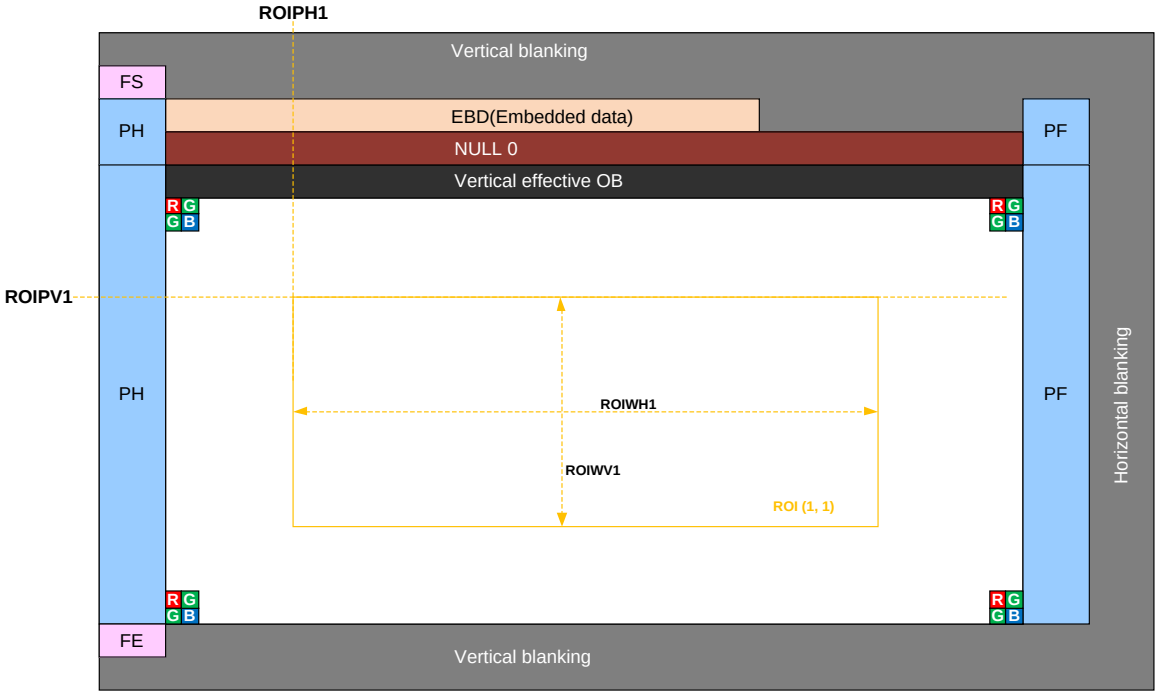
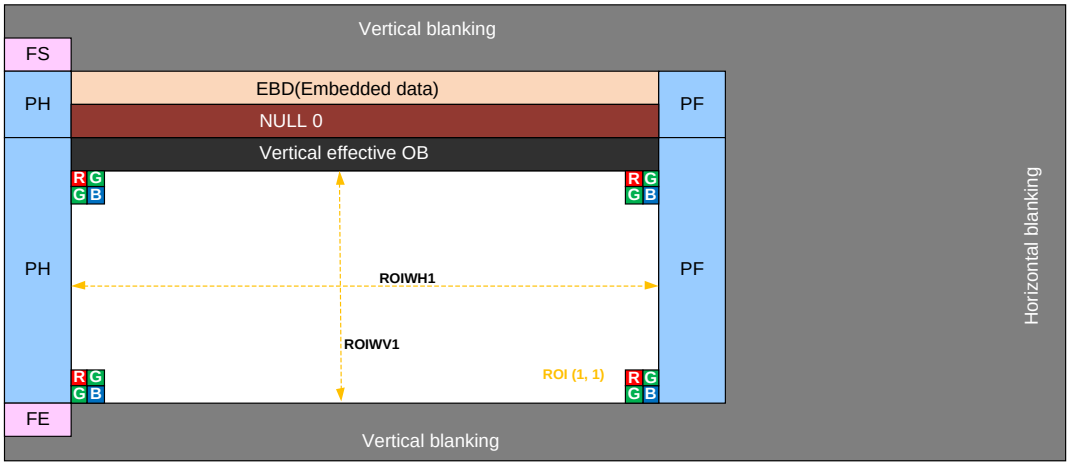


Image Drawing of Designated Areas in ROI Mode



Details of Image Drawing

Register List of ROI mode

Please set All-pixel scan mode to the settings other than the following.

Address	bit	Register name	Initial Value	Setting value AD = 10 bit *1 [frame/s]	Remarks
Chip ID = 02h					
10h	[7:0]	VMAX	46Ah	*1	
11h	[7:0]				
12h	[3:0]				
14h	[7:0]	HMAX	122h	44Ch	
15h	[7:0]				
89h	[7:0]	INCKSEL0	80h	INCK = 37.125 MHz: 80h INCK = 54 MHz: B0h INCK = 74.25 MHz: 80h	
8Ah	[7:0]	INCKSEL1	0Fh	INCK = 37.125 MHz: 0Bh INCK = 54 MHz: 0Fh INCK = 74.25 MHz: 0Fh	
8Bh	[7:0]	INCKSEL2	80h	INCK = 37.125 MHz: 80h INCK = 54 MHz: B0h INCK = 74.25 MHz: 80h	
8Ch	[7:0]	INCKSEL3	0Ch	INCK = 37.125 MHz: 08h INCK = 54 MHz: 0Ch INCK = 74.25 MHz: 0Ch	
Chip ID = 04h					
54h	[7:0]	BLKLEVEL	03Ch	03Ch	Recommended value
55h	[3:0]				
Chip ID = 05h					
00h	[0]	FID0_ROIH1ON	0	The horizontal setting of FID0 ROI area (1, 1) 0: Disable 1: Enable	
	[1]	FID0_ROIV1ON	0	The vertical setting of FID0 ROI area (1, 1) 0: Disable 1: Enable	
10h	[7:0]	FID0_ROIPH1	0000h	Designation of horizontal cropping position for FID0 on area (1, 1) *Set the value of multiple of 4	
11h	[4:0]				
12h	[7:0]	FID0_ROIPV1	000h	Designation of vertical cropping position for FID0 on area (1, 1) *Set the value of multiple of 4	
13h	[3:0]				
14h	[7:0]	FID0_ROIWH1	0000h	Designation of horizontal cropping size for FID0 on area (1, 1) *Set the value of multiple of 4	
15h	[4:0]				
16h	[7:0]	FID0_ROIWV1	000h	Designation of vertical cropping size for FID0 on area (1, 1) *Set the value of multiple of 4	
17h	[3:0]				
Chip ID = 13h					
8Ch	[7:0]		E8h	INCK = 74.25MHz : E8h (232d) INCK = 54MHz : A8h (168d) INCK = 37.125MHz : 74h (116d)	

Restrictions on ROI mode

The register settings should satisfy following conditions:

ROIPH1 + ROIWH1 ≤ 1456d

ROIPV1 + ROIWV1 ≤ 1088d

* Set the horizontal and vertical setting in multiple of 4.

* Minimum width of the window is as below.
  ROIWH1 ≥ 80d

  ROIWV1 ≥ 4d

Frame rate on ROI mode

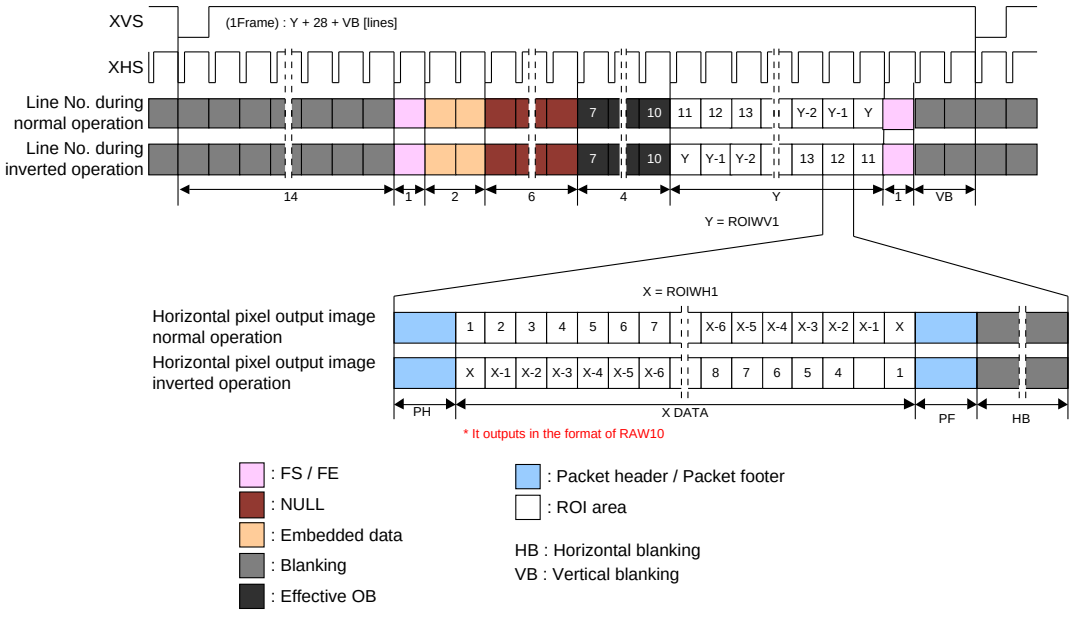
Frame rate [frame/s] = 1 / ((“Number of lines per frame” or VMAX) × (1 H period))

* Number of lines per frame or VMAX = ROIWV1 + 30
* 1 H period:
  Calculate by number of INCK in 1 H and the period of INCK.

The example of ROI setting is shown below.
  ROIWV1 = 600
  ROIWV1 = 4 (minimum value)

Frame rate List of each setting

Register settings No. in register list	1 H period [µs]	Frame rate [frame/s]	
		Total number of ROI 600 [line]	Total number of ROI 4 [line]
*1	14.81	107.14	1985.29



Drive Timing Chart for Serial Output in ROI Mode

Description of Various Function

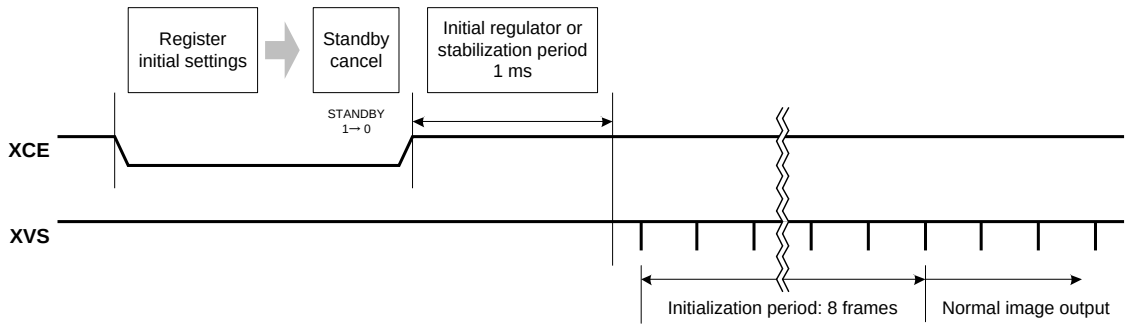
Standby mode

This sensor stops its operation and goes into standby mode which reduces the power consumption by writing “1” to the standby control register STANDBY. Standby mode is also established after power-on or other system reset operation.

Register List of Standby setting

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address ( ) : I^2C	bit			
STANDBY	02h	00h (3000h)	[0]	1h	1h: Standby 0h: Operating	Register communication is executed even in standby mode.

The serial communication registers hold the previous values. However, the address registers transmitted in standby mode are overwritten. The serial communication block operates even in standby mode, so standby mode can be canceled by setting the STANDBY register to “0”. Some time is required for sensor internal circuit stabilization after standby mode is canceled. For details on the sequence of setting and cancel of standby mode, see the sensor setting flow after power on.
After standby mode is canceled, a normal image is output from the 9 frames after internal regulator stabilization (1 ms or more).



Sequence from Standby Cancel to Stable Image Output

Slave Mode and Master Mode

The sensor can be switched between slave mode and master mode.
The switching is made by the XMASTER pin. Establish the XMASTER pin status before canceling the system reset. (Do not switch this pin status during operation.)
Input a vertical sync signal to XVS and input a horizontal sync signal to XHS when a sensor is in slave mode.
For sync signal interval, input data lines to output for vertical sync signal and 1H period designated in each operating mode for horizontal sync signal. See the section of "Readout Drive mode" for the number of output data line and 1H period.
Set the XMSTA register to “0” in order to start the operation after setting to master mode. In addition, set the count number of sync signal in vertical direction by the VMAX [19:0] register and the clock number in horizontal direction by the HMAX [15:0] register. See the description of operation mode for details of the section of “Readout Drive Modes”.

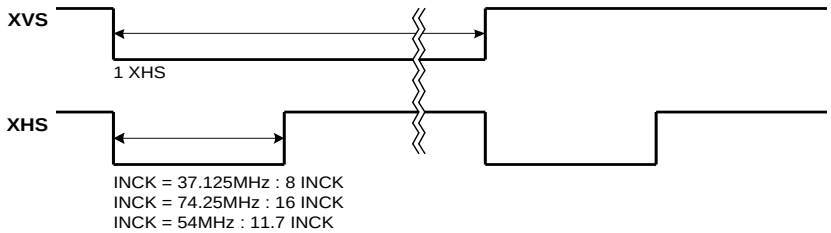
Pin Processing

Pin name	Pin processing	Operation mode	Remarks
XMASTER pin	Low fixed	Master mode	High: OV_{DD} Low: GND
	High fixed	Slave mode	

Register List of Slave Mode and Master Mode

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address ( ) : I^2C	Bit			
XMSTA	02h	0Ah (300Ah)	[0]	1h	1h: Master operation ready (Initial value) 0h: Master operation start	The master operation starts by setting 0.
VMAX [19:0]		10h (3010h)	[7:0]	0046Ah	See the item of each drive mode	Line number per frame designated (Master mode and Slave mode common setting.)
		11h (3011h)	[7:0]			
		12h (3012h)	[3:0]			
HMAX [15:0]		14h (3014h)	[7:0]	0122h	See the item of each drive mode	Clock number per line designated (Master mode and Slave mode common setting.)
		15h (3015h)	[7:0]			

XVS / XHS Output Waveform in Master Mode



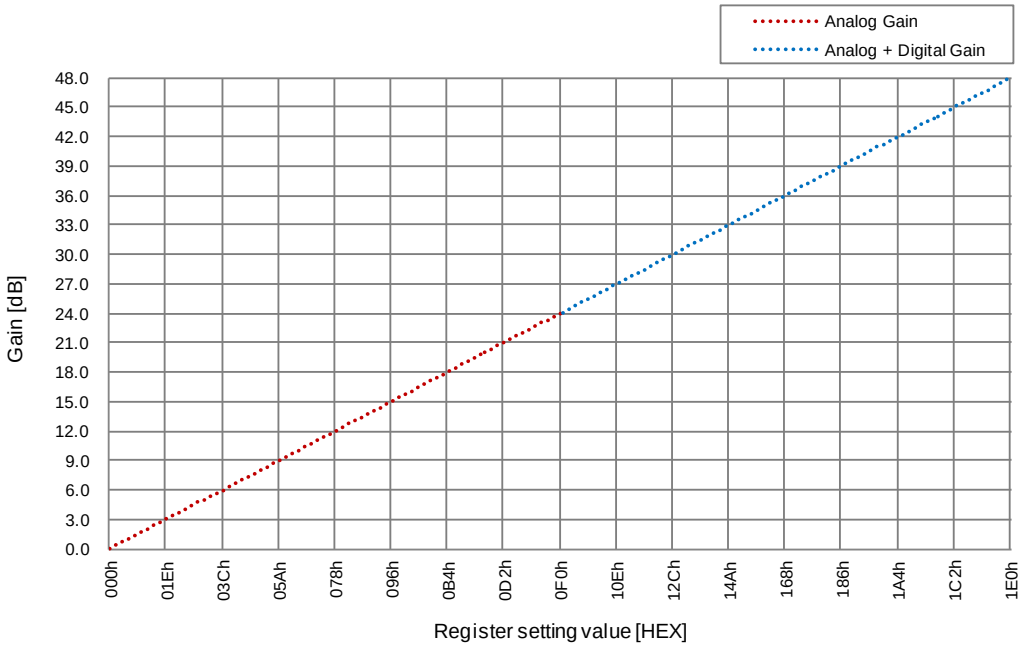
Gain Adjustment Function

PGC

The Programmable Gain Control (PGC) of this device consists of the analog block and digital block.
The total of analog gain and digital gain can be set up to 48 dB by the GAIN [8:0] register setting.
The value which is ten times the gain is set to register.

Example)
When set to 6 dB:

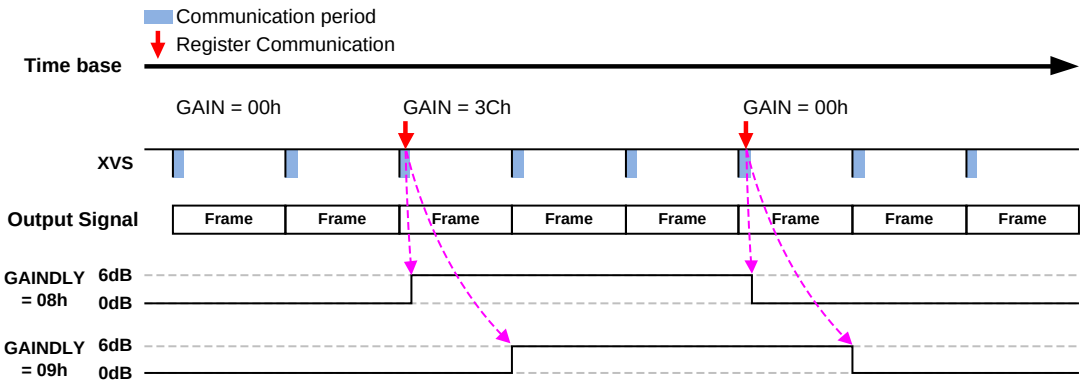
6 × 10 = 60d, GAIN = 03Ch



Register List of Gain setting

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address ( ) : I^2C	bit		Setting range	
GAIN [8:0]	04h	04h (3204h)	[7:0]	000h	000h to 1E0h (0d to 480d)	Setting value: Gain [dB] × 10
		05h (3205h)	[0]			

Gain Reflection Timing is changed by the set value of GAINDLY as shown below.



Gain Reflection Timing

Black Level Adjustment Function

The black level offset (offset variable range: 000h to 1FFh) can be added relative to the data in which the digital gain modulation was performed by the BLKLEVEL [11:0] register. When the BLKLEVEL [11:0] setting is increased by 1 LSB, the black level is increased by 1 LSB.

* Use with values shown below is recommended.
  10 bit output: 03Ch (60 d)

Register List of Black level adjustment

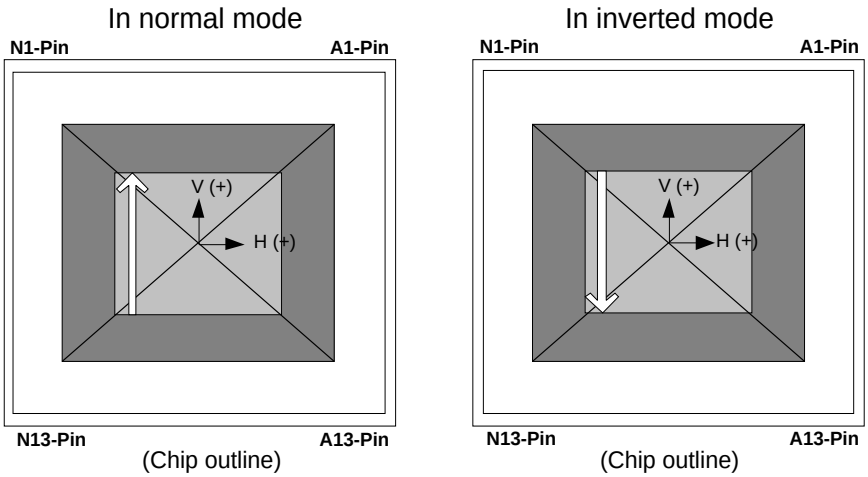
Register	Register details			Initial value	Setting value
	Chip ID	Address ( ) : I^2C	bit		
BLKLEVEL [11:0]	04h	54h (3254h)	[7:0]	03Ch	000h to FFFh
		55h (3255h)	[3:0]		

Horizontal / Vertical Normal Operation and Inverted Operation

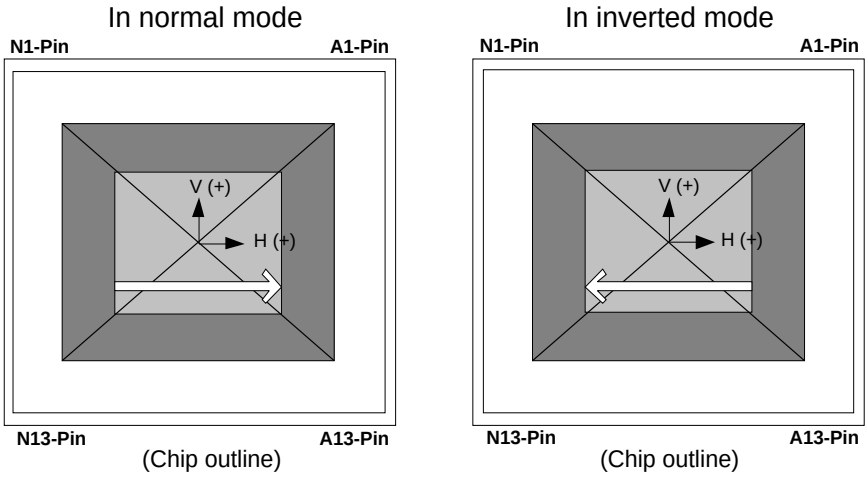
The sensor readout direction (normal / inverted) in vertical direction can be switched by the VREVERSE register setting and sensor readout direction (normal / inverted) in horizontal direction can be switched by the HREVERSE register setting. See the section of “Readout Drive Modes” for the order of readout lines in normal and inverted modes.

Register List of Readout Drive Direction setting

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ) : I^2C	bit		
VREVERSE	02h	0Eh (300Eh)	[0]	0h	0h: Normal (Initial value) 1h: Inverted
HREVERSE			[1]	0h	0h: Normal (Initial value) 1h: Inverted



Normal and Inverted Drive Outline in Vertical Direction (TOP VIEW)



Normal and Inverted Drive Outline in Horizontal Direction (TOP VIEW)

Shutter and Integration Time Settings

This sensor has a global shutter function that integrates to all line collectively by using memory in each pixel.
This sensor has a variable electronic shutter function that can control the integration time in line units for adjust the exposure time. This sensor transferred signal to memory in pixel after the exposure (memory transfer), then this sensor performs output in which readout operation is performed sequentially for each line in sync with the XHS signal.
This sensor has trigger mode that can be controlled exposure start timing and memory transfer timing by trigger.

Note) For integration time control, an image which reflects the setting is output from the frame after the setting changes.

In this item, the shutter operation and storage time are shown as in the figure below with the time sequence on the horizontal axis and the vertical address on the vertical axis. For simplification, shutter and readout operation are noted in line units.

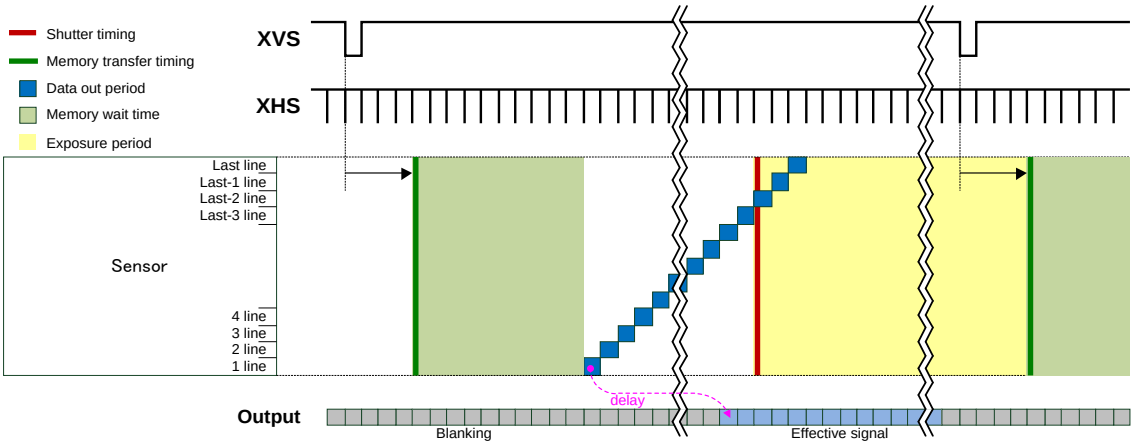


Image Drawing of Global Shutter (Normal mode) Operation

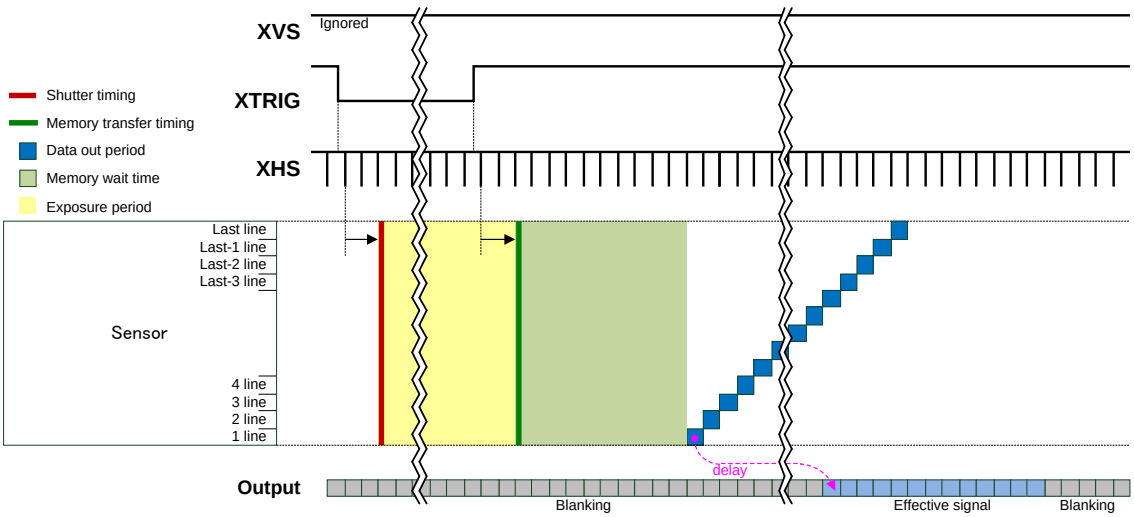


Image Drawing of Global Shutter (Sequential Trigger mode) Operation

Global Shutter (Normal Mode) Operation

The integration time can be controlled by varying the electronic shutter timing. In the electronic shutter settings, the integration time is controlled by the SHS [19:0] register. For setting value of SHS [19:0], see the table “List of Exposure Setting”. When the sensor is operating in slave mode, the number of lines per frame is determined by the XVS interval (number of lines), using the input XHS interval as the line unit. When the sensor is operating in master mode, the number of lines per frame is determined by the VMAX [19:0] register. The number of lines per frame differs according to the operating mode.

Calculation Formula of Exposure Time

Exposure time [s] = (1 H period) × (Number of lines per frame - SHS) + 14.26 [μs][*1]

[*1]: Exposure time error (t_{OFFSET})

Register List of Shutter setting

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ) : I^2C	bit		
VMAX [19:0]	02h	10h (3010h)	[7:0]	0046Ah	Set the number of lines per frame (only in master mode)
		11h (3011h)	[7:0]		
		12h (3012h)	[3:0]		
SHS [19:0]		8Dh (308Dh)	[7:0]	0000Eh	Sets the shutter sweep time. memory wait time to (Number of lines per frame - 1)
		8Eh (308Eh)	[7:0]		
		8Fh (308Fh)	[3:0]		

List of Exposure Setting

Drive mode	memory wait time [H]	Number of lines per frame [DEC]	SHS Setting value [DEC]	Exposure Setting value [H]	MIPI 1 Lane / Maximum frame rate	
					Frame rate [frame/s]	Actually exposure [ms][*4]
					RAW10	RAW10
All-pixel	4	1118	1117	1	60.3	0.029
			1116	2		0.044
			…	…		…
			5	1113		16.503
			4	1114		16.518
ROI	4	V_{TR}[*1]	V_{TR}-1	1	[*2]	0.029
			V_{TR}-2	2		0.044
			…	…		…
			5	V_{TR}-5		[*3]
			4	V_{TR}-4		

[*1] V_{TR} = ROIWV1 + 30
[*2] For the frame rate, see the section “ROI mode” in “Readout Drive Mode”.
[*3] Conform to the calculation formula of exposure time. (Number of lines per frame = V_{TR})
[*4] INCK frequency is input by typical value, and t_{OFFSET} (14.26 [µs]) is included.

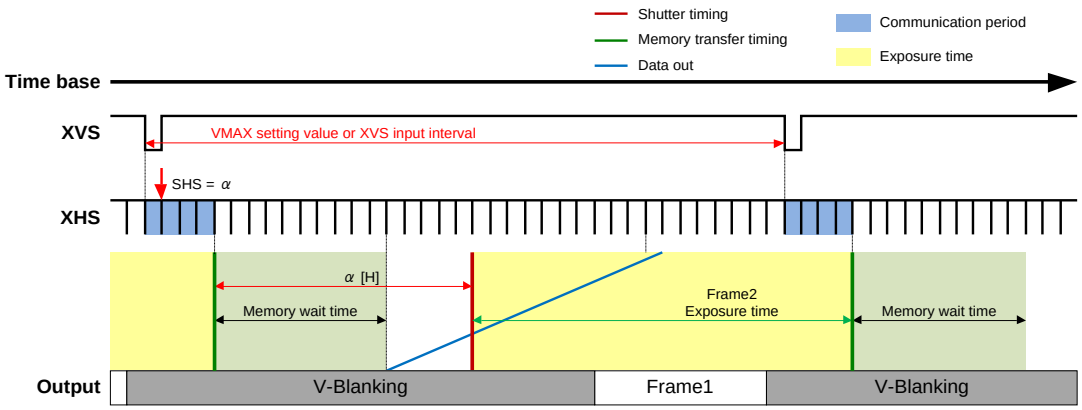


Image Drawing of Global Shutter (Normal Mode)

Global Shutter (Sequential Trigger Mode) Operation

The integration time can be controlled by varying the pulse width that is input to XTRIG pin. The pulse width designated in XHS unit [H]. For the transition from normal mode to trigger mode, set 1 to the register TRIGEN. The XVS input signal is ignored during trigger mode operating. In case of inputting trigger continuously, there are period which prohibit the trigger rise input (t_{TGPD}) and fall input (t_{TGES}) based on the previous trigger rise. When the trigger rise is input before the rise input prohibited period (t_{TGPD}), interrupt operation starts. This function is slave mode only. The number of lines per frame differs according to the operating mode.

Calculation Formula of Exposure Time

Exposure time [s] = (XTRIG low level pulse width [H][*2]) + 14.26 [µs][*1]

[*1]: Exposure time error (t_{OFFSET})

[*2]: Low level pulse width is counted by XHS pulse.

Register List of shutter setting

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ) : I^2C	bit		
XMSTA	02h	0Ah (300Ah)	[0]	1h	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop
TRIGEN	02h	0Bh (300Bh)	[0]	0h	0h: Global shutter (normal mode) 1h: Global shutter (trigger mode)
VINT_EN	02h	AAh (30AAh)	[0]	1h	Setting of Interrupt mode in Trigger Mode 0: V interrupt is disable 1: V interrupt is enable

Parameter List of Global Shutter (Sequential Trigger Mode)

Item	Symbol	Min.	Typ.	Max.	Unit
Integration start delay	t_{TGST}	2	—	3	H
Integration end delay	t_{TGED}	2 + t_{OFFSET}	—	3 + t_{OFFSET}	H
Pulse width	t_{TGSE}	1	—	—	H
Next trigger fall prohibited period (All-pixel, ROI)	t_{TGES}	7	—	—	H
Next trigger rise prohibited period (All-pixel)	t_{TGPD}	1118	—	—	H
Next trigger rise prohibited period (ROI)		V_{TR}[*1]	—	—	
Data output delay (All-pixel / ROI)	t_{TGDLY}	—	15	—	H

[*1] V_{TR} = ROIWV1 + 30

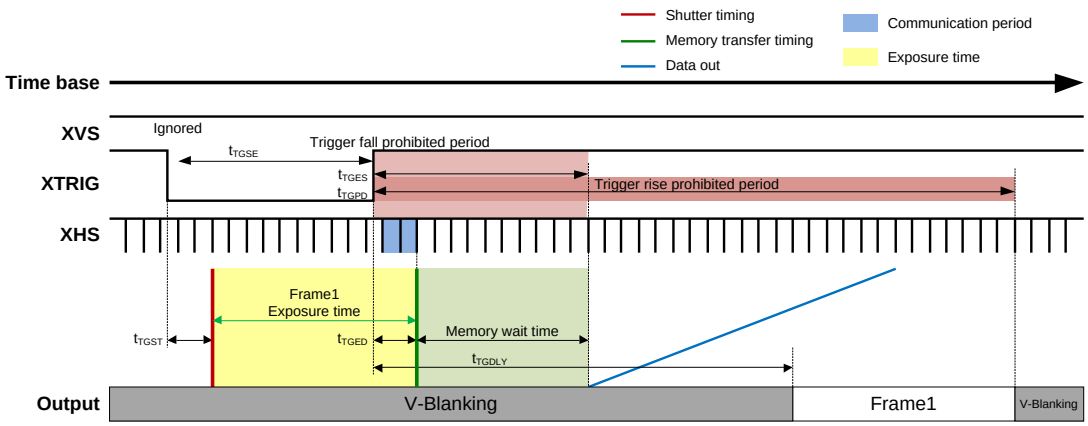


Image Drawing of Global Shutter (Sequential Trigger Mode)

Interrupt Operation

In case of VINT_EN = 1h, the image drawing when the interrupt operation is generated is shown below. When the trigger is raised again and the next frame is output during read of the frame for which read was started by a trigger rise (Frame 1 in the figure below), Frame 1 becomes an invalid frame. Trigger timing of interrupt generating corresponds to t_{TGPD} in Parameter List of Global Shutter (Trigger Mode)
In case of VINT_EN = 0h, both of the rising edge and the falling edge of the trigger signal are ignored in t_{TGPD} (Prohibit period).

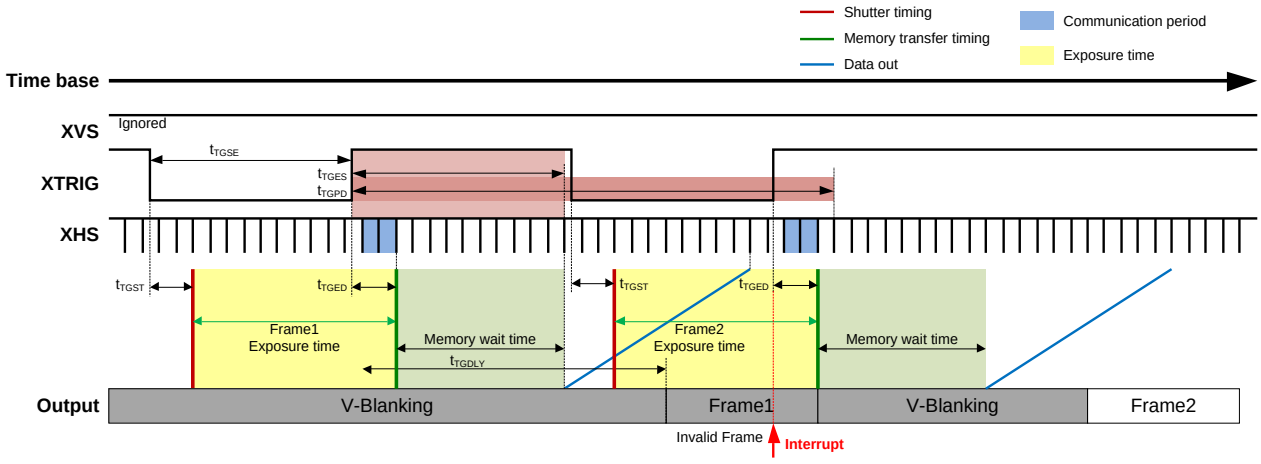


Image Drawing of Interrupt Operation in Global Shutter (Sequential Trigger Mode)

Global Shutter (Fast Trigger Mode) Operation

Fast trigger mode is the trigger mode that starts exposure at fall of XTRIG immediately.
This mode supports Master mode only.

Calculation Formula of Exposure Time

Exposure time [s] = (XTRIG low level pulse width [µs]) + 14.26 [µs][*1]
[*1]: Exposure time error (t_{OFFSET})

Register List of shutter setting

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ) : I^2C	bit		
XMSTA	02h	0Ah (300Ah)	[0]	1h	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop
TRIGEN		0Bh (300Bh)	[0]	0h	0h: Global shutter (normal mode) 1h: Global shutter (trigger mode)
SYNCSEL		36h (3036h)	[5:4]	0h	XHS, XVS pin setting 0h: Normal Output 3h: Hi-Z
LOWLAGTRG		AEh (30AEh)	[0]	0h	Selection of trigger mode 0: Except for Fast trigger mode 1: Fast trigger mode

Parameter List of Global Shutter (Fast Trigger Mode)

Item	Symbol	Min.	Typ.	Max.	Unit
Integration start delay	t_{TGST}	—	—	0.05	µs
Integration end delay	t_{TGED}	—	—	0.05 + t_{OFFSET}	µs
Pulse width	t_{TGSE}	0.05	—	—	µs
Next trigger rise / fall prohibited period (All-pixel)	t_{TGPD}	1126	—	—	H
Next trigger rise / fall prohibited period (ROI)		V_{TR}[*1] + 8	—	—	
Data output delay (All-pixel / ROI)	t_{TGDLY}	—	15	—	H

[*1] V_{TR} = ROIWV1 + 30

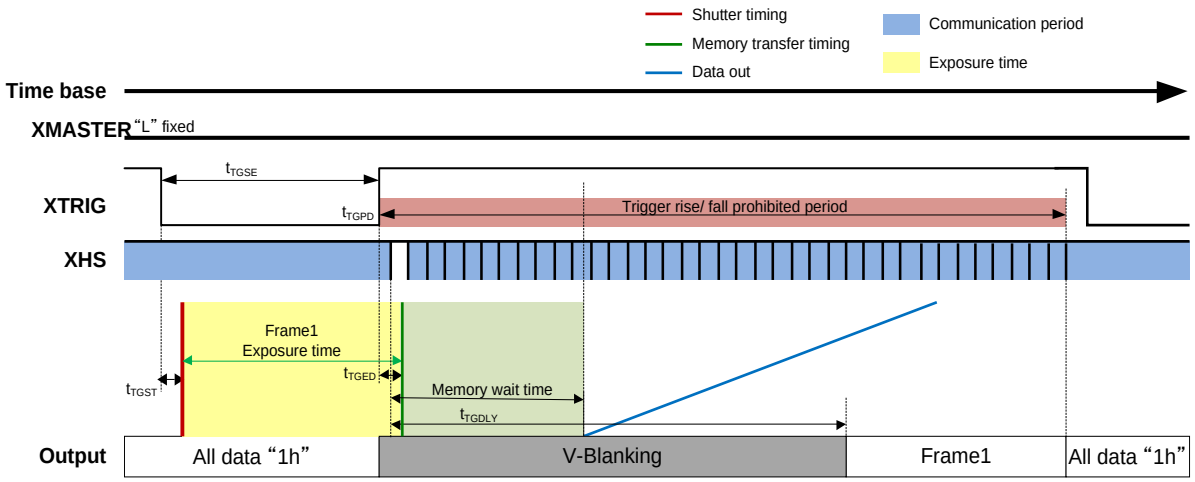


Image Drawing of Global Shutter (Fast Trigger Mode) (4-wire)

Mode Transitions of Global Shutter Operation

The sensor can be switched between normal mode and trigger mode in global shutter operation by setting the register TRIGEN. The sensor will transition to normal mode or trigger mode 4H after the register TRIGEN is set. (The XVS and XTRIG input during transition are prohibited.)
In case of Fast Trigger mode, the mode transition must be done via sensor standby.

Transition from Normal Mode to Sequential Trigger Mode

The sensor will transition from normal mode to trigger mode after setting 1d to register TRIGEN. The XVS input is ignored after transition to trigger mode. Trigger input is prohibited for a 4H period after the register TRIGEN is set. When TRIGEN is set during data read, read operation is stopped and that frame becomes an invalid frame.

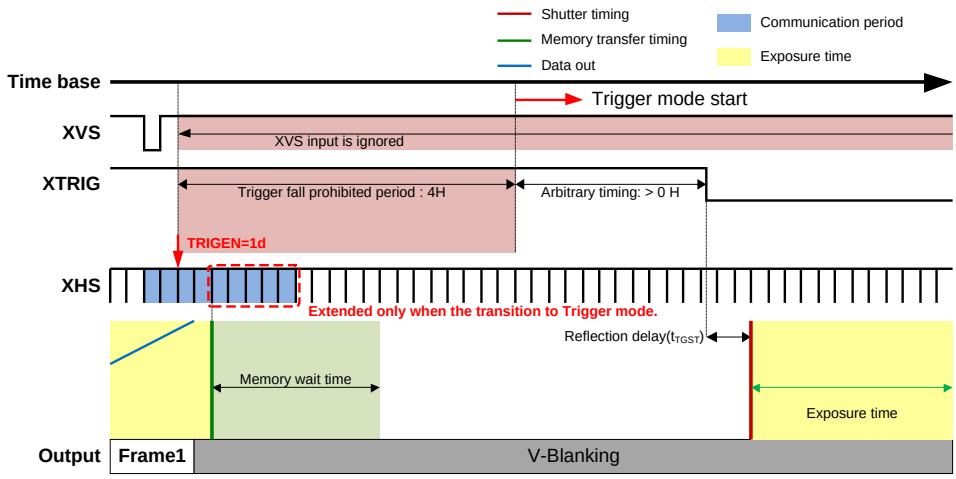


Image Drawing of Transition from Normal Mode to Sequential Trigger Mode

Transition from Sequential Trigger Mode to Normal Mode

The sensor will transition from trigger mode to normal mode after setting 0d to register TRIGEN. Start XVS input after transition to normal mode. Set TRIGEN after Next trigger rise prohibited period (t_{TGPD}) has passed. When TRIGEN is set before t_{TGPD}, read operation is stopped and that frame becomes an invalid frame.

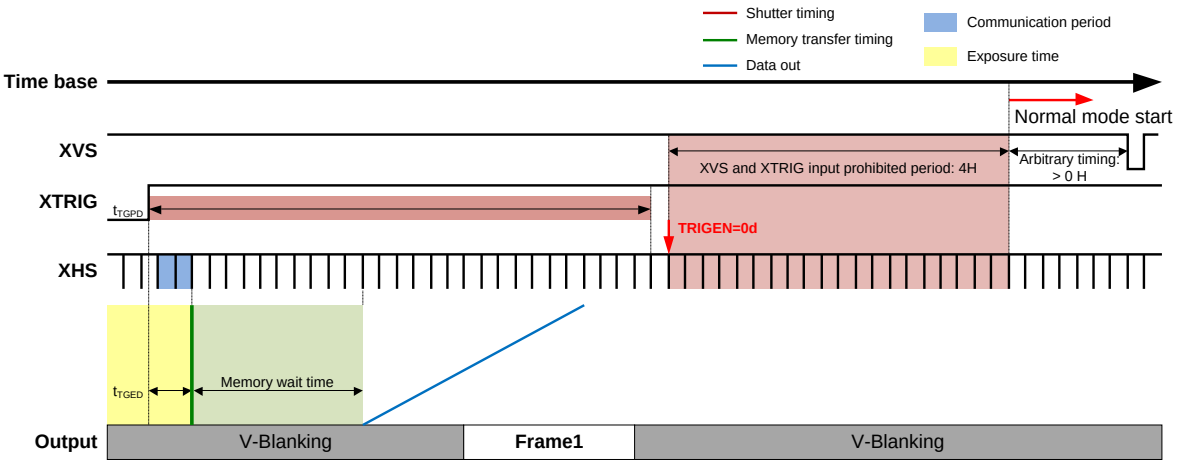


Image Drawing of Transition from Sequential Trigger Mode to Normal Mode

Pulse Output Function

This sensor has a pulse output function that indicates each state of shutter operation. The pulse output from TOUT1 pin and TOUT2 pin. The rise timing and fall timing of pulse are set by Register. For the reference point (The timing when register value set to 0) to be set, see the table “List of Reference point". The pulse is output asynchronously with other signals on the basis of the sensor internal timing shown in the “List of Reference point". This function doesn't support Fast Trigger mode.

Register List of Pulse Output Function

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ) : I^2C	bit		
TOUT1SEL [1:0]	02h	26h (3026h)	[1:0]	0h	TOUT1 pin setting 0h: Low fixed 3h: Pulse output
TOUT2SEL [1:0]			[3:2]	0h	TOUT2 pin setting 0h: Low fixed 3h: Pulse output
TRIG_TOUT1_SEL [2:0]		29h (3029h)	[2:0]	0h	TOUT1 pin output selection 0h: Low fixed 1h: Pulse1 output
TRIG_TOUT2_SEL [2:0]			[6:4]	0h	TOUT2 pin output selection 0h: Low fixed 2h: Pulse2 output
PULSE1_EN_NOR		6Dh (306Dh)	[0]	0	Pulse1 enable in normal mode 0: disable 1: enable
PULSE1_EN_TRIG			[1]	0	Pulse1 enable in trigger mode 0: disable 1: enable
PULSE1_POL			[2]	0	Pulse1 polarity selection 0: High active 1: Low active
PULSE1_UP [19:0]		70h (3070h)	[7:0]	00000h	Pulse1 active period start timing setting Designated in line units from reference point
		71h (3071h)	[7:0]		
		72h (3072h)	[3:0]		
PULSE1_DN [19:0]		74h (3074h)	[7:0]	00000h	Pulse1 active period end timing setting Designated in line units from reference point
		75h (3075h)	[7:0]		
		76h (3076h)	[3:0]		
PULSE2_EN_NOR		79h (3079h)	[0]	0	Pulse2 enable in normal mode 0: disable 1: enable
PULSE2_EN_TRIG			[1]	0	Pulse2 enable in trigger mode 0: disable 1: enable
PULSE2_POL			[2]	0	Pulse2 polarity selection 0: High active 1: Low active
			[3]	0	Fixed to 1
PULSE2_UP [19:0]		7Ch (307Ch)	[7:0]	00000h	Pulse2 active period start timing setting Designated in line units from reference point
		7Dh (307Dh)	[7:0]		
		7Eh (307Eh)	[3:0]		
PULSE2_DN [19:0]		80h (3080h)	[7:0]	00000h	Pulse2 active period end timing setting Designated in line units from reference point
		81h (3081h)	[7:0]		
		82h (3082h)	[3:0]		

List of Reference Point

	Normal mode	Trigger mode
Reference point of Pulse1	XVS fall edge in N frame	Fall edge of input trigger
Reference point of Pulse2	XVS fall edge in N +1 frame	Rise edge of input trigger

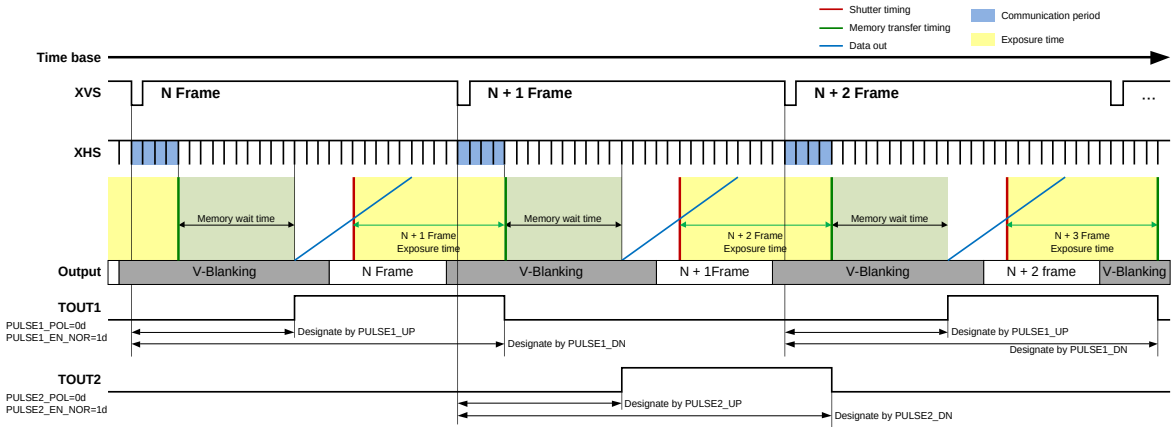


Image Drawing of Pulse Output Function in Global Shutter (Normal Mode)

In normal mode, TOUT1 and TOUT2 are output alternately each time inputting XVS.

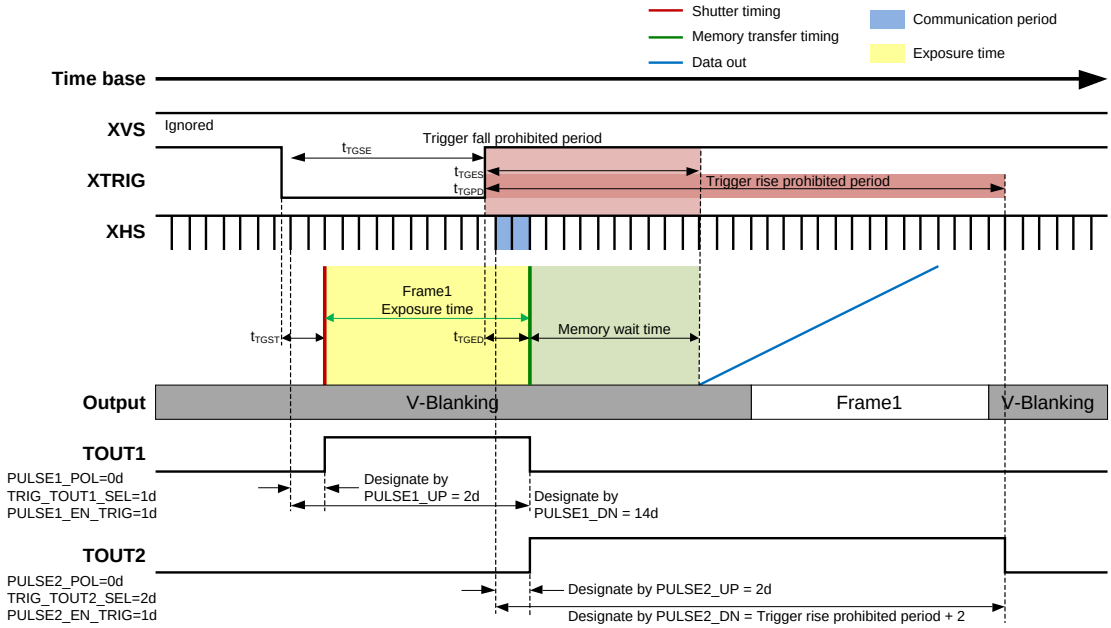


Image Drawing of Pulse Output Function in Global Shutter (Sequential Trigger Mode)

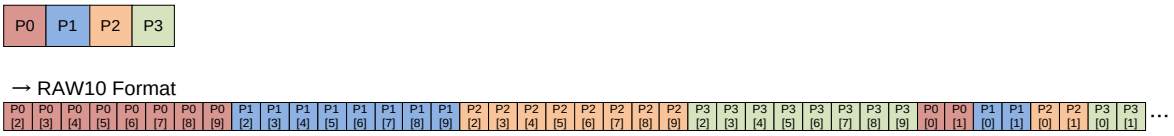
Signal Output
CSI-2 output

The output formats of this sensor support the following modes.

CSI-2 serial 1 Lane, RAW10 (NO COMPRESS)

The 1 Lane serial signal output method using this sensor is described below.
Complied with the CSI-2, data is output using 1 Lane. The image data is output from the CSI-2 output pin.
The DMOP/DMON are called the Lane1 data signal, the clock signals are output from DMCKP/DMCKM of the CSI-2 pins.The bit rate is 1188 Mbps / Lane.

The format of RAW10 is shown below.



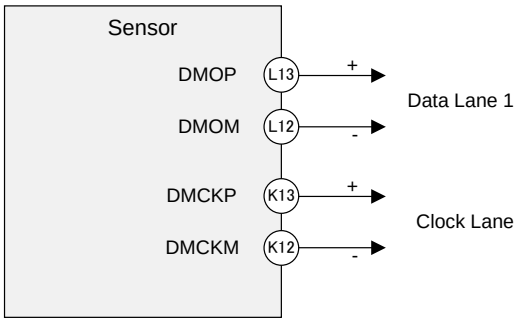
The Example of Format of RAW10

The format of 1 Lane is shown below.

1 Lane Output Format

MIPI Transmitter

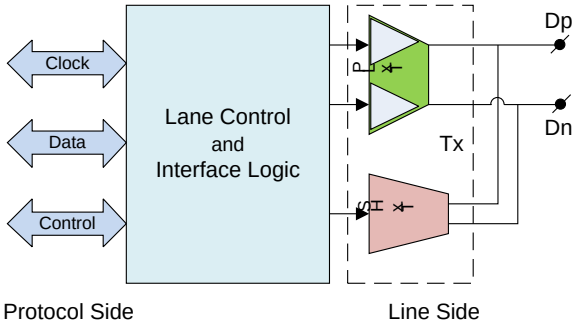
Output pins (DMOP, DMOM, DMCKP, DMCKM) are described in this section.



Relationship between Pin Name and MIPI Output Lane

The pixel signals are output by the CSI-2 High-speed serial interface.
See the MIPI Standard
・MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.10.00
・MIPI Alliance Specification for D-PHY Version 1.10.00

The CSI-2 transfers one bit with a pair of differential signals. The transmitter outputs differential current signal after converting pixel signals to it. Insert external resistance in differential pair in a series or use cells with a built-in resistance on the Receiver side. When inserting an external resistor, as close as possible to the Receiver. The differential signals maintain a constant interval and reach the receiver with the shortest wiring length possible to avoid malfunction. The bit rate of Lane is 1188 Mbps / Lane.



Universal Lane Module Functions

MIPI Global Timing setting

Internal calculation is performed according to setting value of GTTABLENUM to decide the best MIPI Global Timing which also meets MIPI Alliance Specification for D-PHY version 1.10.00 requirements.

Register	Register detail			Initial value	Setting value	Bit rate (MHz)	
	Chip ID	Address ( ) : I^2C	bit			Upper limit(≤)	Lower limit (>)
GTTABLENUM	13h	14h (4114h)	[5:0]	05h	05h	1198	1122

This sensor supports default setting only.

Output Signal Range

The sensor output has a 10-bit gradation, the output range is shown in the value of the table below.

Output Gradation and Output Range

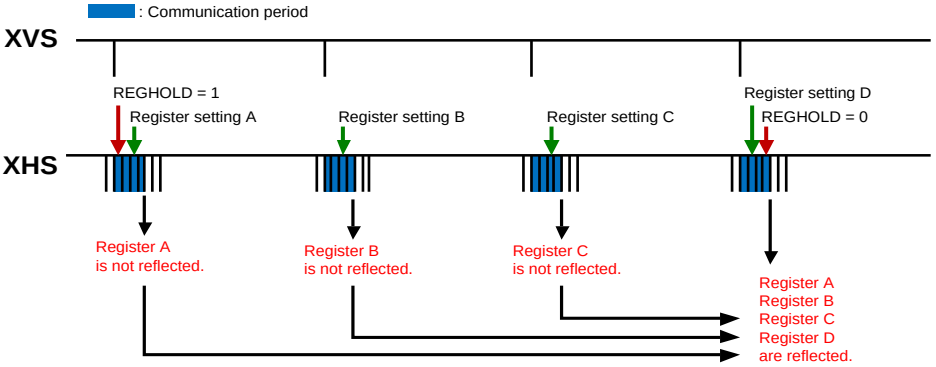
Output gradation	Output value	
	Min.	Max.
10 bit	000h	3FFh

Register Hold Setting

Register setting can be transmitted with divided to several frames and it can be reflected globally at a certain frame by the register REGHOLD. Setting REGHOLD = 1 at the start of register communication period prevents the registers that are set thereafter from reflecting at the frame reflection timing. The registers that are set when setting REGHOLD = 1 are reflected globally by setting REGHOLD = 0 at the end of communication period of the desired frame to reflect the register.

Register List of Register Hold

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ) : I^2C	bit		
REGHOLD	02h	08h (3008h)	[0]	0h	0h: Invalid 1h: Valid (Register hold)



Register Hold Setting

Mode Transition

The Mode transition between operations is shown below. These examples shown in case that setting is completed within one communication timing.

List of Mode Transition

Transition			State
ROI	→	All-pixel	Via the Standby state is unnecessary
All-pixel	→	ROI	
- Transition between modes other than the above - Change the input frequency of INCK [*1] - Change the register setting noted “S” in the reflection timing column of the Register Map.			Via the standby state is necessary

[*1] When changing input INCK frequency, care should be taken not to be input pulses whose width are shorter than the High / Low level width in front and behind of the INCK pulse at the frequency change. If the pulses above generate at the frequency change, change INCK frequency during system reset in the state of XCLR = Low, and then perform system clear in the state of XCLR = High following the item of "Power on sequence" in the section of "Power on / off sequence". Execute initial setting again because the register settings become default state after system clear.

Other Function

This sensor has the function as below. About detail, refer to each application note.

- Multi Frame Set Output mode (2 / 4 frame)
- Multi Exposure Trigger mode
- Driving Low Power Consumption at longtime exposure
- Simple Thermometer
- Pattern Generator (Refer to Support Package)
- Additional Function of Synchronizing Sensors

Extension Function

Use these function after enough checks and evaluation.

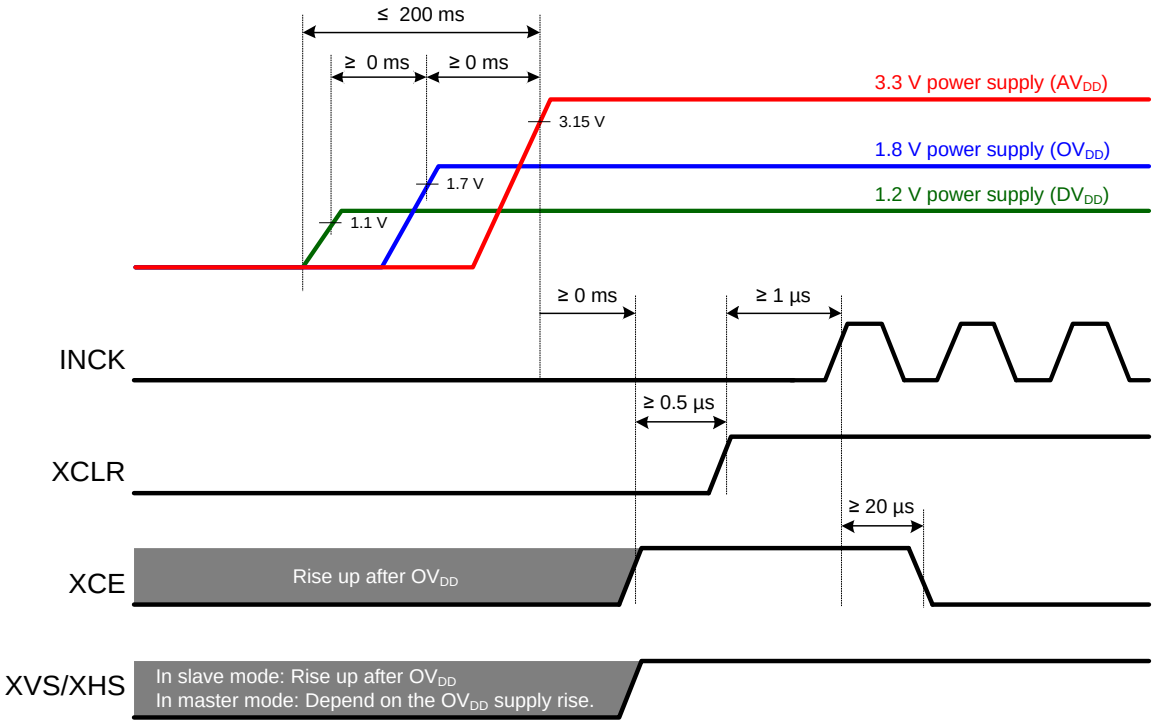
- Black Level Auto Adjust Off
- Short Exposure Mode

Power-on and Power-off Sequence

Power-on sequence

Follow the sequence below to turn On the power supplies.

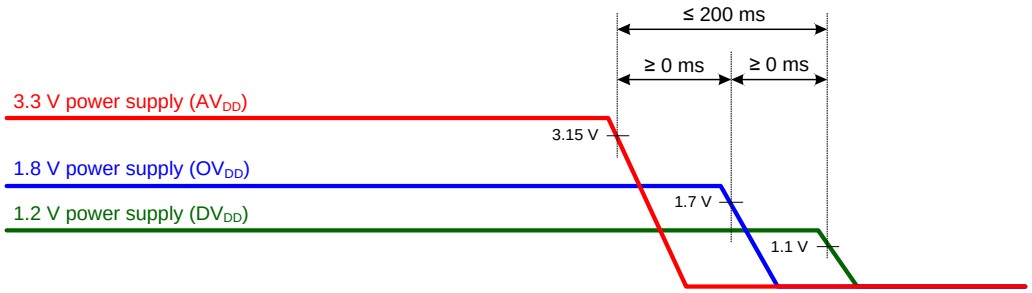
1. Turn On the power supplies so that the power supplies rise in order of 1.2 V power supply (DV_{DD}) →1.8 V power supply (OV_{DD}) → 3.3 V power supply (AV_{DD}). In addition, all power supplies should finish rising within 200 ms.
2. The register values are undefined immediately after power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.)
   In addition, hold XCE to High level during this period. Rise XCE after 1.8 V power supply (OV_{DD}), so hold XCE at High level until INCK is input.
3. Start the input of INCK after turning the level of XCLR into the high.
4. Make the sensor setting by register communication after the system clear. A period of 0 µs or more should be provided after setting XCLR High before inputting the communication enable signal XCE.



Power-on Sequence

Power-off Sequence

Turn Off the power supplies so that the power supplies fall in order of 3.3 V power supply (AV_{DD}) → 1.8 V power supply (OV_{DD}) → 1.2 V power supply (DV_{DD}). In addition, all power supplies should finish falling within 200 ms. Set each digital input pin (INCK, XCE, SCK, SDI, XCLR, XMASTER, XTRIG, SLAMODE, XVS, XHS) to 0 V or high impedance before the 1.8 V power supply (OV_{DD}) falls.

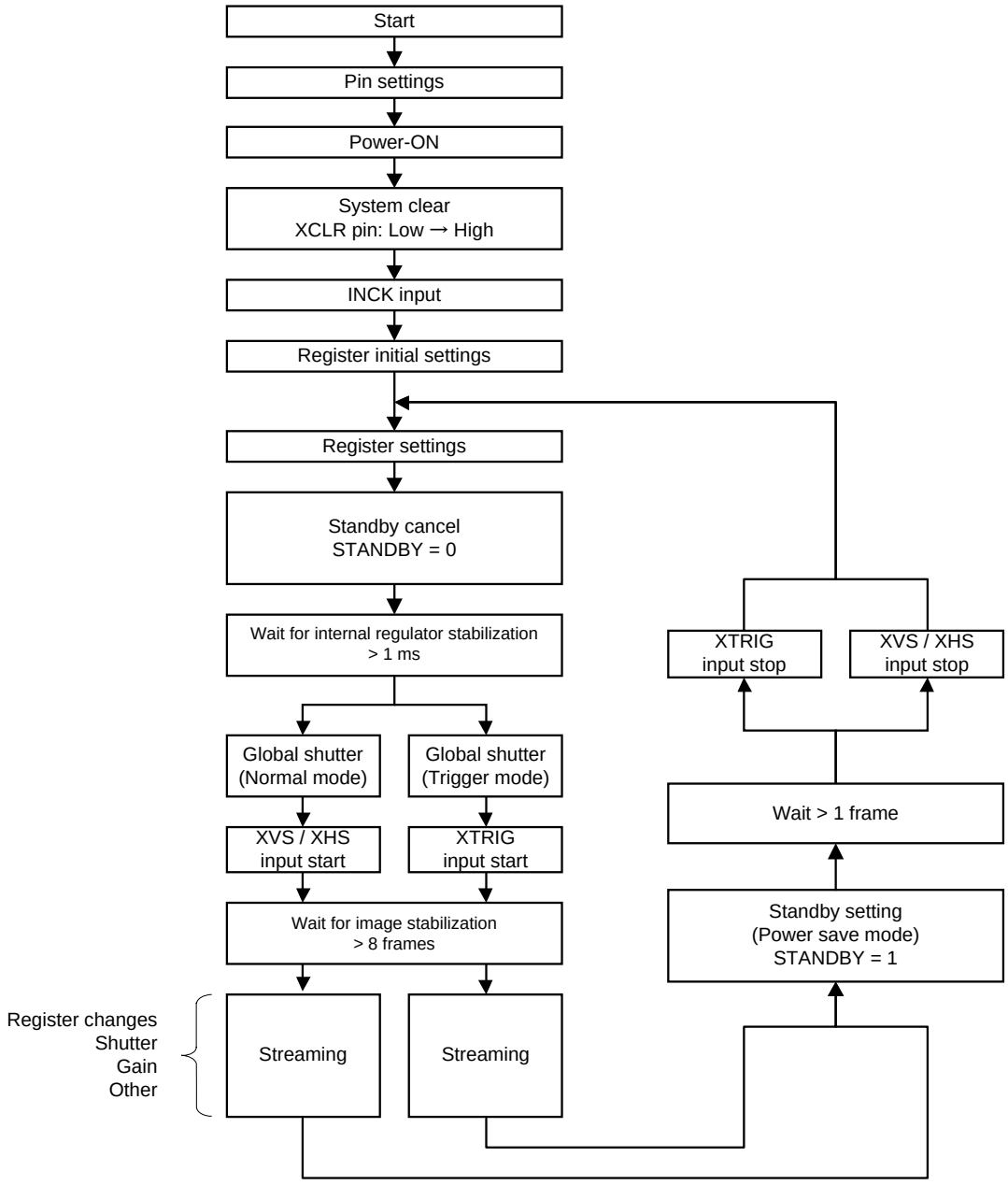


Power-off Sequence

Sensor Setting Flow

Setting Flow in Sensor Slave Mode

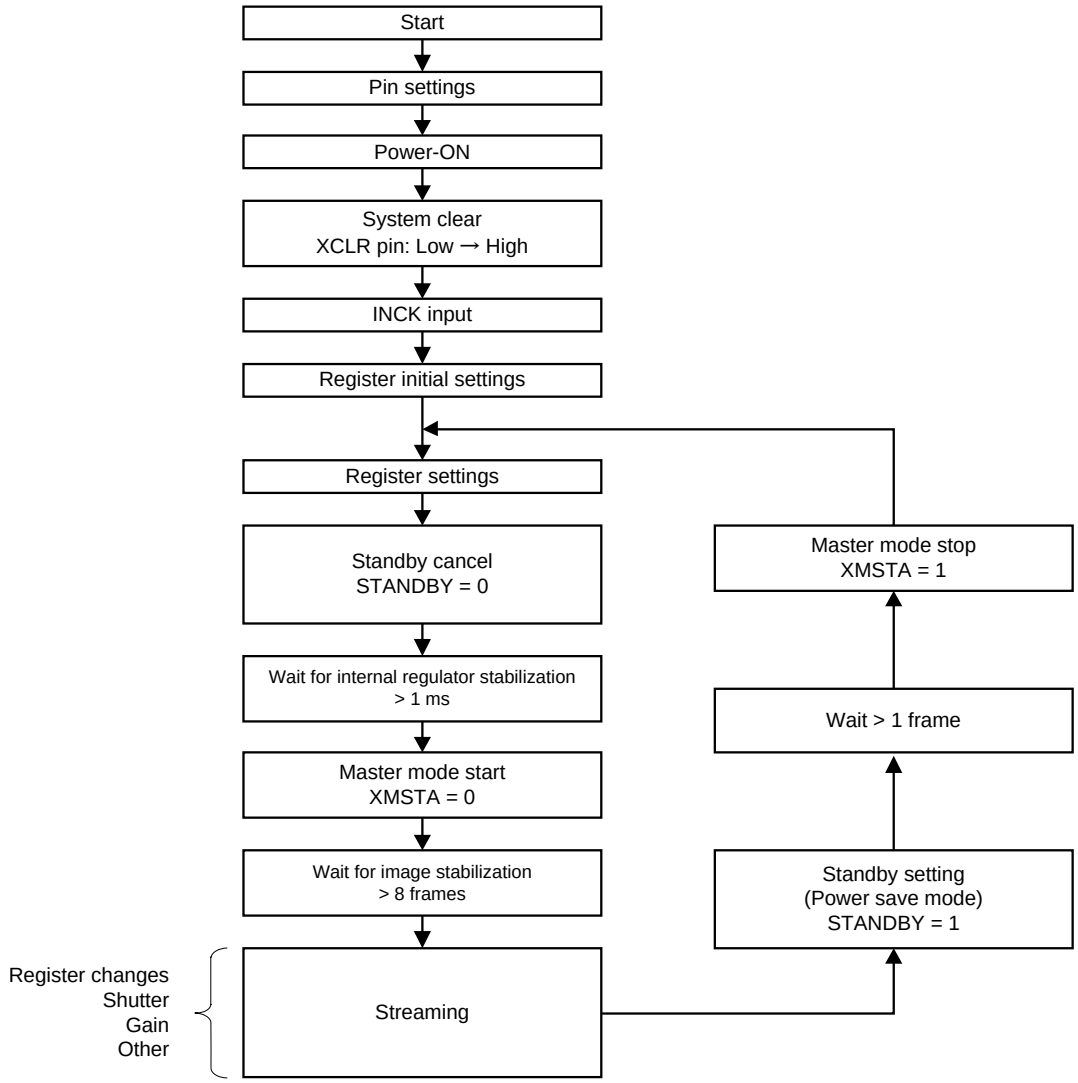
The figure below shows operating flow in sensor slave mode.
For details of "Power on" to "System clear", see the item of "Power on sequence" in this section. For details of "Standby cancel" to "Wait for image stabilization", see the item of "Standby mode". “Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”.



Sensor Setting Flow (Sensor Slave Mode)

Setting Flow in Sensor Master Mode

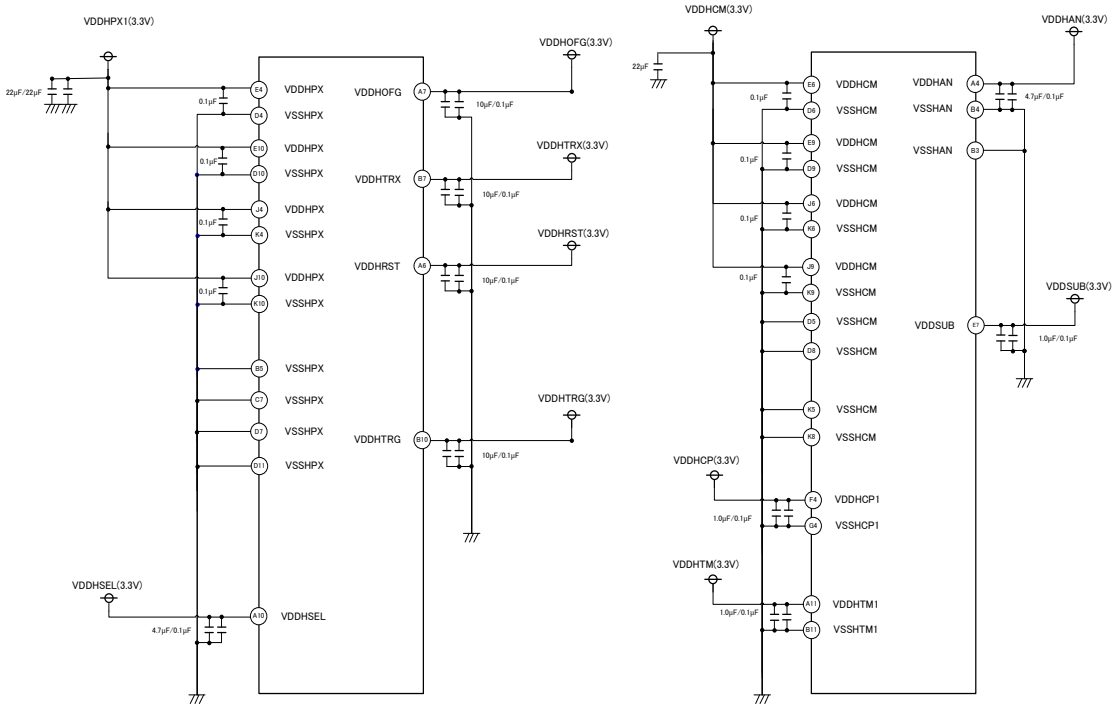
The figure below shows operating flow in sensor master mode.
For details of "Power on" to "System clear", see the item of "Power on sequence" in this section. For details of "Standby cancel" to "Wait for image stabilization", see the item of "Standby mode". In master mode, “Master mode start” by setting the master mode start register XMSTA to “0” after “Wait for internal regulator stabilization”.
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”. This time, set "master mode stop" by setting XMSTA to "1".



Sensor Setting Flow (Sensor Master Mode)

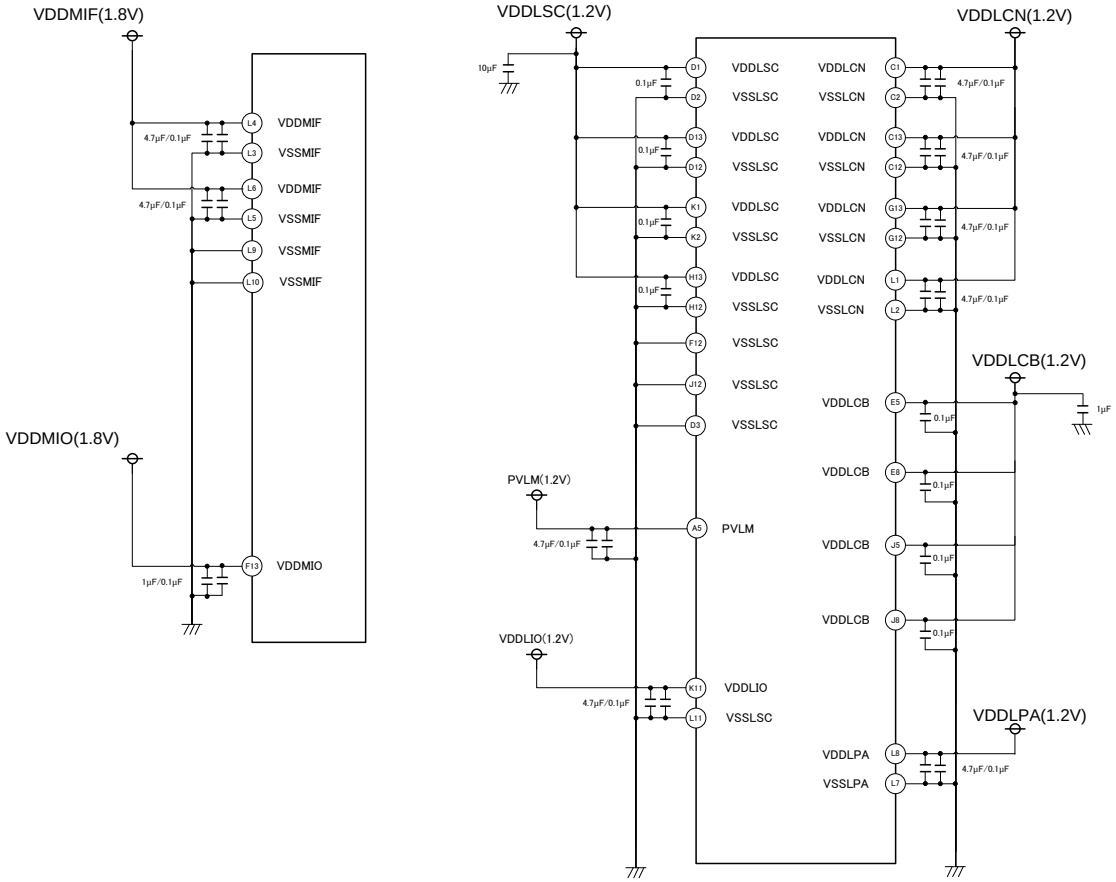
Peripheral Circuit

Analog Power Pins



Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

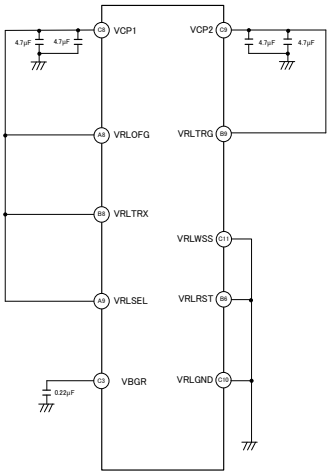
Digital Power Pins



Pin E5, E8, J5, and J8 are analog power pins. But these pins can be connected to the digital power pins. So, it describe on this page. These pins can be separated from the digital power pins.

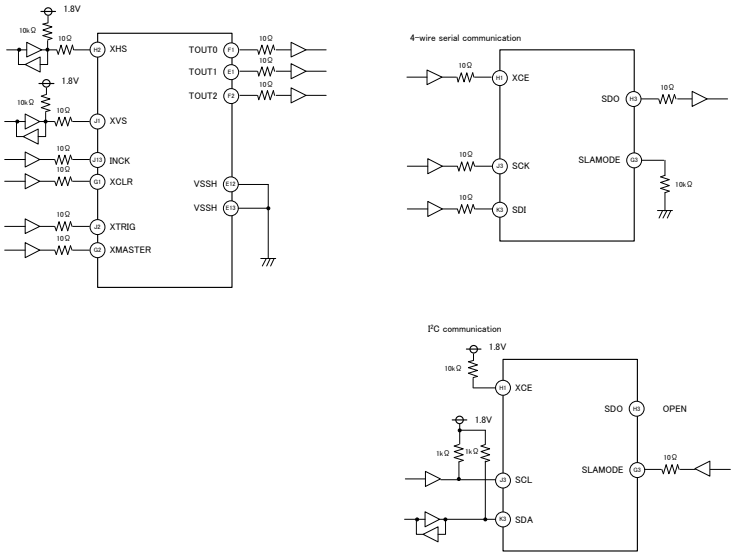
Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Analog Other Pins



Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

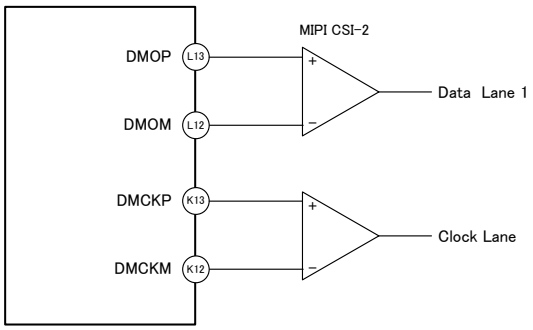
Digital I/O Pins



Pin E12, E13 are 3.3V GND. But, these pins are I/O terminal GND. So, these pins describe on this page.

Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Output pins



Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

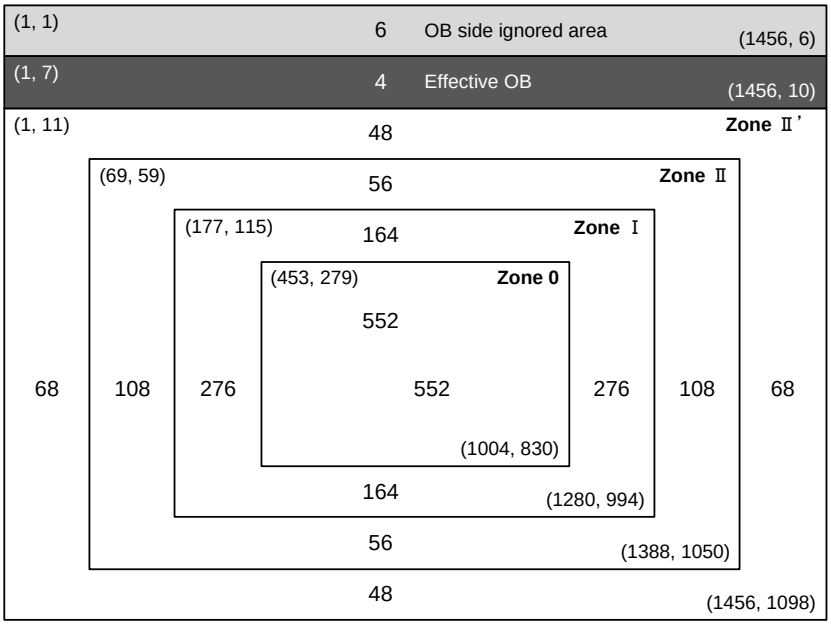
Spot Pixel Specifications

(Tj = 60 ˚C)

Type of distortion	Level	Maximum distorted pixels in each zone			Measurement method	Remarks
		0 to II'	Effective OB	Ineffective OB		
Black and white pixels at high light	30 % ≤ D	12	No evaluation criteria applied		1	
White pixels in the dark	5.6 mV ≤ D	137		No evaluation criteria applied	2	1/30 s storage
Black pixels at signal saturated	D ≤ 700 mV	0	No evaluation criteria applied		3	

Note) 1. Zone is specified based on all-pixel drive mode
2. D…Spot pixel level
3. See the Spot Pixel Pattern Specifications for the specifications in which pixel and black pixel are close.

Sport Pixel Zone Definition



Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, cosmic radiation may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".) Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Semiconductor Solutions Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Semiconductor Solutions Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
5.6 mV or higher	4 pcs
10.0 mV or higher	2 pcs
24.0 mV or higher	1 pcs
50.0 mV or higher	1 pcs
72.0 mV or higher	1 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

For Your Reference:

The annual number of White Pixels occurrence at an altitude of 3,000 meters is from 5 to 10 times more than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the annual number of White Pixels occurrence in such areas approximately doubles when compared with that in Tokyo.

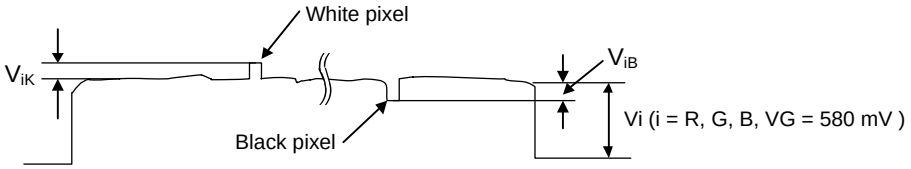
Material_No.03-0.0.9

Measurement Method for Spot Pixels

After setting to standard imaging condition II, and the device driver should be set to meet bias and clock voltage conditions. Configure the drive circuit according to the example and measure.

1. Black or white pixels at high light
   After adjusting the luminous intensity so that the average value VG of the Gb / Gr signal outputs is 580 mV, measure the local dip point (black pixel at high light, ViB) and peak point (white pixel at high light, ViK) in the Gr / Gb / R / B signal output Vi (i = Gr / Gb / R / B), and substitute the value into the following formula.

   Spot pixel level D = ((ViB or ViK) / Average value of Vi) × 100 [%]



Signal output waveform

2. White pixels in the dark
   Set the device to a dark setting and measure the local peak point of the signal output waveform, using the average value of the dark signal output as a reference.

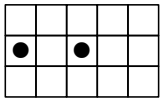
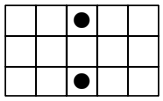
3. Black pixels at signal saturated
   Set the device to operate in saturation and measure the local dip point, using the OB output as a reference.

Signal output waveform

Spot Pixel Pattern Specification

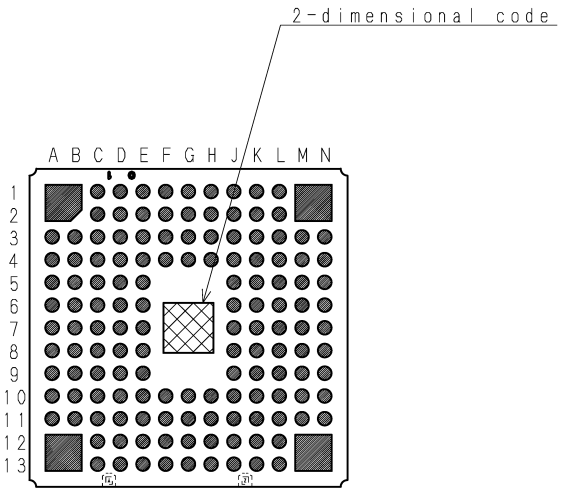
White Pixel, Black Pixel and Bright Pixel are judged from the pattern whether they are allowed or rejected, and counted.

List of White Pixel, Black Pixel and Bright Pixel Pattern

No.	Pattern	White pixel Black pixel Bright pixel
1		Rejected
2		Rejected

Note) 1. “●” shows the position of white pixel, black pixel and bright pixel.
White pixel, black pixel and bright pixel are specified separately according the pattern.
(Example: If a black pixel and a white pixel is in the pattern No.1 respectively, they are not judged to be rejected.)
2. When one or more spot pixels indicated “Rejected” is selected and removed.
3. Spot pixels other than described in the table above are all counted including the number of allowable spot pixels by zone.

Marking



Note:Following characters enter into "Y", and"Z". (No Au coat)
Y:In English upper case character, One character
Z:Number, single number

DRAWING No. AM-C296LQR(2D)

Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

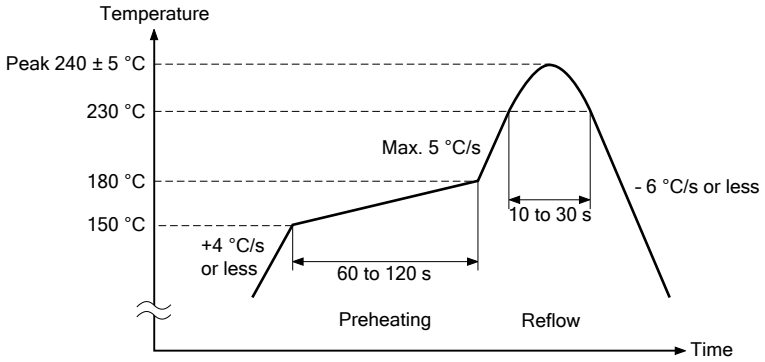
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (- 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.
(b) Perform the reflow soldering only one time.
(c) Finish reflow soldering within 72 h after unsealing the degassed packing.
Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.
(d) Perform re-baking only one time under the condition at 125 °C for 24 h.
(e) Note that condensation on glass or discoloration on resin interfaces may occur if the actual temperature and time exceed the conditions mentioned above.

(3) Others

(a) Carry out evaluation for the solder joint reliability in your company.
(b) After the reflow, the paste residue of protective tape may remain around the seal glass.
(The paste residue of protective tape should be ignored except remarkable one.)
(c) Note that X-ray inspection may damage characteristics of the sensor.

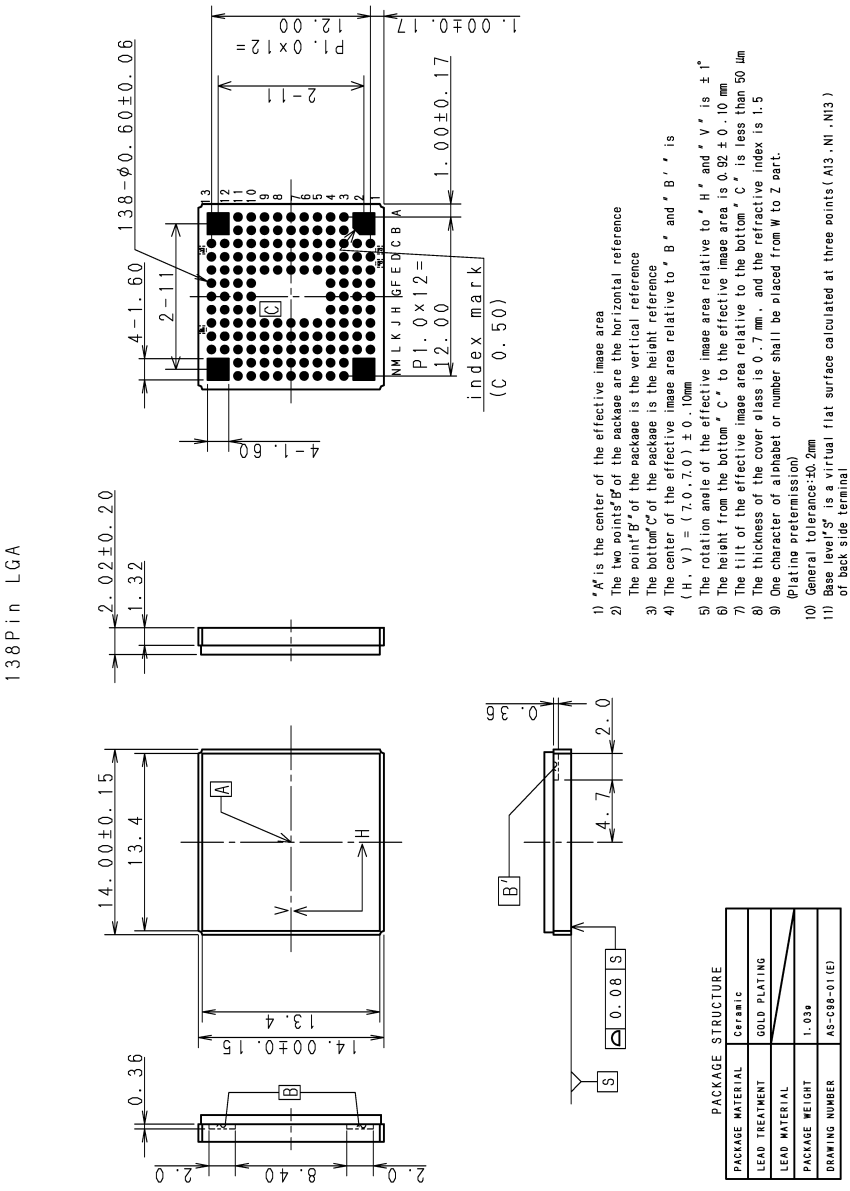
5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

Material_No.14-0.0.8

Package Outline

(Unit: mm)



List of Trademark Logos and Definition Statements

Pregius

* Pregius is a trademark of Sony Corporation. The Pregius is global shutter pixel technology for active pixel-type CMOS image sensors that use Sony's low-noise CCD structure, and realizes high picture quality.

SONY

Revision History

Date of change	Revision	Page	Contain of Change
28 - Aug. - 18	0.1	—	First edition
20 - Dec. - 18	E18Z06	10	Correction : D12 of Pin Configuration
		76, 77	Correction : Sensor Setting Flow
		87	Update : Marking
		90	Update : Package Outline