Crystal Image through Imaging Innovation

PIXELPLUS

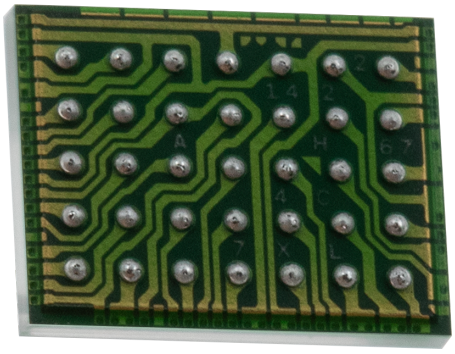
Datasheet

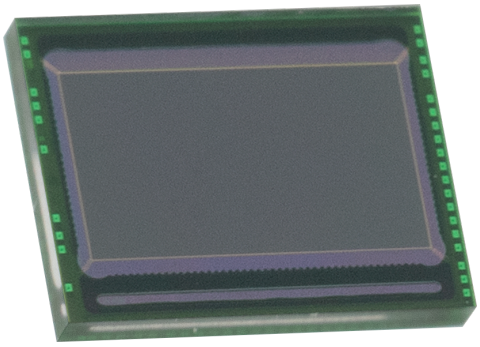
For the latest data sheet, please visit www.sunnywale.com

1/4 inch HD Single Chip

CMOS Image Sensor with HD-Analog Transmitter

PV4109K





Rev 0.5

Last update : 15. Oct. 2021

6th Floor, Gyeonggi R&DB Center, 906-5 Iui-dong, Yeongtong-gu,
Suwon-si, Gyeonggi-do, 443-766, Korea

Table of Contents

Features 7
General Description 8
Chip Architecture 9
Frame Structure 10
Pixel Data Format 11
Parallel Formatter 12
    Windowing 12
    Data control 13
    Vsync and Hsync 16
    PCLK 18
Digital Parallel Interface 19
Recommended Power Sequence 21
Clock 22
    PLL 22
    Clock Divider 23
    PLL and Clock Setting Sequence 24
Reset 25
Initialization 26
    Initialization Flow 26
    Required Time of Initialization 27
    Wire-strapping 27
    Internal ROM 27
    External ROM 28
        External ROM Structure 28
        I2C EEPROM 28
        Register Selector in Master Mode 29
External Communication Specification 30
    I2C Communication 30
        Register Update Timing 31
LED Control 32
Exposure Control 34
    Integration Time 34
    Global Gain 35
    Exposure factor update control 36
ISP(Image Signal Processing) 37
    Test Pattern (TP) Control 37
    Lens Shading Compensation (LSC) 39
    White Balance Gain 40
    Noise Reduction (NR) 41
    Edge Enhancement 41
    Color Correction (CCR) 42
    RGB Gamma 43
    De-color 44
    Y Gamma 45
    Contrast 46
    Y Offset 47
    Color Saturation 47
Flicker Detection 48

AE Window Setting 49
AE Auto/Manual Mode Control 50
AWB Window Setting 52
Parking Guide Line Control 53
PVI Encoder 57
Color Subcarrier Selection 57
Video Tunning 58
Video Timing Tunning 58
Electrical Characteristics 61
DC Characteristics 61
AC Characteristics 63
Register Map 64

List of Figures

1. Chip architecture 9
2. Default frame structure(top view) 10
3. Bayer color filter pattern 11
4. Mirror 11
5. Windowing 12
6. Parallel format timing 13
7. Parallel format 13
8. Parallel format header 14
9. Sync drop 16
10. Hsync all lines 16
11. Vsync polarity 17
12. Hsync polarity 17
13. PCLK polarity 18
14. Timing diagram of power-on/off sequence 21
15. Clock divider 22
16. Clock setting sequence 24
17. Soft reset 25
18. Initialization flow 26
19. External ROM structure 28
20. I2C functional description 31
21. LED control with CdS 32
22. Fundamental concept of integration time 34
23. Globalgain's gain 35
24. Test image 38
25. LSC center control 39
26. LSC gain fitting with LSC center and LSC scale 40
27. CCR matrix 42
28. Gamma curve fitting of RGB gamma 43
29. Gamma curve fitting of Y gamma 45
30. ISP_cont 46
31. Color saturation matrix 47
32. AE window setting 49
33. AWB window setting 52
34. Parking guide line 53
35. Timing diagram of SCL and SDA 63

List of Tables

1. Key Performance Parameter 8
2. Register Table - Frame structure 10
3. Register Table - Mirror 11
4. Register Table - Window 12
5. Register Table - Parallel format 14
6. Register Table - Data sequence 15
7. Register Table - Active data(data_cmlamp = enable) 15
8. Register Table - Data clamp 15
9. Register Table - Sync control 17
10. Register Table - PCLK control 18
11. Register Table - digital parallel interface 19
12. Recommended power-on/off sequence 21
13. Register Table - PLL 23
14. Register Table - Clock divider 23
15. Register Table - Soft reset 25
16. Setting mode according to wire-strapping 27
17. Mirror mode 27
18. Register Table - External ROM settings 28
19. Register Table - Register Selecter in Master mode 29
20. I2C update timing control 31
21. Register Table - LED control with CdS 32
22. Register Table - Integration time 34
23. Register Table - Global Gain 35
24. Register Table - Exposure register update 36
25. Register Table - Test pattern control 37
26. Register Table - LSC 40
27. Register Table - White balance gain 41
28. Register Table - NR 41
29. Register Table - Edge enhancement 42
30. Register Table - CCR 42
31. Register Table - RGB gamma 43
32. Register Table - De-color 44
33. Register Table - Y Gamma 45
34. Register Table - ISP Contrast 47
35. Register Table - Y offset 47
36. Register Table - Color saturation 47
37. Register Table - Flicker detection 48
38. Register Table - AE window setting 49
39. Register Table - AE manual 50
40. Register Table - AWB window setting 52
41. Register Table - Parking guide line 54
42. Register Table - Subcarrier register 57
43. Register Table - Subcarrier selection 57
44. Register Table - Video tunning 58
45. Register Table - PVI 59
46. DC characteristics 61
47. 2-wire serial interface characteristics 63
48. Register Table - Group A 64

49. Register Table - Group B 68
50. Register Table - Group D 69
51. Register Table - Group E 71
52. Register Table - Group F 73
53. Register Table - Group H 74
54. Register Table - Group I 75
55. Register Table - Group O 76
56. Register Table - Control register map 77

Features

- 1284x724 effective pixel array with RGB bayer color filters and micro-lens
- Output Interface
  - DVP(Digital Video Parallel) 8-bit
    - Raw RGB Bayer 8-bit
    - YCbCr422 8-bit
  - HD-Analog
- Auto black level compensation
- Programmable frame size, frame rate, window size, exposure and white balance gain
- Horizontal/Vertical mirroring
- Image processing on chip : lens shading compensation, gamma correction, defect correction, color correction, NR(2D noise reduction), color interpolation, edge enhancement, brightness, contrast, de-color, auto white balance, auto exposure control, back light compensation, Color saturation, Low light enhancement
- Automatic flicker cancellation
- Auto IR-LED/TDN(moving) filter controller with CdS
- Programmable static parking guideline
- Software reset
- On-chip phase locked loop (PLL)
- I2C master included
- Crystal input support

General Description

The PV4109K is a 1/4-inch CMOS image sensor with HD-Analog Transmitter. It is a single chip with an effective pixel array of 1284 (width) x 724 (height). The PV4109K can generate a PVI(HD-Analog) data at maximum frame rate of 30 FPS. On-chip sensor functions can be controlled through I2C interface.

Table 1 Key Performance Parameter

Parameter	Typical value
Pixel size	2.8 [um] x 2.8 [um]
Effective pixel array	1284(H) x 724(V)
Effective image area	3.5952 [mm] x 2.0272 [mm]
Optical format	1/4 [inch]
Input clock frequency	27 [MHz]
Output interface	DVP 8-bit
	HD-Analog
Max. frame rate	30 [FPS]
Dark signal	34.2 [e/sec]
Sensitivity	20.4K [e/lux*sec]
Power supply	HVDD : 3.3 [V]
	AVDD : 3.3 [V]
	RVDD : 3.3 [V]
	DVDD : 1.2 [V]
Power consumption	119.6 [mW] @ dynamic (DVP)
	163.8 [mW] @ dynamic (HD-Analog)
	383 [uW] @ standby
Operating temp. (Fully functional temp.)	-40~85 [°C] (Ambient)
Dynamic range	63.8 [dB]
SNR	43.1 [dB]
Package type	CSP

Chip Architecture

The PV4109K has a 1284 x 724 total pixel array and includes column/row driver circuits for reading out pixel data progressively. CDS circuit reduces noises generated from various sources, which mainly are resulted from process variations. The fixed error signal level caused by pixel process variation can be reduced by sampling the difference between the output and the reset level of the pixel. Each of R, G, and B pixel output can be multiplied by different gain factors to balance the color of images under various light conditions. The analog signals are converted into digital data of one line at a time and each line data is streamed out column by column. The Bayer RGB data passes through a sequence of image signal processing to produce various output datas. Image signal processing includes operations such as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. The PV4109K with PVI TX supports PVI(HD-Analog) analog output. The control of internal functions and output signal timings can be enabled by modifying registers directly through a 2-wire serial interface called I2C or by programming the internal/external ROMs which contain device settings.

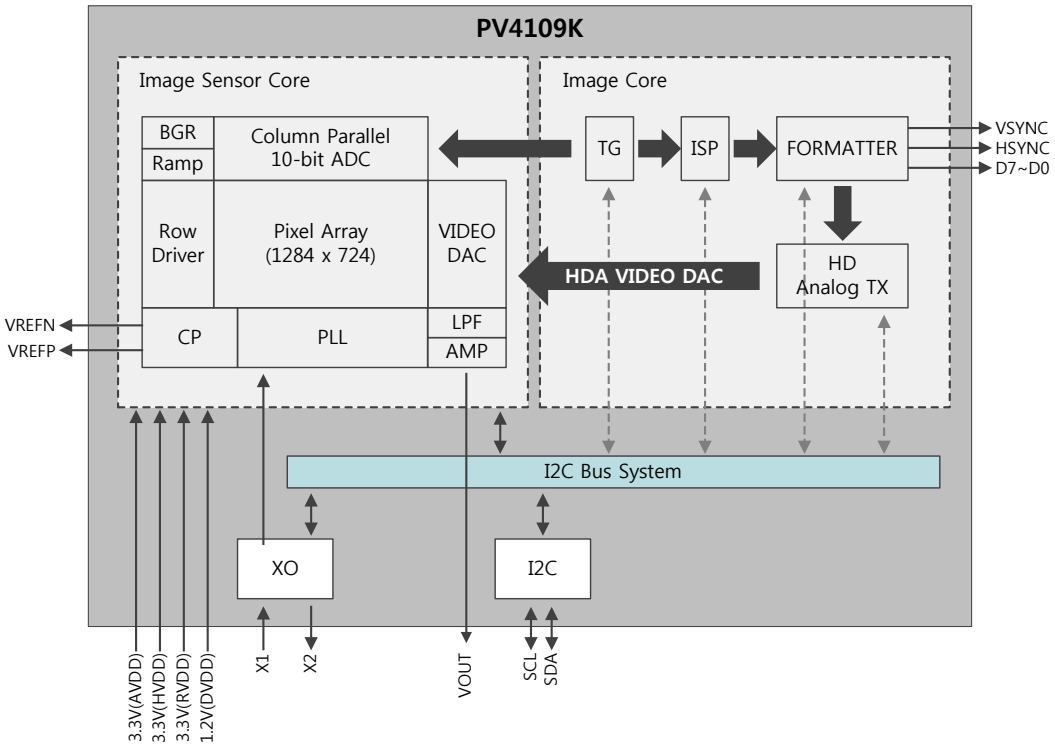


Figure 1 Chip architecture

Frame Structure

The size of a frame is determined by framewidth and frameheight registers. One frame consists of (framewidth + 1) columns and (frameheight + 1) rows, where the size of one frame is allowed to be larger than the total pixel array size. Window determines the output image size, and its default size is 1280 x 720 pixels. It is possible to define a specific region of the frame by a determined window. Pixel scanning is performed row by row on entire frame. Frame row counter and frame column counter, which are limited by framewidth and frameheight values respectively, are used to indicate the current coordinate of pixel being scanning. The column counter value increase by every pixel clock (pclk). every time the column counter reaches maximum value, the row counter value increase. Figure 2 shows the default frame structure and the window position of the PV4109K with origin point (0,0) in the top right corner .

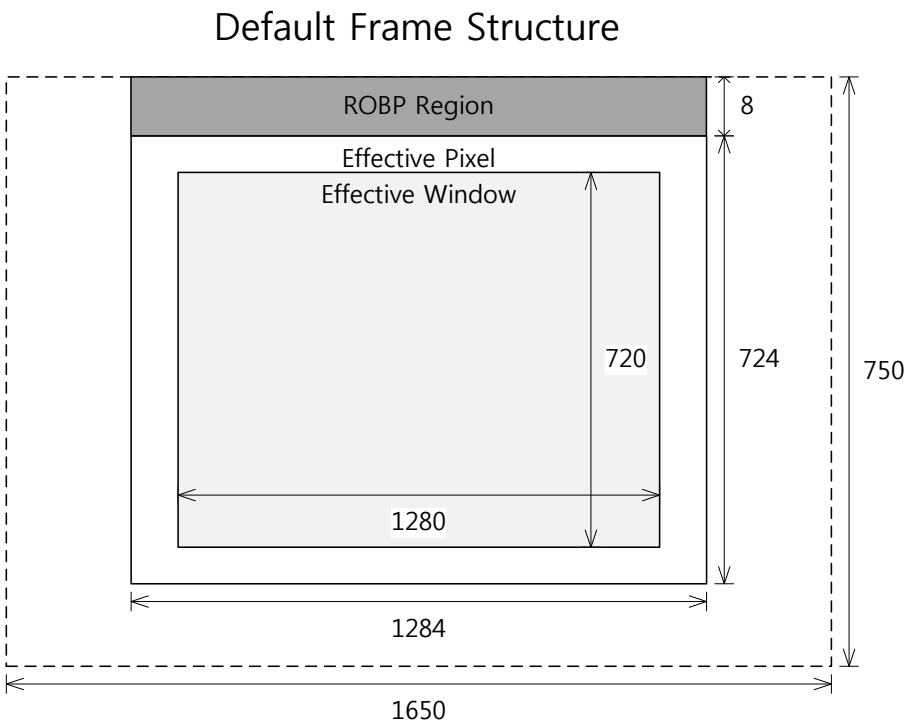


Figure 2 Default frame structure(top view)

Table 2 Register Table - Frame structure

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
framewidth_h	A	06	[2:0]	0x06	RW	aev	Framewidth High Byte (must be larger than window width)
framewidth_l	A	07	[7:0]	0x71	RW	aev	Framewidth Low Byte (must be larger than window width)
frameheight_h	A	08	[1:0]	0x02	RW	aev	Frameheight High Byte (must be larger than window height)
frameheight_l	A	09	[7:0]	0xED	RW	aev	Frameheight Low Byte (must be larger than window height)

Pixel Data Format

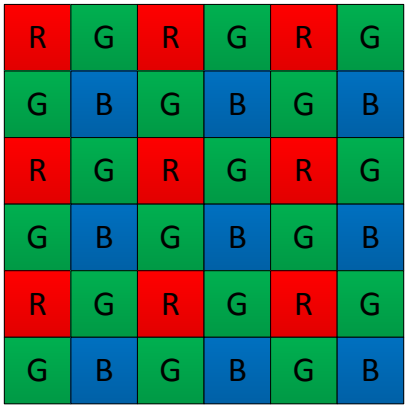


Figure 3 Bayer color filter pattern

The pixel array is covered by Bayer color filters as shown in the Figure 3. Since each pixel can have only one type of filter on it, only one color component can be produced by a pixel. PV4109K provides RGB Bayer pattern data through a 10-bit channel which it passes one pixel data to the output bus at every pclk.

The PV4109K provides horizontal, vertical mirror which respectively reverse the sensor data readout order horizontaly and vertically. Figure 4 shows a normal image and a mirrored image.

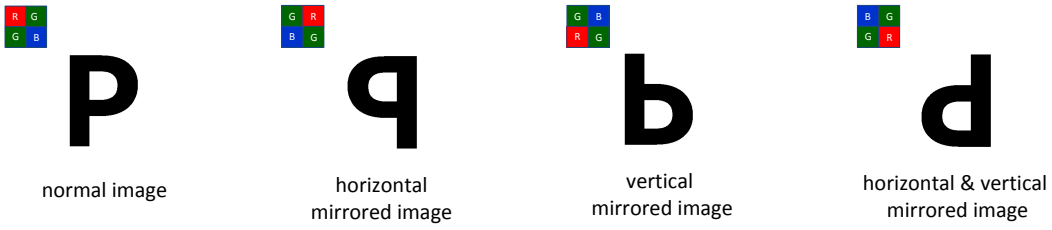


Figure 4 Mirror

Table 3 shows registers relevant to mirror.

Table 3 Register Table - Mirror

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
mirror	A	05	[1:0]	0xx	RW	aev	Image Inversion mirror[1] : vertical inversion mirror[0] : horizontal inversion

Parallel Formatter

Windowing

The image data is outputed by adjusting the desired size to the window within the effective pixel area. windowx1, windowx2, widnwy1, and windowy2 registers determine window's position and size.
upper right corner of window = (windowx1, windowy1)
lower left corner of window = (windowx2, windowy2)

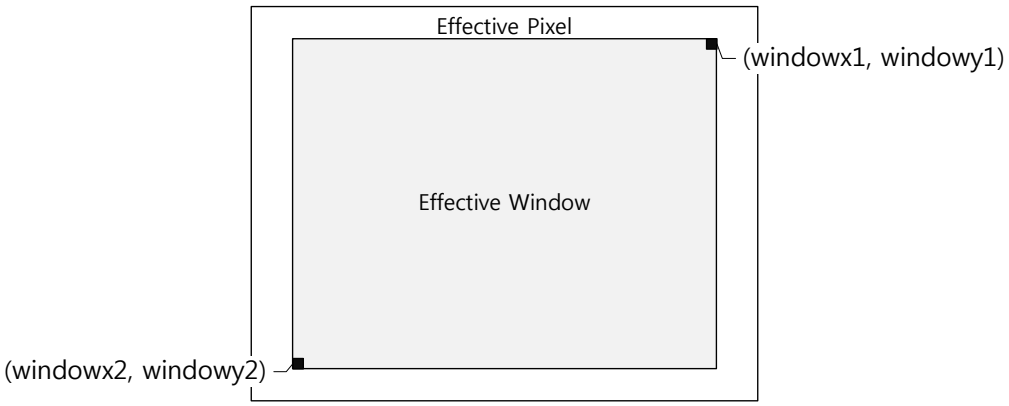


Figure 5 Windowing

Table 4 Register Table - Window

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
windowx1_h	A	0C	[2:0]	0x00	RW	aev	Window horizontal start point High Byte
windowx1_l	A	0D	[7:0]	0x02	RW	aev	Window horizontal start point Low Byte
windowy1_h	A	0E	[2:0]	0x00	RW	aev	Window vertical start point High Byte
windowy1_l	A	0F	[7:0]	0x02	RW	aev	Window vertical start point Low Byte
windowx2_h	A	10	[2:0]	0x05	RW	aev	Window horizontal end point High Byte
windowx2_l	A	11	[7:0]	0x02	RW	aev	Window horizontal end point Low Byte
windowy2_h	A	12	[2:0]	0x02	RW	aev	Window vertical end point High Byte
windowy2_l	A	13	[7:0]	0xD2	RW	aev	Window vertical end point Low Byte

Data control

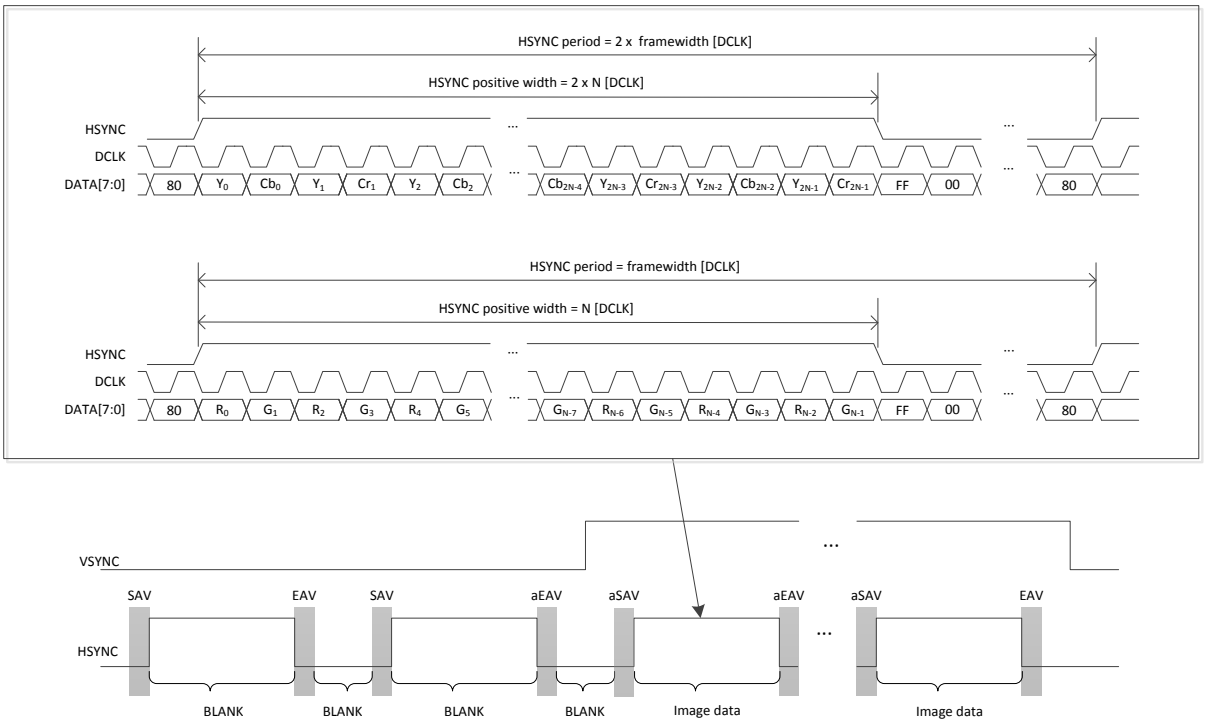


Figure 6 Parallel format timing

The parallel data is controlled by format header, also called timing reference sequence (TRS). The TRS indicates Start or End of video and is included with pixel data during serial transfer. Figure 7 shows TRS and vertical timing.

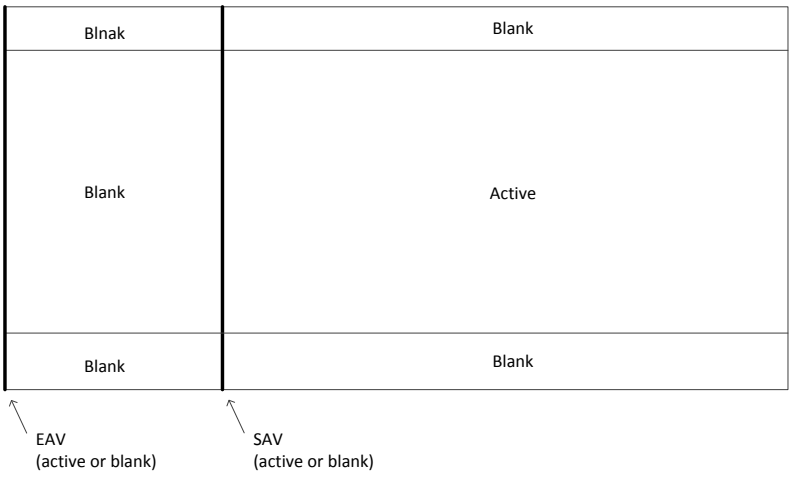


Figure 7 Parallel format

SAV, EAV, aEAV, aSAV and blank data shown in Figure 7 are generated as follows.

```
SAV   = {sync_CCIR_FF, sync_CCIR_00, sync_CCIR_00, sync_blankSAV}
EAV   = {sync_CCIR_FF, sync_CCIR_00, sync_CCIR_00, sync_blankEAV}
aSAV  = {sync_CCIR_FF, sync_CCIR_00, sync_CCIR_00, sync_activeSAV}
aEAV  = {sync_CCIR_FF, sync_CCIR_00, sync_CCIR_00, sync_activeEAV}
BLANK = {sync_CCIR_80, sync_CCIR_10} - - - {sync_CCIR_80, sync_CCIR_10}
```

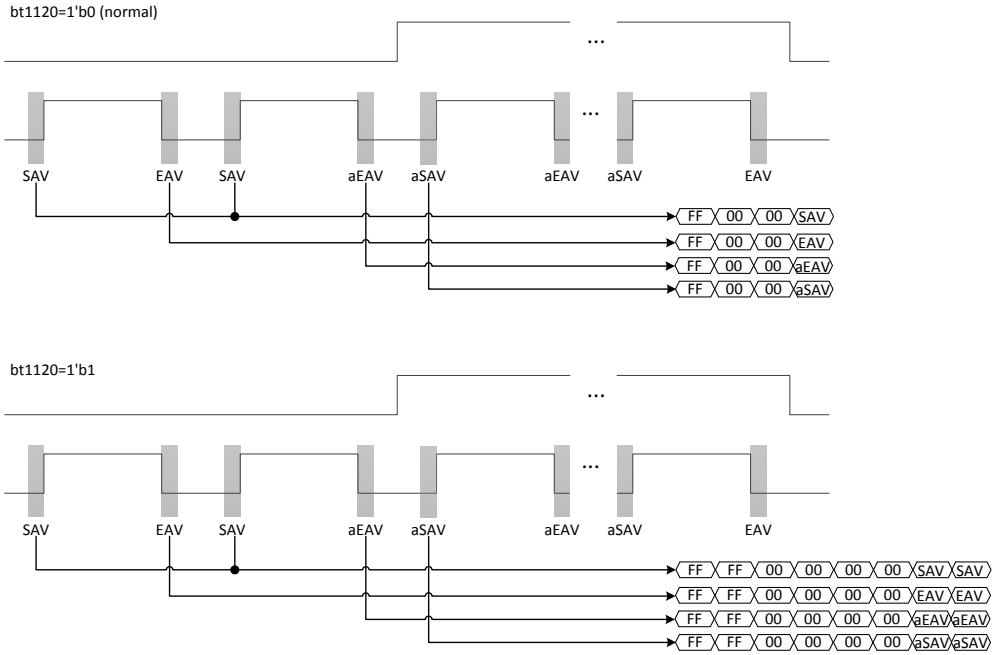


Figure 8 Parallel format header

Table 5 Register Table - Parallel format

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
bt1120	A	1D	[0]	1'b0	RW		Data header control 1'b0 : CCIR656 1'b1 : BT1120
format_control	A	2E	[7:0]	8'h00	RW	aev	1'b0 : yuv422 1'b1 : raw_bayer
sync_blankEAV	A	1E	[7:0]	0xB6	RW		blank EAV for frame data
sync_blankSAV	A	1F	[7:0]	0xAB	RW		blank SAV for frame data
sync_activeEAV	A	20	[7:0]	0x9D	RW		active EAV for frame data
sync_activeSAV	A	21	[7:0]	0x80	RW		active SAV for frame data
sync_CCIR_FF	A	22	[7:0]	0xFF	RW		SMPTE blank data format
sync_CCIR_00	A	23	[7:0]	0x00	RW		SMPTE blank data format
sync_CCIR_80	A	24	[7:0]	0x80	RW		SMPTE blank data format
sync_CCIR_10	A	25	[7:0]	0x10	RW		SMPTE blank data format
init_fmask	A	29	[7:0]	0x01	RW		Initial frame masking after power on
stdby_fmask	A	2A	[7:0]	0x00	RW		Initial frame masking after standby

```
Data sequence
2'b00 = {Cb1, Y1, Cr1, Y2}
2'b01 = {Cr1, Y1, Cb1, Y2}
2'b10 = {Y1, Cb1, Y2, Cr1}
2'b11 = {Y1, Cr1, Y2, Cb1}
```

Table 6 Register Table - Data sequence

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
data_seq	A	1D	[3:2]	2'b00	RW		Data sequence selection

When data_clamp is enabled, active data is clamped by data_min and data_max as shown in Table 7. data_min determine minimum value of active data, and data_max determine maximum value of active data. Table 8 shows registers relevant to data clamp.

Table 7 Register Table - Active data(data_cmlamp = enable)

output bit	data_min	data_max
MSB 8bit	010h	FE0h
MSB 9bit	008h	FF0h
MSB 10bit	004h	FF8h
MSB 11bit	002h	FFCh
MSB 12bit	001h	FFEh

Table 8 Register Table - Data clamp

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
data_clamp	A	1D	[1]	1'b1	RW		Data clamping enable 1'b0 : disable 1'b1 : enable
sync_data_min	A	26	[7:0]	0x01	RW		SMPTE data min value
sync_data_max	A	27	[7:0]	0xFE	RW		SMPTE data max value

Vsync and Hsync

By manipulating vsyncstartrow0, vsyncstoprow0, and vsynccolumn0 register value, start and stop positions of vsync are controlled. sync_drop register allows user to drop vsync or hsync. Figure 9 shows 4 different cases of sync_drop. In addition, sync_hsyncAllLines enables hsync during vsync blank region. Figure 10 shows operation of sync_hsyncAlllines.

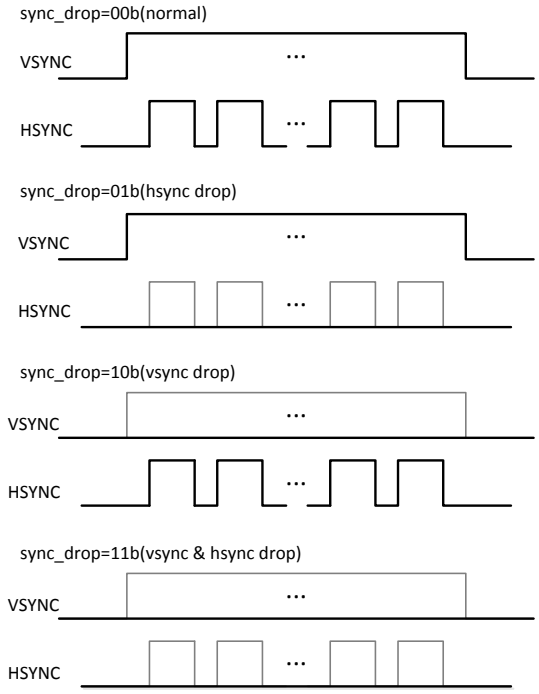


Figure 9 Sync drop

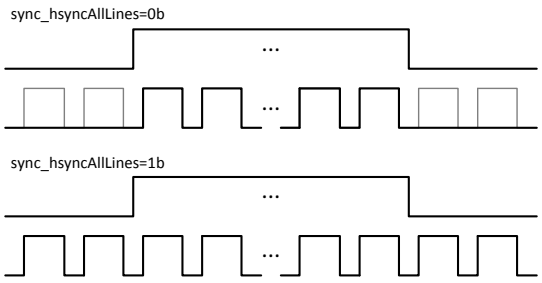


Figure 10 Hsync all lines

sync_vsyncPolarity, sync_hsyncPolarity registers invert vsync, hsync signal respectively. The inversion functions are shown in Figure 11, Figure 12.

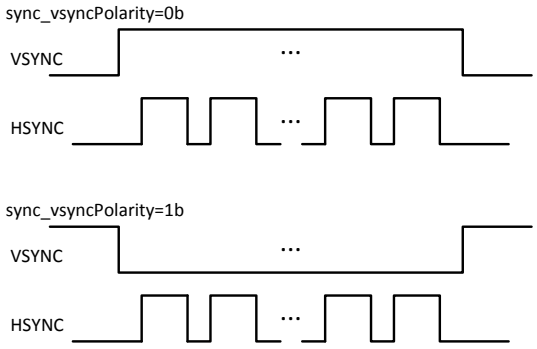


Figure 11 Vsync polarity

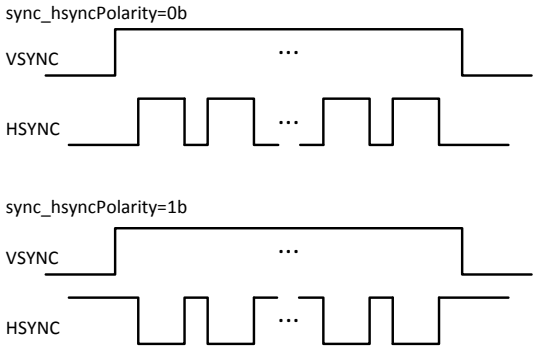


Figure 12 Hsync polarity

Table 9 Register Table - Sync control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
sync_drop	A	1C	[6:5]	2'b00	RW		Vsync, hsync drop control 2'b00 : No drop 2'b01 : hsync drop 2'b10 : vsync drop 2'b11 : hsync and vsync drop
vsync_polarity	A	1D	[6]	1'b0	RW		Vsync polarity change 1'b0 : disable 1'b1 : enable
hsync_all_line	A	1D	[5]	1'b0	RW		Hsync output all lines enable(black and active) 1'b0 : No hsync during vertical blank 1'b1 : hsync during vertical blank
hsync_polarity	A	1D	[4]	1'b0	RW		Hsync polarity change 1'b0 : disable 1'b1 : enable
vsyncstartrow_f0_h	A	14	[4:0]	0x00	RW	aev	Vsync generation row 0 start point High Byte
vsyncstartrow_f0_l	A	15	[7:0]	0x0F	RW	aev	Vsync generation row 0 start point Low Byte
vsyncstoprow_f0_h	A	16	[4:0]	0x02	RW	aev	Vsync generation row 0 stop point High Byte
vsyncstoprow_f0_l	A	17	[7:0]	0xDF	RW	aev	Vsync generation row 0 stop point Low Byte

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
vsynccolumn_h	A	18	[4:0]	0x00	RW	aev	Vsync generation column point High Byte
vsynccolumn_l	A	19	[7:0]	0x00	RW	aev	Vsync generation column point Low Byte

PCLK

PCLK inversion can be enabled via pclk_pol register as shown in Figure 13.

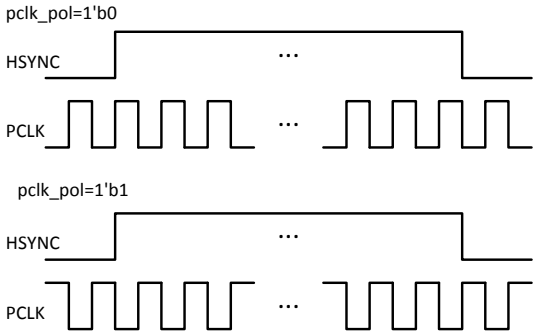


Figure 13 PCLK polarity

Table 10 Register Table - PCLK control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
pclk_pol	A	60	[7]	1'b0	RW		PCLK pad polarity control 1'b0 : disable 1'b1 : enable
pclk_pad_en	A	60	[6]	1'b0	RW		PCLK pad enable 1'b0 : disable 1'b1 : enable
pclk_pad_drv	A	60	[5:4]	2'b00	RW		PCLK pad drivability control
digi_pclk_delay	A	60	[3:0]	4'b0000	RW		PCLK timing delay delay = dly_digi_PCLK*0.4 ns

Digital Parallel Interface

The digital parallel interface uses VSYNC, HSYNC, PCLK, D[7:0] PIN. Table 11 shows digital parallel interface control registers.

Table 11 Register Table - digital parallel interface

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
pclk_pol	A	60	[7]	1'b0	RW		PCLK pad polarity control 1'b0 : disable 1'b1 : enable
pclk_pad_en	A	60	[6]	1'b0	RW		PCLK pad enable 1'b0 : disable 1'b1 : enable
pclk_pad_drv	A	60	[5:4]	2'b00	RW		PCLK pad drivability control
digi_pclk_delay	A	60	[3:0]	4'b0000	RW		PCLK timing delay delay = dly_digi_PCLK*0.4 ns
vsync_pad_en	A	61	[7]	1'b0	RW		Digital video pad enable 1'b0 : disable 1'b1 : enable
hsync_pad_drv	A	61	[6:5]	2'b00	RW		Hsync Pad drivability control
hsync_pad_en	A	61	[4]	1'b0	RW		Hsync pad enable 1'b0 : disable 1'b1 : enable
pad_drv	A	61	[3:2]	2'b00	RW		Data pad drivability control
dpad_swap	A	61	[1]	1'b0	RW		Data pad swap option 1'b0 : [MSB:LSB] 1'b1 : [LSB:MSB]
d7_pad_en	A	62	[7]	1'b0	RW		D7 pad control 1'b0 : disable 1'b1 : enable
d6_pad_en	A	62	[6]	1'b0	RW		D6 pad control 1'b0 : disable 1'b1 : enable
d5_pad_en	A	62	[5]	1'b0	RW		D5 pad control 1'b0 : disable 1'b1 : enable
d4_pad_en	A	62	[4]	1'b0	RW		D4 pad control 1'b0 : disable 1'b1 : enable
d3_pad_en	A	62	[3]	1'b0	RW		D3 pad control 1'b0 : disable 1'b1 : enable
d2_pad_en	A	62	[2]	1'b0	RW		D2 pad control 1'b0 : disable 1'b1 : enable
d1_pad_en	A	62	[1]	1'b0	RW		D1 pad control 1'b0 : disable

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							1'b1 : enable
d0_pad_en	A	62	[0]	1'b0	RW		D0 pad control 1'b0 : disable 1'b1 : enable
led_pad_sel	A	63	[6]	1'b0	RW		D0 pad selection 1'b0 : D0 pad 1'b1 : LED pad
led_pad_drv	A	63	[5:4]	1'b0	RW		LED pad drivability contro
mirs_pad_drv	A	63	[1:0]	1'b0	RW		MIRS pad drivability contro

Recommended Power Sequence

- AVDD : Analog block1 & Pixel (external 3.3[V])
- RVDD : Analog block2 (external 3.3[V])
- HVDD : IO (external 3.3[V])
- DVDD : TG & ISP (external 1.2[V])

Table 12 Recommended power-on/off sequence

Symbol	Descriptions	Min	Typ	Max	Unit
t1	From HVDD rising to DVDD rising	0	-	100	ms
t2	From DVDD rising to AVDD & RVDD rising	0	-	100	ms
t3	Sensor reset time	20	-	-	us
t4	From AVDD & RVDD falling to DVDD falling	0	-	-	ms
t5	From DVDD falling to HVDD falling	0	-	-	ms

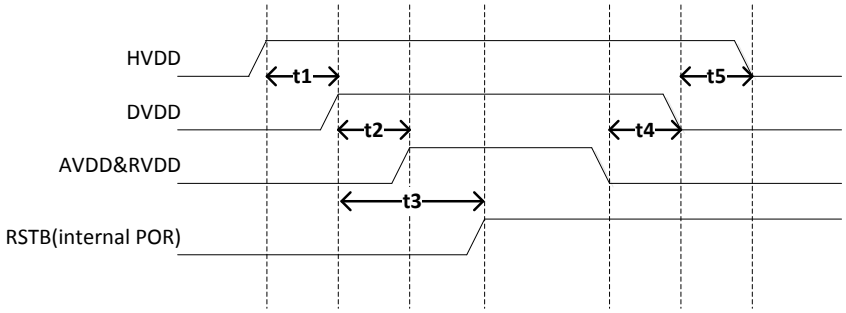


Figure 14 Timing diagram of power-on/off sequence

Clock

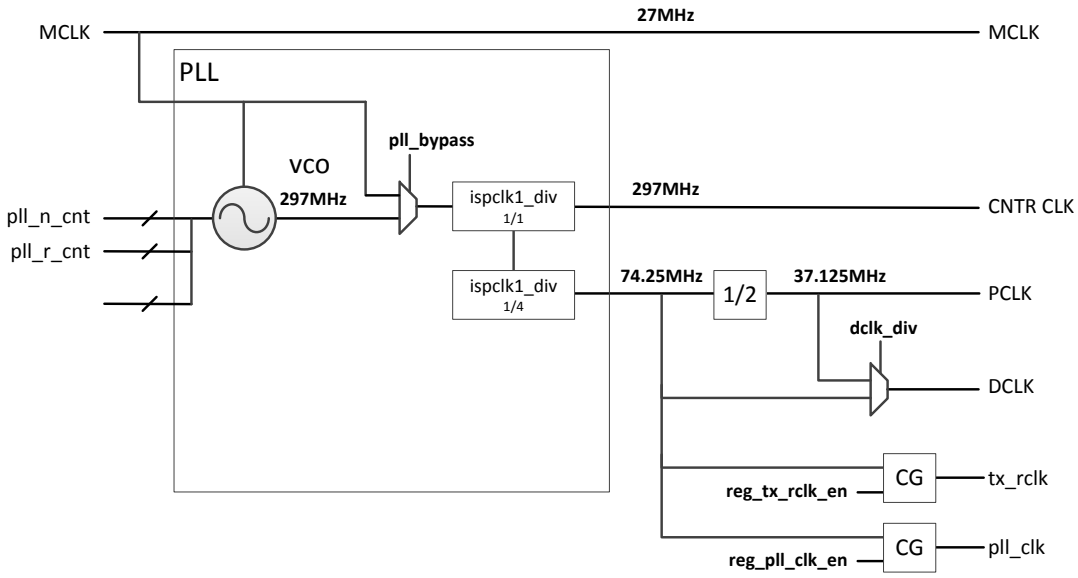


Figure 15 Clock divider

- MCLK : PLL input clock
- VCO : PLL output clock
- CNTR CLK : Clock for Counter
- PCLK : The counter values increase at the pace of pclk.
- DCLK : Clock for formatter
- tx_rclk : Clock for Tx
- pll_clk : Clock for VDAC

PLL

- Frequency of mclk(PLL input clock) should be mclk/pll_r_cnt $\geq$ 4MHz.
- Frequency of vco(PLL output clock) should be 120MHz $\geq$ vco $\leq$ 606MHz.
  vco = mclk x pll_n_cnt/pll_r_cnt
- PLL Lock time should be >20us.
- Status of initial PLL
  strap_master = 1'b0 : status of initial PLL = off
  strap_master = 1'b1 : status of initial PLL = on. PLL is on automatically after about 33 ms from reset.

Table 13 Register Table - PLL

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
pll_n_cnt	A	57	[7:0]	0x2C	RW		PLL multiplication factor
pll_r_cnt	A	58	[4:0]	0x04	RW		PLL division factor
plltg_pd	A	55	[5]	1'b1	RW		PLL power down mode 1'b0 : pll power on 1'b1 : pll power down
pll_bypass	A	55	[4]	1'b1	RW		PLL bypass 1'b0 : use pll mode 1'b1 : pll bypass mode

Clock Divider

Table 14 Register Table - Clock divider

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
adcclk_div	A	59	[7:6]	2'b01	RW		ADC clock divider isp_clk =vco1/(2^adcclk_div)
ispclk1_div	A	59	[5:4]	2'b10	RW		ISP clock divider isp_clk =vco1/(2^ispclk_div)
dclk_div	A	5C	[7]	1'b0	RW		D clk divider 1'b0 : 1/1 1'b1 : 1/2
cp_test_en	A	5C	[4]	1'b0	RW		CP test mode enable 1'b0 : disable 1'b1 : enable
tx_rclk_en	A	5C	[3]	1'b1	RW		tx_rclk clock gate enable 1'b0 : disable 1'b1 : enable
pll_clk_en	A	5C	[2]	1'b1	RW		pll_clk clock gate enable 1'b0 : disable 1'b1 : enable
clkoff	A	5F	[3]	1'b0	RW		Clock pad kill enable 1'b0 : disable (not kill) 1'b1 : enable (kill)
osc_pad_drv	A	5F	[1:0]	2'b00	RW		OSC pad drivability control
osc_pad_en	A	5F	[2]	1'b1	RW		OSC pad enable 1'b0 : disable 1'b1 : enable

PLL and Clock Setting Sequence

- When using PLL, set-up sequence, show Figure 16, is necessary.
- I2C update timing register, i2c_control_1, is changed before setting clock dividers to immediately apply clock divider settings.

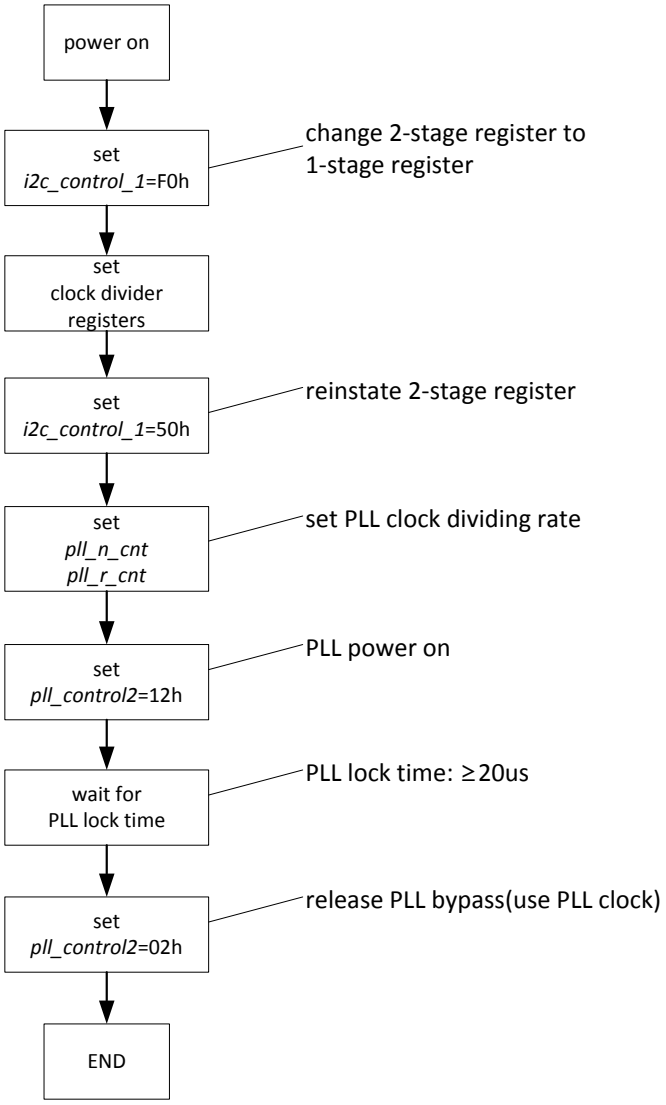


Figure 16 Clock setting sequence

Reset

The PV4109K has two methods to reset: hard reset and soft reset. Hard reset signal from RSTB PAD must remain low (active low) for at least 8 master clocks to correctly reset the sensor. All registers are set to their default values after reset.

Figure 17 shows device soft reset by setting softreset register through I2C interface. When softreset register is set, async_rstb (asynchronous reset) and sync_rstb signal changes from 1 to 0 and holds for 1 clock of SCL. Afterward, async_rstb is set back to 1 while sync_rstb holds 0 for another 16 clocks of pclk for stable reset operation. Therefore, PV4109K requires at least 1 clock of SCL and 16 clocks of pclk to perform a soft reset operation.

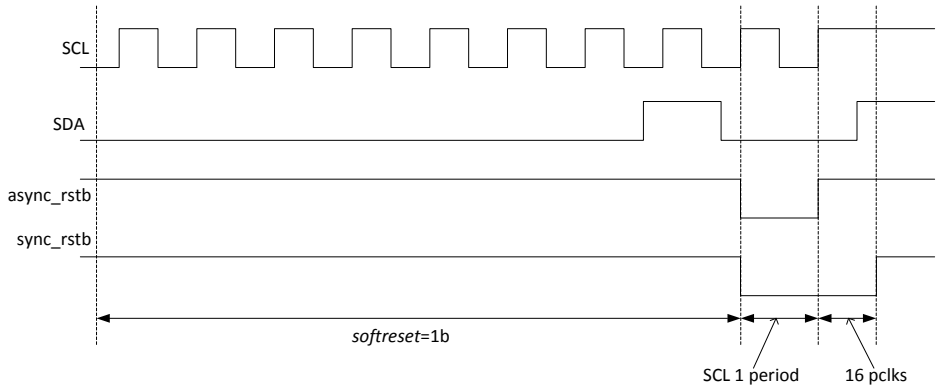


Figure 17 Soft reset

Table 15 Register Table - Soft reset

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
softreset	A	37	[0]	0x00	RW		Soft reset 1'b0 : disable 1'b1 : enable (after succesful reset value re-verts to 0)

Initialization

Initialization Flow

When power is applied to the chip, an initialization operation is performed. The initialization operation performs different operations depending on the master mode. If master mode is off, initialization is not performed. If master mode is on, start from internal ROM setting. After completing the setting of the internal ROM, the I2C bus must be idle state before entering the next initialization phase. After internal ROM setting, detection is performed for EEPROM, and if there is no corresponding ROM, jump to the next step. Figure 18 represents the initialization flow.

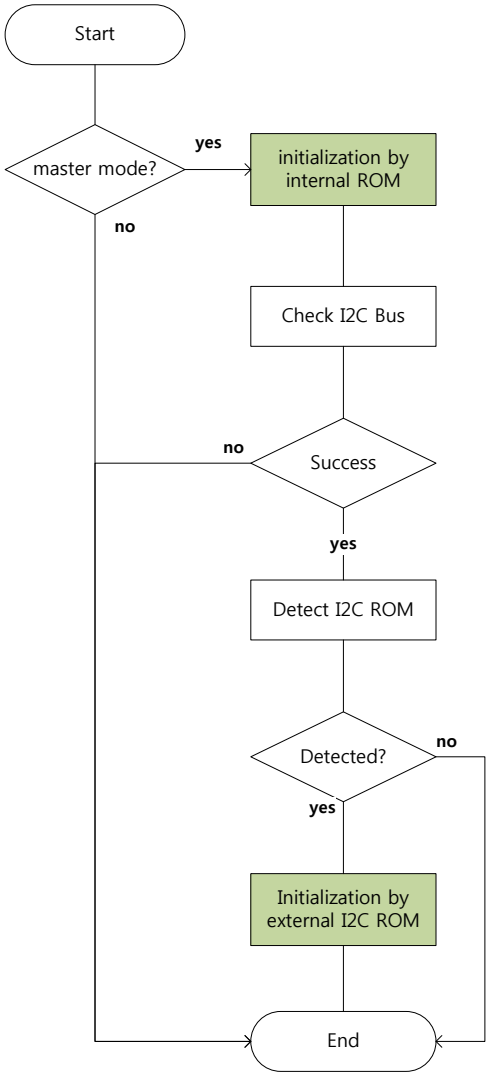


Figure 18 Initialization flow

PV4109K has a single I2C master and shares the SCL / SDA line with the I2C slave. External I2C master can access PV4109K after Figure 18 process is completed. The initialization time depends on the conditions of master mode and external ROM.

Required Time of Initialization

- Master mode on
  a. In case that external ROM does not exist
     The time to end the internal ROM setting is 33 ms.
  b. In case that EEPROM does exist(SCL @ about 400 KHz)
     Cycle time for register write is 125 us
  c. In master mode, the initialization time is calculated as a + b.
- Master mode off
  a. Setting time is 0 s.
  b. The initialization time is not required when master mode is off.

Wire-strapping

Wire-strapping is a function that can control the setting mode with PAD input. The setting mode is determined by VSYNC, D5, D6, and D7 PAD. Check the PAD input voltage during chip initialization and perform setting according to setting mode. It is shown in setting mode Table 16 according to PAD input voltage.

Table 16 Setting mode according to wire-strapping

		VSYNC	D5	D6	D7
MASTER MODE	ON	H	-	-	-
	OFF	L	-	-	-
PG	Enable	-	H	-	-
	Disable	-	L	-	-
MIRROR	NO MIRROR	-	-	H	L
	MIRROR-V	-	-	L	L
	MIRROR-H	-	-	H	H
	MIRROR-VH	-	-	L	H

Internal ROM

PV4109K reads the data according to the PAD input from the internal ROM and performs setting.

Register settings according to mirror mode are shown in Table 17.

Table 17 Mirror mode

{MIRR1,MIRR0}	2'b00	2'b01	2'b10	2'b11
Register name	**V mirror**	**HV mirror**	**NO mirror**	**H mirror**
mirror	02	03	00	01

External ROM

External ROM Structure

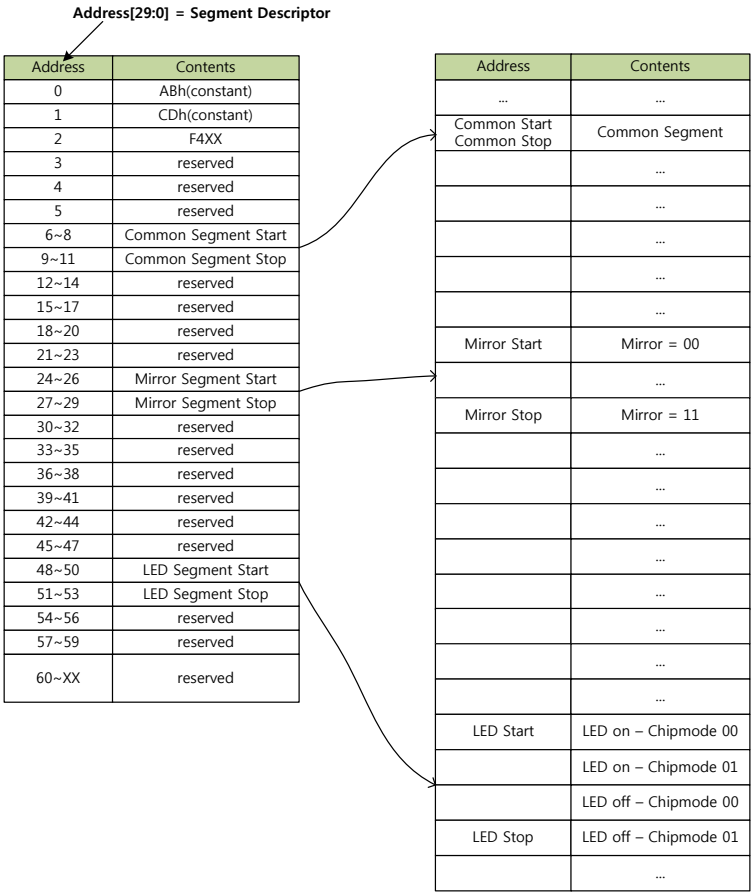


Figure 19 External ROM structure

Figure 19 shows external ROM structure. The user can use the external ROM to apply settings differently depending on the strap input or the external environment. The external ROM consists of the following segments.

Common segment : Regardless of the strap, it is set in the external ROM initialization process.
Mirror segment : Depending on the mirror strap, the settings are applied differently.
LED segment : Depending on the LED state(ON/OFF), the settings are applied differently.

Table 18 Register Table - External ROM settings

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
sif_chip_mode	F	64	[6:5]	2'b00	RW		Chip mode selection 2'b00 : Chipmode 00 else : Chipmode 01

I2C EEPROM

EEPROM can be used as External ROM. All segments are used in EEPROM.

Register Selector in Master Mode

bank_m select register bank in Master mode.

- Register group
  - A(00h) / B(01h) / C(02h) / D(03h) / E(04h) / F(05h) / G(06h) / H(07h)
  - I(08h) / J(09h) / K(0Ah) / L(0Bh) / M(0Ch) / N(0Dh) / O(0Eh) / P(0Fh)

Table 19 Register Table - Register Selecter in Master mode

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
bank_m	A	FF	[7:0]	0x00	RW		Register group selector in master mode

External Communication Specification

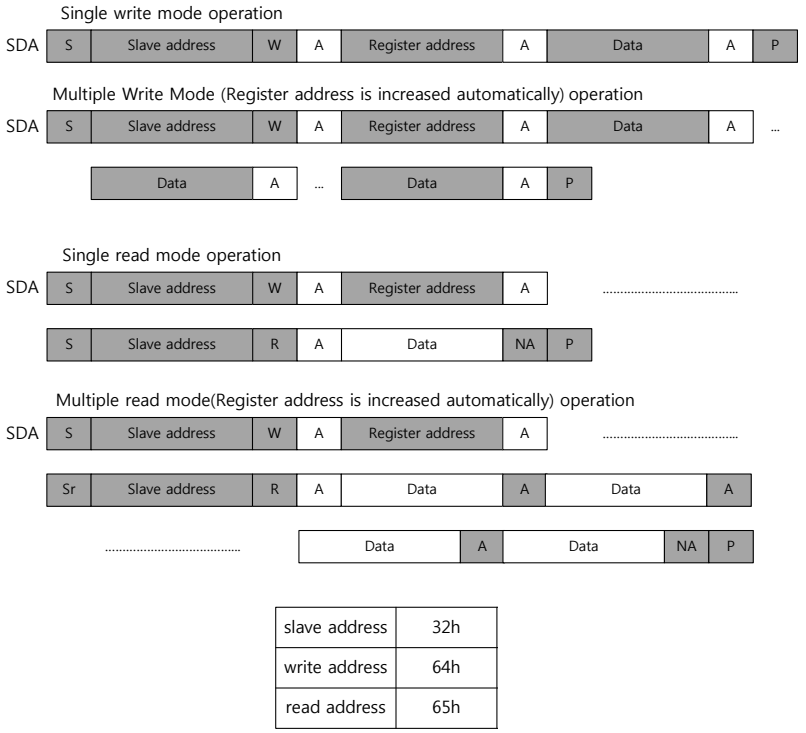
I2C Communication

I2C communication is a serial interface which utilizes SCL/SDA lines to transfer 8-bit data per transaction. PV4109K includes only I2C slave function and requires external master to access the internal registers. Each transaction requires 8-bit data and 1-bit acknowledge bit. There are four types of operations supported in PV4109K's I2C operation: single write, multiple write, single read, multiple read.

In single write operation, after the start state, 7-bit slave address and write bit are transmitted from master device to PV4109K. If correct slave address is detected, PV4109K reply with acknowledge bit as confirmation of valid address. Then master device transmits register address and waits for acknowledge bit from PV4109K. Lastly, 8-bit data is sent to PV4109K and waits for acknowledge bit again. Once acknowledge bit is recieved, master device announces the stop state to terminate I2C communication.

Multiple write operation works exactly the same until stop state procedure. Instead of announcing the stop state, master device transmits more data. If PV4109K detects multiple write operation, any data stream following the first 8-bit is stored in subsequent register addresses of the first register address.

Read operation consists of two sub-procedure: address write and data read. The procedure is performed exactly same as register address write procedure from single write operation. Afterward, master device announces repeated start and transmit slave address with read bit. When PV4109K detects read operation, PV4109K sends acknowledge bit to master device, then reads register corresponding to register address. PV4109K transmits read data to master device and waits for master device to respond. If master device responds with no acknowledge bit followed by stop state, read operation is terminated. On the other hand, if master device responds with acknowledge, PV4109K reads the subsequent register and transmits again. As long as master device replies with acknowledge bit after each data transaction, PV4109K will continuously read the subsequent register and transmit until no acknolwedge bit followed by stop state is presented. If only one 8-bit data is read, the procedure is single read operation. whereas, reading more than 8-bit data is multiple read operation. Figure 20 shows read/write operation of I2C communication.



slave address	32h
write address	64h
read address	65h

R/W : Read/Write selection, High = read / Low = write
A : Acknowledge bit, NA : No Acknowledge, DATA : 8-bit data. P : Stop condition
S : Start condition, Sr : Repeated start(start without preceding stop)

Figure 20 I2C functional description

Register Update Timing

Registers has three different types of update timing: "aev" and "autov" update, regular update. Registers with "aev" and "autov" update type update new values from I2C write operation at the last line of the frame. Whereas, registers with regular update type apply new values immediately after I2C write operation. However, By changing updatecontrol register value, register updates for "aev" and "autov" type can either be disabled or be updated immediately.

Table 20 I2C update timing control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
updatecontrol	A	35	[7:4]	4'b0101	RW		[7:6] : Control I2C Register Update by auto_vsync update_autov <= reg_updatecontrol[3] or (autov_update and reg_updatecontrol[2]) [5:4] : Control I2C Register Update by ae_vsync update_aev <= reg_updatecontrol[1] or (aev_update and reg_updatecontrol[0])

LED Control

LED control functions include IRLED control with CdS, LED blinking.

The IRLED control function uses infrared light by operating the external IRLED in low light conditions where there is not enough visible light. real_led_data means the amount of light absorbed by CdS. IRLED control function has auto mode and manual mode.

- ledctl en = 1'b1 (auto mode)
  When real_led_data is less than led_lvth1, 1'b1 (LED on) signal is output. When real_led_data is greater than led_lvth2, it outputs 1'b0 (LED off) signal. The led_frame is a value that delays the IRLED on / off transition. The unit of led_frame is frame. (refet to Figure 21)

- ledctl en = 1'b0 (manual mode)
  The ledctl manual controls the IRLED control output. When ledctl manual is set to 1'b1, it outputs LED on signal, If ledctl manual is set to 1'b0, it outputs LED off signal.

Bwled en is a function that changes the screen to black and white in LED on operation.

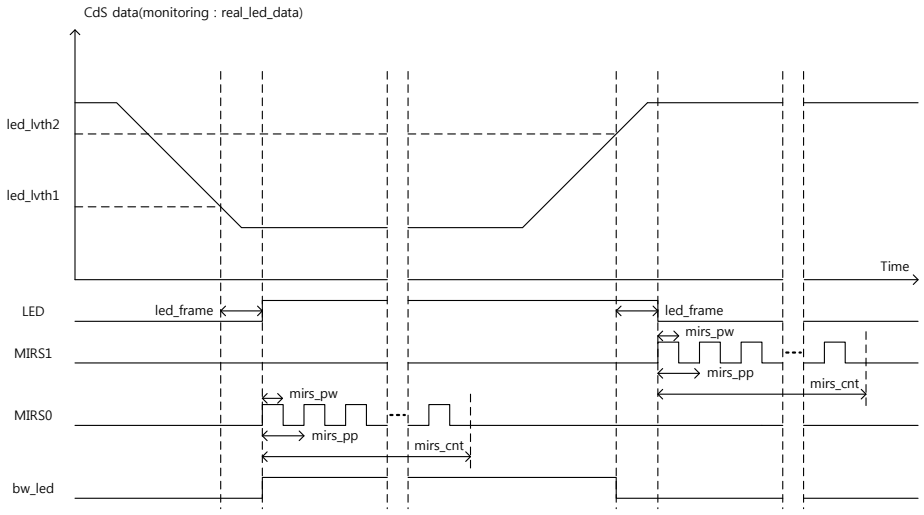


Figure 21 LED control with CdS

Table 21 Register Table - LED control with CdS

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
ledctrl_en	A	80	[7]	1'b0	RW		LED control enable 1'b0 : disable 1'b1 : enable
ledctl_manual	A	80	[6]	1'b0	RW		LED manual enable 1'b0 : disable 1'b1 : enable
ledctl_pol	A	80	[5]	1'b0	RW		LED control polarity enable 1'b0 : disable 1'b1 : enable
led_pad_sel	A	63	[6]	1'b0	RW		D0 pad selection

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							1'b0 : D0 pad 1'b1 : LED pad
led_pad_drv	A	63	[5:4]	1'b0	RW		LED pad drivability contro
mirs_en	A	80	[3]	1'b0	RW		MIRS control enable 1'b0 : disable 1'b1 : enable
mirs_manual_mode	A	81	[4]	1'b0	RW		MIRS manual mode enable 1'b0 : enable 1'b1 : disable
mirs_manual	A	80	[2:1]	2'b00	RW		MIRS manual control 2'b00 : MIRS1 Low / MIRS0 Low 2'b01 : MIRS1 Low / MIRS0 High 2'b10 : MIRS1 High / MIRS0 Low 2'b11 : MIRS1 High / MIRS0 High
mirs_pol	A	80	[0]	1'b0	RW		MIRS control polarity enable 1'b0 : disable 1'b1 : enable
mirs_swap	A	81	[5]	1'b0	RW		MIRS control swap enable 1'b0 : disable 1'b1 : enable
mirs_pad_en	A	8B	[0]	0x00	RW		MIRS pad enable
real_led_data	B	E9	[7:0]		RO		Current CdS data
led_lvth1	A	82	[7:0]	0x00	RW		CdS level threshold for LED control via CdS
led_lvth2	A	83	[7:0]	0x00	RW		CdS level threshold for LED control via CdS
led_frame	A	84	[7:0]	0x80	RW		LED blink pulse width control
mirs_pw	A	85	[7:0]	0x64	RW		Moving filter control pulse width
mirs_pp	A	86	[7:0]	0xC8	RW		Moving filter control pulse period
mirs_cnt	A	87	[7:0]	0x01	RW		The number of moving filter control pulse
bwled_en	A	80	[4]	1'b0	RW		BWLED enable 1'b0 : disable 1'b1 : enable
bwled_manual	A	81	[6]	1'b0	RW		BWLED manual enable 1'b0 : disable 1'b1 : enable
led_blink_en	A	81	[3]	1'b0	RW		LED blink enable 1'b0 : disable 1'b1 : enable
led_blink_frame	A	8A	[7:0]	0x00	RW		LED blinks per # frame

Exposure Control

Integration Time

PV4109K employs rolling shutter [1] for capturing image. Reset operation initializes ROBP and active pixel region in sequence row by row. Readout process reads pixel data stored in photodetector at the identical order and speed as reset operation. The difference in time between reset and readout operation is known as integration time (refer to Figure 22). Integration time controls photodetector's level of exposure to light. Integration time can be adjusted in line unit level (line inttime) and column unit level (column inttime). Under the assumption of fixed frame structure, the maximum line inttime is "frame height - 5" and column inttime is "frame width - 1". Upper 16 bits of inttime register represent number of lines for line inttime and lower 8 bits of inttime register represent number of column inttime, where number of column changes in framewidth/256 increment.

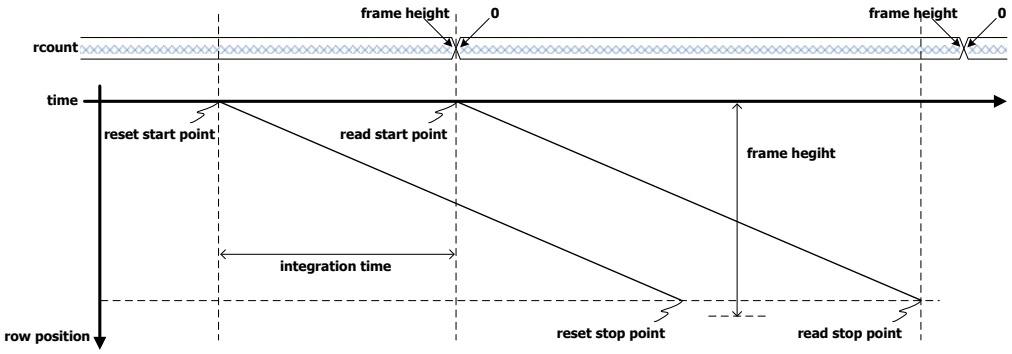


Figure 22 Fundamental concept of integration time

Table 22 shows registers relevant to integration time.

Table 22 Register Table - Integration time

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
inttime_h	B	6E	[7:0]	0x01	RW	wr_en	Integration time (line) High Byte
inttime_m	B	6F	[7:0]	0x40	RW	wr_en	Integration time (line) Low Byte
inttime_l	B	70	[7:0]	0x00	RW	wr_en	Iinteration time (column)

[1] Image capture method in which each frame is scanned row by row instead of capturing entire frame at once

Global Gain

Global gain affects analog gain level of comparators, which determines Bayer data values. In PV4109K, global gain is ranged from 0x00 to 0x5F.

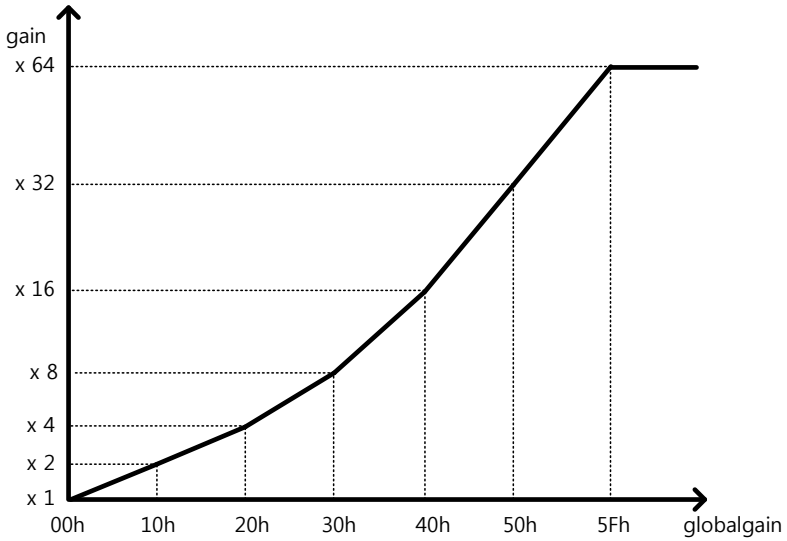


Figure 23 Globalgain's gain

Table 23 shows registers relevant to global gain.

Table 23 Register Table - Global Gain

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
globalgain	B	71	[7:0]	0x00	RW	wr_en	Analog gain

Exposure factor update control

If the exposure factor is changed over several frames, the brightness of the screen changes for each frame, which causes hunting. Therefore, exposure related registers are updated at once and the brightness of the screen is not changed many times.

- If wr_en = 1'b1, exposure register is updated. and then wr_en = 1'b0.
- If wr_en_off = 1'b1, wr_en is disabled.

Table 24 shows registers relevant to exposure register update

Table 24 Register Table - Exposure register update

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
wr_en	B	74	[0]	0x00	RW		Update exposure related register 1'b0 : no update 1'b1 : wr_en set
wr_en_off	B	75	[0]	0x01	RW		wr_en control register 1'b0 : wr_en enable 1'b1 : wr_en disable

ISP(Image Signal Processing)

ISP in PV4109K enhances image quality of input images from the pixel sensor. Supported functions in PV4109K are as follows:

- "Test Pattern (TP) Control"
- "Lens Shading Compensation (LSC)"
- "White Balance Gain"
- "Noise Reduction (NR)"
- "Edge Enhancement"
- "Color Correction (CCR)"
- "RGB Gamma"
- "De-color"
- "Y Gamma"
- "Contrast"
- "Y Offset"
- "Color Saturation"

Test Pattern (TP) Control

TP control generates test images from ISP block. Test images type can be selected by setting tp_control_0 registers. In case of test image types from 0x15 to 0x1A values for tp_control_0, tp_control_1/2/3/4/5 registers are used as color values and the following rule shows how the color value is determined:

- R : {tp_control_1, tp_control_5[7:6]}
- Gr : {tp_control_2, tp_control_5[5:4]}
- Gb : {tp_control_3, tp_control_5[3:2]}
- B : {tp_control_4, tp_control_5[1:0]}

Table 25 shows registers relevant to Test Pattern Control.

Table 25 Register Table - Test pattern control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
tp_control_0	D	70	[7:0]	0x00	RW		Test pattern selection
tp_control_1	D	71	[7:0]	0x00	RW		R[9:2] color for test pattern
tp_control_2	D	72	[7:0]	0x00	RW		G1[9:2] color for test pattern
tp_control_3	D	73	[7:0]	0x00	RW		G2[9:2] color for test pattern
tp_control_4	D	74	[7:0]	0x00	RW		B[9:2] color for test pattern
tp_control_5	D	75	[7:0]	0x00	RW		{R[1:0],G1[1:0],G2[1:0],B[1:0]} for test pattern

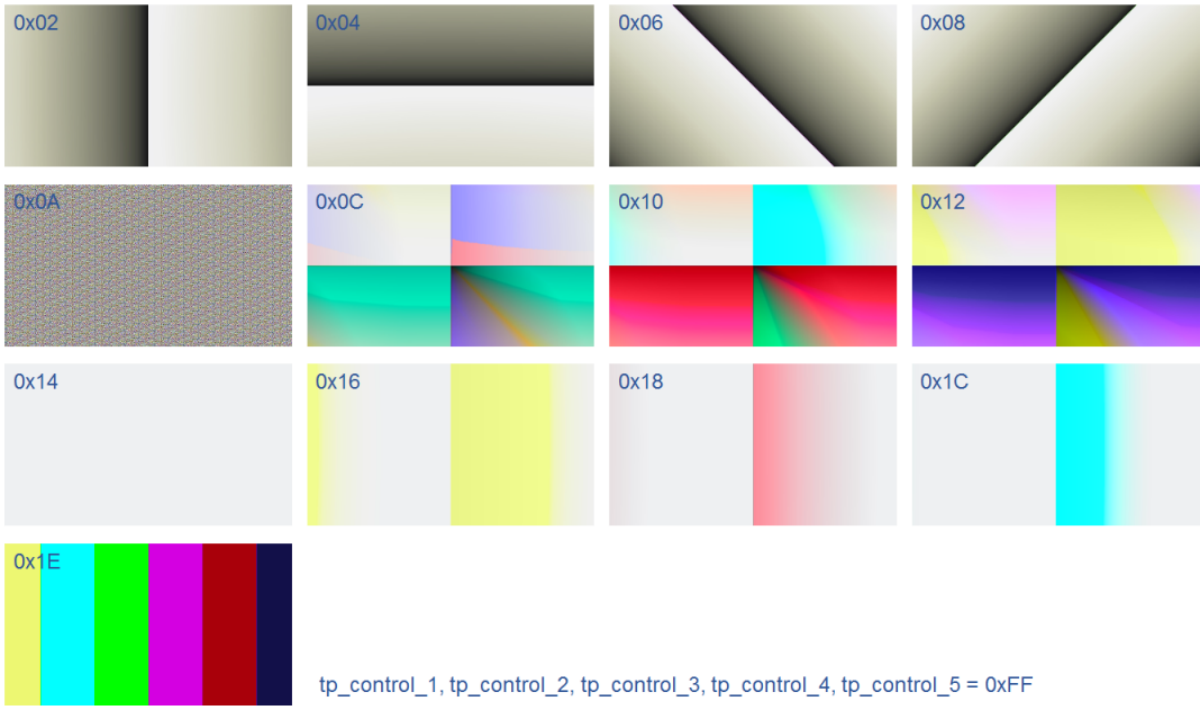


Figure 24 Test image

Lens Shading Compensation (LSC)

Pixel sensor residing in edge of the lens receives less light, whereas ample light exposure is obtained in center pixels. LSC feature compensates this uneven distribution of light exposure. By setting lens_en = 1'b1, LSC feature is enabled. LSC function control components are LSC center, LSC scale, and LSC gain.

- LSC center
  By setting lens_x and lens_y, LSC center is adjusted as shown in Figure 25. This parameter is adjusted if the center of the image is not lined up with the center of the lens.

- LSC scale
  By setting lens_scale, scale rate of lens gain from the LSC center is adjusted. lens_scale value is directly proportional to lens gain value.

- LSC gain
  Lens gain of R, G1, G2, B channel can be separately adjusted through lens_gainr, lens_gain_g1, lens_gain_g2, and lens_gainb registers respectively. Setting high value to the registers result in high lens gain.

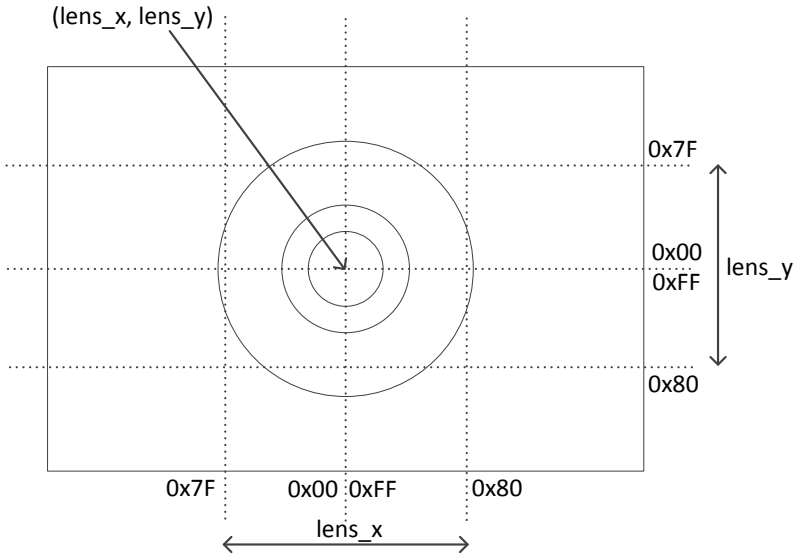


Figure 25 LSC center control

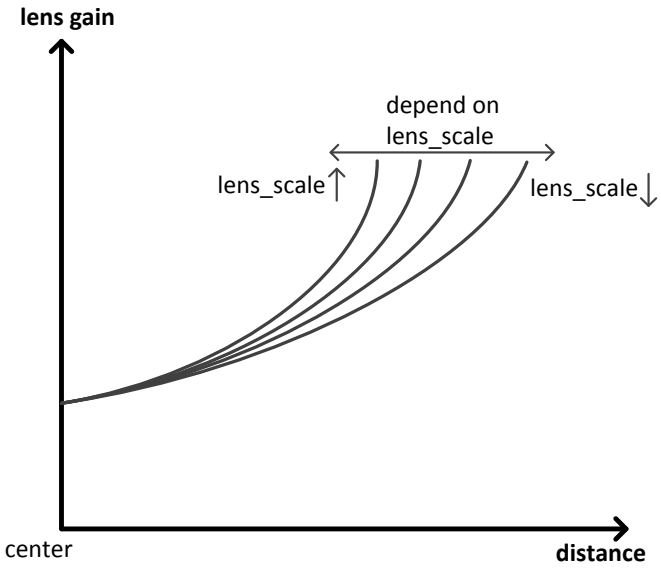


Figure 26 LSC gain fitting with LSC center and LSC scale

Table 26 shows registers relevant to LSC functions.

Table 26 Register Table - LSC

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
lens_en	D	66	[7]	1'b1	RW	aev	Lens shading compensation enable 1'b0 : disable 1'b1 : enable
lens_scale	D	83	[7:0]	0x0C	RW		Lens shading compensation scale control
lens_x	D	84	[7:0]	0x00	RW		Lens shading compensation center horizontal control
lens_y	D	85	[7:0]	0x00	RW		Lens shading compensation center vertical control
lens_gainr	D	86	[7:0]	0x20	RW	aev	Lens shading compensation R gain
lens_gaing1	D	87	[7:0]	0x20	RW	aev	Lens shading compensation G1 gain
lens_gaing2	D	88	[7:0]	0x20	RW	aev	Lens shading compensation G2 gain
lens_gainb	D	89	[7:0]	0x20	RW	aev	Lens shading compensation B gain

White Balance Gain

WB gain is applied to images to remove the unrealistic color coming from different color temperature. Proper application of WB results in objects which appear white in person are displayed white in the output image. PV4109K includes two modes of WB process: automatic WB mode and manual WB mode. Automatic WB mode and manual WB mode are selected by setting wb_manual = 1'b0 and wb_manual = 1'b1 respectively. In automatic WB mode, ISP firmware attempts to evaluate proper WB gain and stores to wb_r/g/bgain registers. Whereas, in manual WB mode, users apply desired WB gain by writing values to wb_mr/mg/mbgain.

Table 27 shows registers relevant to WB gain.

Table 27 Register Table - White balance gain

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
wb_rgain_h	D	8F	[0]	0x00	RW	aev	Auto white balanc "R" gain High Byte
wb_rgain_l	D	90	[7:0]	0x5D	RW	aev	Auto white balanc "R" gain Low Byte
wb_ggain_h	D	91	[0]	0x00	RW	aev	Auto white balanc "G" gain High Byte
wb_ggain_l	D	92	[7:0]	0x40	RW	aev	Auto white balanc "G" gain Low Byte
wb_bgain_h	D	93	[0]	0x00	RW	aev	Auto white balanc "B" gain High Byte
wb_bgain_l	D	94	[7:0]	0x5E	RW	aev	Auto white balanc "B" gain Low Byte
wb_mrgain_h	D	96	[0]	0x00	RW	aev	Manual white balanc "R" gain High Byte
wb_mrgain_l	D	97	[7:0]	0x5D	RW	aev	Manual white balanc "R" gain Low Byte
wb_mggain_h	D	98	[0]	0x00	RW	aev	Manual white balanc "G" gain High Byte
wb_mggain_l	D	99	[7:0]	0x40	RW	aev	Manual white balanc "G" gain Low Byte
wb_mbgain_h	D	9A	[0]	0x00	RW	aev	Manual white balanc "B" gain High Byte
wb_mbgain_l	D	9B	[7:0]	0x5E	RW	aev	Manual white balanc "B" gain Low Byte
wb_manual	D	9C	[0]	0x00	RW		WB gain mode selection 1'b0 : auto WB gain 1'b1 : manual WB gain

Noise Reduction (NR)

NR is enabled by setting nr_en = 1’b1. The effectiveness of noise reduction is adjusted by changing nr_ratio registers. Lower value of nr_ratio results in higher noise reduction strength. On the other hand, higher value of nr_ratio results in lower noise reduction strength.

Table 28 shows registers relevant to NR functions.

Table 28 Register Table - NR

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
nr_en	H	04	[7]	1'b0	RW	aev	NR enable 1'b0 : disable 1'b1 : enable
nr_ratio	H	04	[3:0]	0x00	RW	aev	NR strength control 4'h0 : 100% NR 4'h8 : 50% NR 4'hF : 0% NR

Edge Enhancement

Edge enhancement function controls the sharpness of input image. The function is enabled by setting edge_en = 1’b1. Control factors for edge enhancement are edge gain, edge threshold, and edge maximum value.

- Edge gain
  Edge is intensified directly by setting high edge gain values. edge_pgain and edge_mgain affects positive edge gain and negative edge gain respectively.

- Edge threshold

Threshold can be set to exclude edge with certain level to be excluded from edge enhancement process. Edge value smaller than edge_pth are excluded from the process for positive edge. In similar fashion, edge value smaller than edge_mth are excluded from the process for negative edge.

- Edge Max. value
  After edge threshold evaluation, maximum value clamping is proceeded. Maximum edge value for positive edge is dark_ec_pmax and for negative edge is dark_ec_mmax.

Table 29 shows registers relevant to edge enhancement functions.

Table 29 Register Table - Edge enhancement

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
edge_en	D	67	[3]	1'b1	RW	aev	Edge enhancement enable 1'b0 : disable 1'b1 : enable
edge_pgain	D	DE	[7:0]	0x10	RW	aev	Positive max edge clamp gain
edge_mgain	D	DF	[7:0]	0x20	RW	aev	Negative max edge clamp gain
dark_ec_pmax	D	E2	[7:0]	0x80	RW	aev	Current edge clamp plus max filter fitting value
dark_ec_mmax	D	E3	[7:0]	0x80	RW	aev	Current edge clamp minus max filter fitting value
dark_ec_pth	D	E0	[7:0]	0x10	RW	aev	Current edge clamp plus TH filter fitting value
dark_ec_mth	D	E1	[7:0]	0x10	RW	aev	Current edge clamp minus TH filter fitting value

Color Correction (CCR)

CCR function utilizes 3 by 3 matrix multiplication to correct RGB color. dark_ccr register reduces the effectiveness of CCR. As dark_ccr value increases, degree of CCR decreases.

$$\begin{bmatrix} R` \\ G` \\ B` \end{bmatrix} = \begin{bmatrix} ccr\_m11 & ccr\_m12 & ccr\_m13 \\ ccr\_m21 & ccr\_m22 & ccr\_m23 \\ ccr\_m31 & ccr\_m32 & ccr\_m33 \end{bmatrix} X \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

Figure 27 CCR matrix

Table 30 shows registers relevant to CCR functions.

Table 30 Register Table - CCR

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
ccr_en	D	66	[1]	1'b1	RW	aev	Color correction enable 1'b0 : disable 1'b1 : enable

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
ccr_m11	E	31	[7:0]	0x31	RW	aev	Color correction matrix value 1
ccr_m12	E	32	[7:0]	0xA6	RW	aev	Color correction matrix value 2
ccr_m13	E	33	[7:0]	0x82	RW	aev	Color correction matrix value 3
ccr_m21	E	34	[7:0]	0x90	RW	aev	Color correction matrix value 4
ccr_m22	E	35	[7:0]	0x44	RW	aev	Color correction matrix value 5
ccr_m23	E	36	[7:0]	0x94	RW	aev	Color correction matrix value 6
ccr_m31	E	37	[7:0]	0x84	RW	aev	Color correction matrix value 7
ccr_m32	E	38	[7:0]	0x9E	RW	aev	Color correction matrix value 8
ccr_m33	E	39	[7:0]	0x43	RW	aev	Color correction matrix value 9
dark_ccr	E	3A	[7:0]	0x00	RW	aev	Current color correction fitting value

RGB Gamma

RGB gamma function performs non-linear operation on RGB color after CCR. RGB gamma function uses a fixed gamma reference curve(gamma=1) and a configurable gamma reference curve: gamma curve0 and gamma curve1. Depending on the dark_rgb_gm setting level, the system determines which curve to apply for RGB (refer to Figure 28). RGB gamma is enabled by setting rgbgm_en = 1'b1.

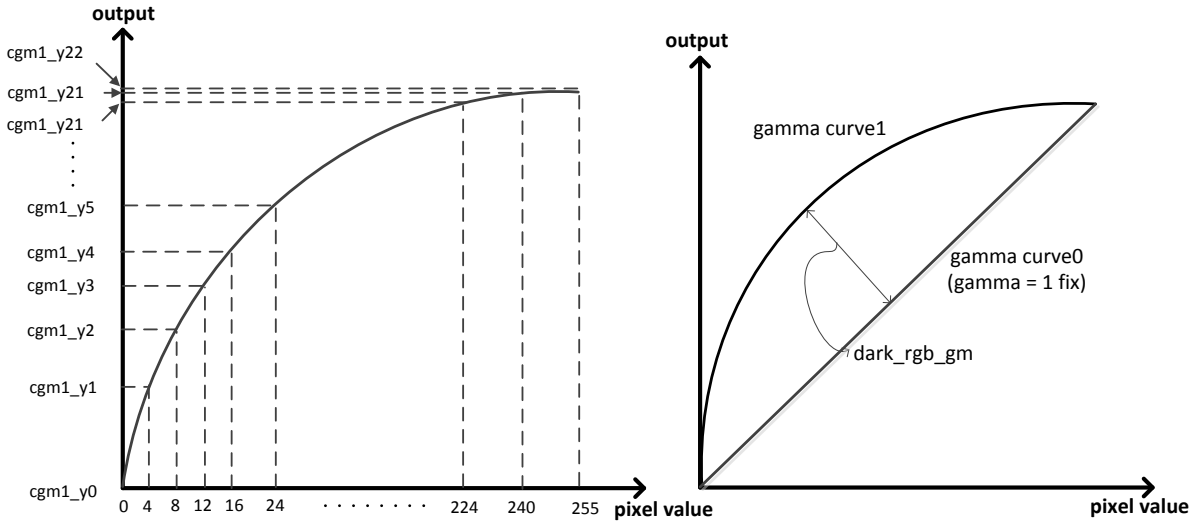


Figure 28 Gamma curve fitting of RGB gamma

Table 31 shows registers relevant to RGB gamma functions.

Table 31 Register Table - RGB gamma

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
cgm_en	D	67	[7]	1'b1	RW	aev	RGB gamma enable 1'b0 : disable 1'b1 : enable

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
Y/C gm fitting	O	69	[3]	1'b1	RW	autov	Y/RGB gamma fitting enable 1'b0 : disable 1'b1 : enable
gm1_y0	E	04	[7:0]	0x00	RW		gamma1 coefficient 0
gm1_y1	E	05	[7:0]	0x3B	RW		gamma1 coefficient 1
gm1_y2	E	06	[7:0]	0x49	RW		gamma1 coefficient 2
gm1_y3	E	07	[7:0]	0x52	RW		gamma1 coefficient 3
gm1_y4	E	08	[7:0]	0x5A	RW		gamma1 coefficient 4
gm1_y5	E	09	[7:0]	0x60	RW		gamma1 coefficient 5
gm1_y6	E	0A	[7:0]	0x65	RW		gamma1 coefficient 6
gm1_y7	E	0B	[7:0]	0x6A	RW		gamma1 coefficient 7
gm1_y8	E	0C	[7:0]	0x6F	RW		gamma1 coefficient 8
gm1_y9	E	0D	[7:0]	0x76	RW		gamma1 coefficient 9
gm1_y10	E	0E	[7:0]	0x7D	RW		gamma1 coefficient 10
gm1_y11	E	0F	[7:0]	0x83	RW		gamma1 coefficient 11
gm1_y12	E	10	[7:0]	0x88	RW		gamma1 coefficient 12
gm1_y13	E	11	[7:0]	0x92	RW		gamma1 coefficient 13
gm1_y14	E	12	[7:0]	0x9A	RW		gamma1 coefficient 14
gm1_y15	E	13	[7:0]	0xA1	RW		gamma1 coefficient 15
gm1_y16	E	14	[7:0]	0xA8	RW		gamma1 coefficient 16
gm1_y17	E	15	[7:0]	0xBE	RW		gamma1 coefficient 17
gm1_y18	E	16	[7:0]	0xCF	RW		gamma1 coefficient 18
gm1_y19	E	17	[7:0]	0xDD	RW		gamma1 coefficient 19
gm1_y20	E	18	[7:0]	0xEA	RW		gamma1 coefficient 20
gm1_y21	E	19	[7:0]	0xF5	RW		gamma1 coefficient 21
gm1_y22	E	1A	[7:0]	0xFF	RW		gamma1 coefficient 22
dark_rgb_gm	E	66	[7:0]	0x00	RW	aev	Current RGB gamma fitting value

De-color

De-color function reduces chroma level and is enabled by setting dc_en = 1’b1. High dark_dc level results in achromatic color. The maximum value of dark_dc is 0x3F.

Table 32 shows registers relevant to decolor functions.

Table 32 Register Table - De-color

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
dc_en	D	6C	[2]	1'b1	RW	aev	De-color enable 1'b0 : disable 1'b1 : enable
dark_dc	E	6B	[7:0]	0x00	RW	aev	Current de-color dark filter fitting value

Y Gamma

Y gamma function performs non-linear operation on Y component. Y gamma function uses a fixed gamma reference curve(gamma=1) and a configurable gamma reference curve: gamma curve0 and gamma curve1. Depending on the dark_y_gm setting level, the system determines which curve to apply for Y (refer to Figure 29). Y gamma is enabled by setting ygm_en = 1'b1.

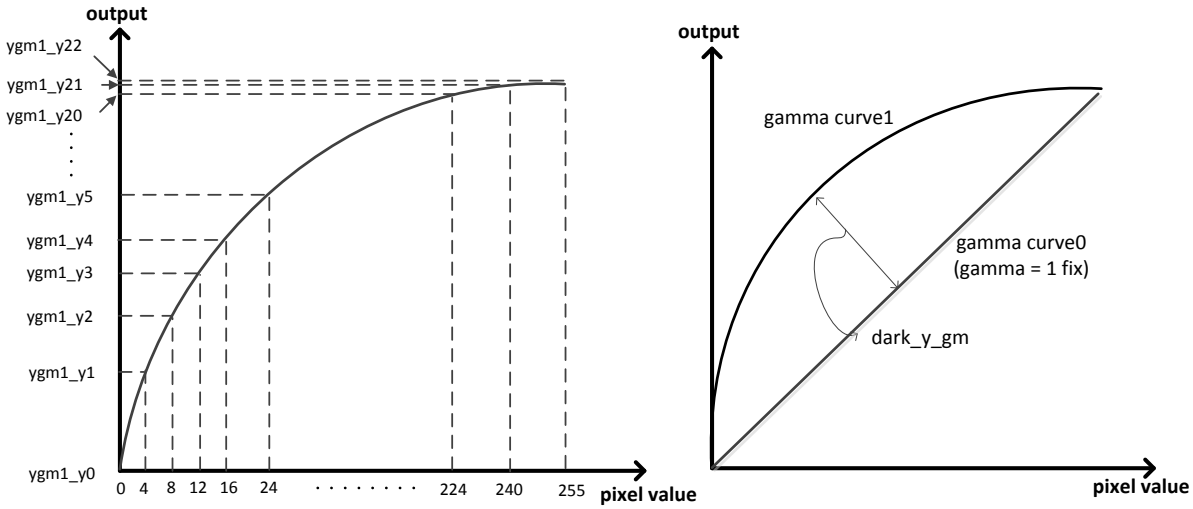


Figure 29 Gamma curve fitting of Y gamma

Table 33 shows registers relevant to Y gamma functions.

Table 33 Register Table - Y Gamma

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
ygm_en	D	67	[6]	1'b1	RW	aev	Y gamma enable 1'b0 : disable 1'b1 : enable
Y/C gm fitting	O	69	[3]	1'b1	RW	autov	Y/RGB gamma fitting enable 1'b0 : disable 1'b1 : enable
gm1_y0	E	04	[7:0]	0x00	RW		gamma1 coefficient 0
gm1_y1	E	05	[7:0]	0x3B	RW		gamma1 coefficient 1
gm1_y2	E	06	[7:0]	0x49	RW		gamma1 coefficient 2
gm1_y3	E	07	[7:0]	0x52	RW		gamma1 coefficient 3
gm1_y4	E	08	[7:0]	0x5A	RW		gamma1 coefficient 4
gm1_y5	E	09	[7:0]	0x60	RW		gamma1 coefficient 5
gm1_y6	E	0A	[7:0]	0x65	RW		gamma1 coefficient 6
gm1_y7	E	0B	[7:0]	0x6A	RW		gamma1 coefficient 7
gm1_y8	E	0C	[7:0]	0x6F	RW		gamma1 coefficient 8
gm1_y9	E	0D	[7:0]	0x76	RW		gamma1 coefficient 9

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
gm1_y10	E	0E	[7:0]	0x7D	RW		gamma1 coefficient 10
gm1_y11	E	0F	[7:0]	0x83	RW		gamma1 coefficient 11
gm1_y12	E	10	[7:0]	0x88	RW		gamma1 coefficient 12
gm1_y13	E	11	[7:0]	0x92	RW		gamma1 coefficient 13
gm1_y14	E	12	[7:0]	0x9A	RW		gamma1 coefficient 14
gm1_y15	E	13	[7:0]	0xA1	RW		gamma1 coefficient 15
gm1_y16	E	14	[7:0]	0xA8	RW		gamma1 coefficient 16
gm1_y17	E	15	[7:0]	0xBE	RW		gamma1 coefficient 17
gm1_y18	E	16	[7:0]	0xCF	RW		gamma1 coefficient 18
gm1_y19	E	17	[7:0]	0xDD	RW		gamma1 coefficient 19
gm1_y20	E	18	[7:0]	0xEA	RW		gamma1 coefficient 20
gm1_y21	E	19	[7:0]	0xF5	RW		gamma1 coefficient 21
gm1_y22	E	1A	[7:0]	0xFF	RW		gamma1 coefficient 22
dark_y_gm	E	2E	[7:0]	0x00	RW	aev	Current Y gamma fitting value

Contrast

Contrast function performs linear operation on Y component. This function acts by setting two points. (refer to Figure 30)

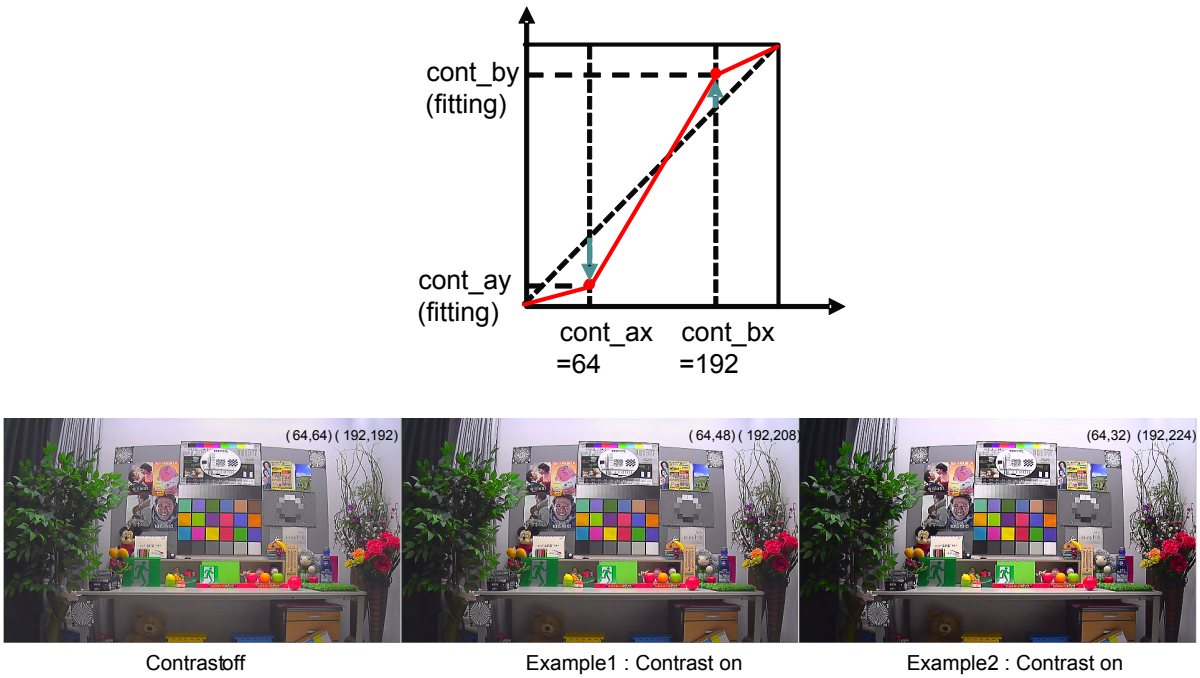


Figure 30 ISP_cont

Table 34 shows registers relevant to contrast functions.

Table 34 Register Table - ISP Contrast

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
y_cont_ay	E	73	[7:0]	0xC0	RW	aev	contrast 1st point Y axis
y_cont_by	E	74	[7:0]	0xC0	RW	aev	contrast 2nd point Y axis

Y Offset

Y offset is the brightness offset of the system. The number representation of Y offset is 2's complement. Y offset level can be adjusted by changing ybrightness register.

Table 35 shows registers relevant to Y offset functions.

Table 35 Register Table - Y offset

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
ybrightness	E	72	[7:0]	0x00	RW	aev	Current Y brightness fitting value

Color Saturation

Color saturation functions performs 2 by 2 matrix operation on chroma domain (Cb/Cr) to adjust hue and saturation. user_cs register is additional multiplication coefficient parameter for cs11 and cs22 components.

$$\begin{bmatrix} Cb` \\ Cr` \end{bmatrix} = \begin{bmatrix} user\_cs \times cs11 & cs12 \\ cs21 & user\_cs \times cs22 \end{bmatrix} X \begin{bmatrix} Cb \\ Cr \end{bmatrix}$$

Figure 31 Color saturation matrix

Table 36 shows registers relevant to color saturation functions.

Table 36 Register Table - Color saturation

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
cs11	E	76	[7:0]	0x20	RW	aev	Color saturation matrix value 1
cs12	E	77	[7:0]	0x80	RW	aev	Color saturation matrix value 2
cs21	E	78	[7:0]	0x80	RW	aev	Color saturation matrix value 3
cs22	E	79	[7:0]	0x20	RW	aev	Color saturation matrix value 4
user_cs	E	7A	[7:0]	0x28	RW		User CS gain

Flicker Detection

PV4109K includes flicker detection feature. Generally, operating frequency of light source is either 60 Hz or 50 Hz. Therefore, PV4109K's flicker detection feature is pre-configured states with 60 Hz light source frequency as state A and 50 Hz light source frequency as state B.
Three different flicker detection mode is available in PV4109K: auto mode, manual A mode, and manual B mode.

- Auto mode(fd_en = 1'b1, manual_A = 1'b0, manual_B = 1'b0)
  When flicker in image is detected, current state is toggled. In other word, current state is switched to the other state.

- manual_A mode(fd_en = 1'b0, manual_A = 1'b1, manual_B = 1'b0)
  Manual A mode puts flicker detection state in state A regardless of flicker. Factory setting of PV4109K is configured for 60 Hz light source.

- manual_B mode(fd_en = 1'b0, manual_A = 1'b0, manual_B = 1'b1)
  Manual B mode puts flicker detection state in state B regardless of flicker. Factory setting of PV4109K is configured for 50 Hz light source.

Table 37 shows registers relevant to flicker detection.

Table 37 Register Table - Flicker detection

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
fd_en	D	55	[6]	1'b0	RW		Flicker detection enable 1'b0 : disable 1'b1 : enable
fd_manual_A	D	55	[3]	1'b1	RW		manual A mode enable 1'b0 : disable 1'b1 : enable
fd_manual_B	D	55	[2]	1'b0	RW		manual B mode enable 1'b0 : disable 1'b1 : enable

AE Window Setting

AE feature gathers brightness information from 5 different sections of an image. This sections is called AE window and can be controlled by AE-window1/2/3/4/C registers.

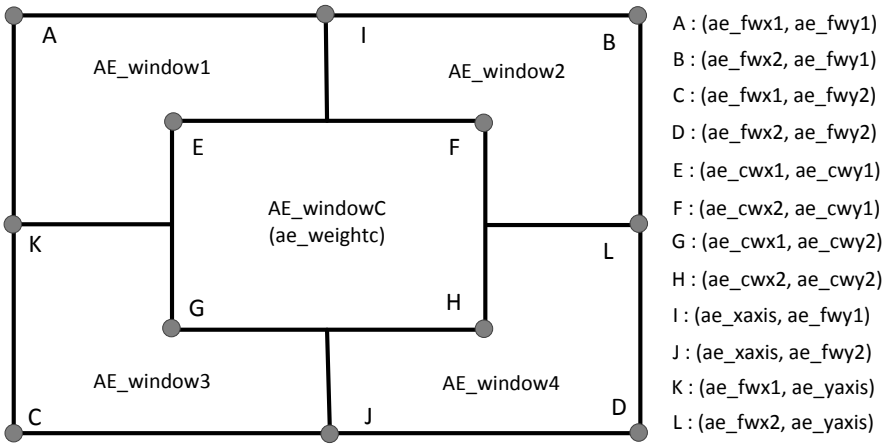


Figure 32 AE window setting

Table 38 shows registers relevant to AE window.

Table 38 Register Table - AE window setting

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
ae_fwx1_h	E	AD	[2:0]	0x00	RW		AE full window X start position High Byte
ae_fwx1_l	E	AE	[7:0]	0x04	RW		AE full window X start position Low Byte
ae_fwx2_h	E	AF	[2:0]	0x05	RW		AE full window X stop position High Byte
ae_fwx2_l	E	B0	[7:0]	0x04	RW		AE full window X stop position Low Byte
ae_fwy1_h	E	B1	[2:0]	0x00	RW		AE full window Y start position High Byte
ae_fwy1_l	E	B2	[7:0]	0x04	RW		AE full window Y start position Low Byte
ae_fwy2_h	E	B3	[2:0]	0x02	RW		AE full window Y stop position High Byte
ae_fwy2_l	E	B4	[7:0]	0xD4	RW		AE full window Y stop position Low Byte
ae_cwx1_h	E	B5	[2:0]	0x01	RW		AE center window X start position High Byte
ae_cwx1_l	E	B6	[7:0]	0xAD	RW		AE center window X start position Low Byte
ae_cwx2_h	E	B7	[2:0]	0x03	RW		AE center window X stop position High Byte
ae_cwx2_l	E	B8	[7:0]	0x5A	RW		AE center window X stop position Low Byte
ae_cwy1_h	E	B9	[2:0]	0x00	RW		AE center window Y start position High Byte
ae_cwy1_l	E	BA	[7:0]	0xF2	RW		AE center window Y start position Low Byte
ae_cwy2_h	E	BB	[2:0]	0x01	RW		AE center window Y stop position High Byte
ae_cwy2_l	E	BC	[7:0]	0xE5	RW		AE center window Y stop position Low Byte
ae_xaxis_h	E	BD	[2:0]	0x02	RW		AE window X axis High Byte
ae_xaxis_l	E	BE	[7:0]	0x84	RW		AE window X axis Low Byte

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
ae_yaxis_h	E	BF	[2:0]	0x01	RW		AE window Y axis High Byte
ae_yaxis_l	E	C0	[7:0]	0x6C	RW		AE window Y axis Low Byte

AE Auto/Manual Mode Control

There are auto mode and manual mode in AE operation mode. Normally, it operates in auto mode. Auto/manual mode operates as follows according to exposure_mode [1:0] setting.

- exposure_mode[1:0] = 2'b00(auto mode)
  The exposure value changes according to the image characteristic. Inttime, globalgain, and digitalgain are calculated by the exposure value.
- exposure_mode[1:0] = 2'b01(manual1 : exposure control)
  The user can set the exposure directly. Inttime, globalgain, and digitalgain are calculated by the exposure value.
- exposure_mode[1:0] = 2'b10(manual2 : external gain control)
  The applied inttime corresponds to ext_inttime, and the applied globalgain corresponds to ext_glbg. User can set ext_inttime, ext_glbg directly.
- exposure_mode[1:0] = 2'b11(manual3 : inttime, gain control)
  User directly controls inttime, globalgain, and digitalgain.

Table 39 Register Table - AE manual

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
exposure_mode	O	08	[7:0]	0x00	RW	autov	Exposure mode selection
exposure_t	O	25	[7:0]	0x00	RW	autov	Exposure value 1
exposure_h	O	26	[7:0]	0x01	RW	autov	Exposure value 2
exposure_m	O	27	[7:0]	0x40	RW	autov	Exposure value 3
exposure_l	O	28	[7:0]	0x00	RW	autov	Exposure value 4
ext_inttime_h	O	20	[7:0]	0x00	RW	autov	Manual integration time High Byte @ external AE mode
ext_inttime_m	O	21	[7:0]	0x80	RW	autov	Manual integration time Middle Byte @ external AE mode
ext_inttime_l	O	22	[7:0]	0x00	RW	autov	Manual integration time Low Byte @ external AE mode
ext_glbg_h	O	23	[7:0]	0x01	RW	autov	Manual analog gain High Byte @ external AE mode
ext_glbg_l	O	24	[7:0]	0x00	RW	autov	Manual analog gain Low Byte @ external AE mode
inttime_h	B	6E	[7:0]	0x01	RW	wr_en	Integration time (line) High Byte
inttime_m	B	6F	[7:0]	0x40	RW	wr_en	Integration time (line) Low Byte
inttime_l	B	70	[7:0]	0x00	RW	wr_en	Iinteration time (column)
globalgain	B	71	[7:0]	0x00	RW	wr_en	Analog gain

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
isp_dgain	D	E6	[7:0]	0x40	RW	aev	Digital gain

AWB Window Setting

PV4109K can select specific region of an image to perform AWB process. This region is called AWB window and, normally, has the same size as ISP window for optimal operation.

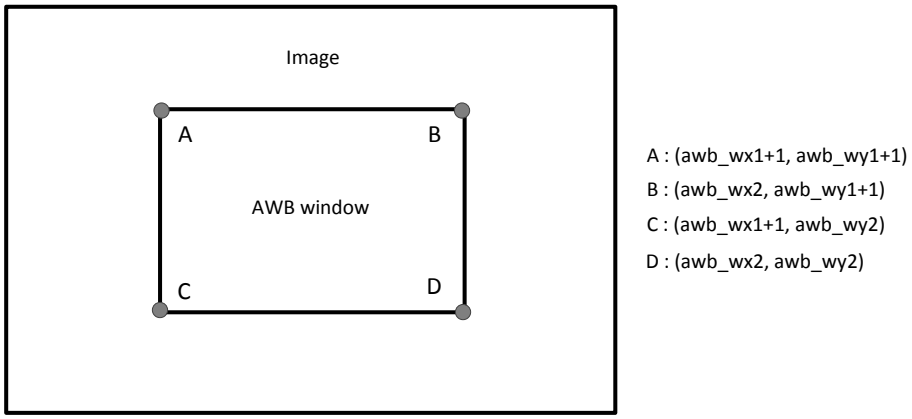


Figure 33 AWB window setting

Table 40 shows registers relevant to AWB window.

Table 40 Register Table - AWB window setting

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
awb_wx1_h	E	C1	[2:0]	0x00	RW		AWB window X start position High Byte
awb_wx1_l	E	C2	[7:0]	0x04	RW		AWB window X start position Low Byte
awb_wx2_h	E	C3	[2:0]	0x05	RW		AWB window X stop position High Byte
awb_wx2_l	E	C4	[7:0]	0x04	RW		AWB window X stop position Low Byte
awb_wy1_h	E	C5	[2:0]	0x00	RW		AWB window Y start position High Byte
awb_wy1_l	E	C6	[7:0]	0x04	RW		AWB window Y start position Low Byte
awb_wy2_h	E	C7	[2:0]	0x02	RW		AWB window Y stop position High Byte
awb_wy2_l	E	C8	[7:0]	0xD4	RW		AWB window Y stop position Low Byte

Parking Guide Line Control

Since the image data related to the parking guide is stored in PV4109K, the data of the external ROM is not necessary.

Figure 34 represents the parking guide line. If pg_enable is 1'b1, the parking guide line is enabled.

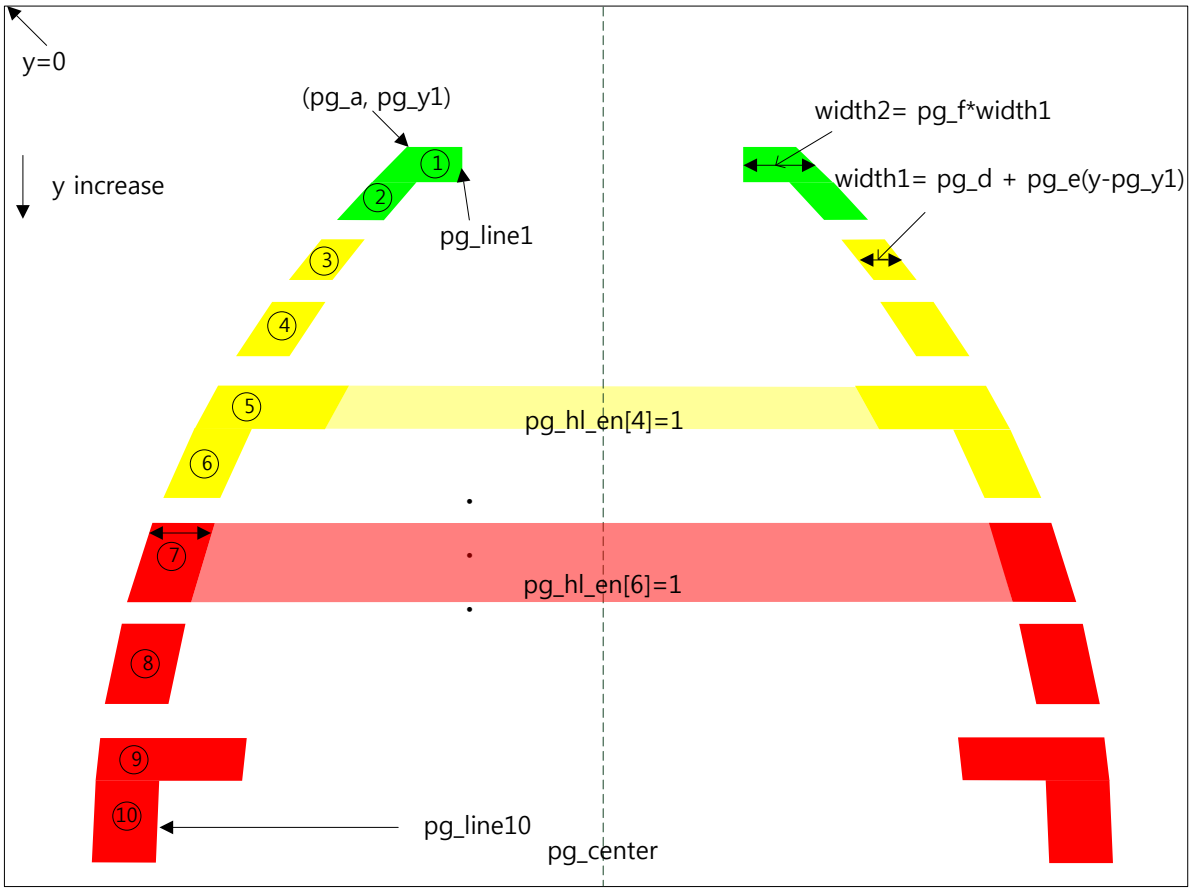


Figure 34 Parking guide line

- pg_yt
  It shows the boundary between the straight line and the curve of the embedded parking guide line.

- pg_y1~10
  Embedded parking guide lines can be represented by up to 10 dashed lines. pg_y1 ~ 10 represent y start coordinates of 10 dashed lines. pg_y2 / 10 is the relative coordinate with pg_y1.

- pg_a
  pg_a is the starting x-coordinate of the embedded parking guide line. The x-coordinate is 2*pg_a and must be at least 1.

- pg_b
  pg_b determines the overall linear slope of the embedded parking guide line.

- pg_c

Pg_c indicates the degree of bending of the curve of the embedded parking guide line

- pg_d
  pg_d is the initial line width of the embedded parking guide line. The line width should be at least 4.
- pg_e
  The line width of the embedded parking guide line increases as it goes downward. pg_e adjusts the increment of the line width.
- pg_f
  pg_f determines the size of the long line width. The "long line width" is pg_f*"short line width".
- pg_line1~10
  Pg_line1~10 determine the height of each dotted line.
- pg_line_info1~10
  - pg_line_info1~10[3:1] : line palette 1~4 selection (pal_y/cb/cr_1~4)
  - pg_line_info1~10[0] : line width type selection (long/short)
- pg_center
  Embedded parking guide line is symmetrical about pg_center.
- pg_blink
  Parking guide line blinks every #(blink_frame)frame.
- pg_hl_en
  Parking guide horizontal line enable.

Table 41 Register Table - Parking guide line

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
pg_enable	A	BC	[3]	1'b0	RW		PG enable 1'b0 : disable 1'b1 : enable
pg_blink	A	BF	[5]	1'b0	RW	aev	PG blink enable 1'b0 : disable 1'b1 : enable
pg_hlight	A	BF	[4]	1'b0	RW	aev	PG hlight enable 1'b0 : disable 1'b1 : enable
pg_rm_ych	A	BF	[3]	1'b1	RW	aev	Remove yochul line of PG 1'b0 : disable 1'b1 : enable
pg_rm	A	BF	[2:1]	2'b00	RW	aev	pg_rm[1] : remove left side of PG 1'b0 : disable 1'b1 : enable pg_rm[0] : remove right side of PG 1'b0 : disable 1'b1 : enable
manual_chrm_zero	A	BD	[7]	1'b0	RW		Always encoder chroma signal 0'd 1'b0 : disable 1'b1 : enable

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
bw_chrm_zero	A	BD	[6]	1'b0	RW		If bwled is, encoder chroma signal 0'd 1'b0 : disable 1'b1 : enable
pg_yt	A	C0	[7:0]	0x7F	RW	aev	Control the position of straight line and curve boundary
pg_y1_h	A	C1	[2:0]	0x01	RW	aev	Parking guide line y position 1 Hgih Byte
pg_y1_l	A	C2	[7:0]	0x5A	RW	aev	Parking guide line y position 1 Low Byte
pg_y2	A	C3	[7:0]	0x04	RW	aev	Parking guide line y position 2
pg_y3	A	C4	[7:0]	0x0E	RW	aev	Parking guide line y position 3
pg_y4	A	C5	[7:0]	0x11	RW	aev	Parking guide line y position 4
pg_y5	A	C6	[7:0]	0x1A	RW	aev	Parking guide line y position 5
pg_y6	A	C7	[7:0]	0x20	RW	aev	Parking guide line y position 6
pg_y7	A	C8	[7:0]	0x07	RW	aev	Parking guide line y position 7
pg_y8	A	C9	[7:0]	0x2C	RW	aev	Parking guide line y position 8
pg_y9	A	CA	[7:0]	0x3E	RW	aev	Parking guide line y position 9
pg_y10	A	CB	[7:0]	0x0A	RW	aev	Parking guide line y position 10
pg_line1	A	CC	[6:0]	0x03	RW	aev	Parking guide line color and height control 1
pg_line2	A	CD	[6:0]	0x09	RW	aev	Parking guide line color and height control 2
pg_line3	A	CE	[6:0]	0x0C	RW	aev	Parking guide line color and height control 3
pg_line4	A	CF	[6:0]	0x12	RW	aev	Parking guide line color and height control 4
pg_line5	A	D0	[6:0]	0x18	RW	aev	Parking guide line color and height control 5
pg_line6	A	D1	[6:0]	0x06	RW	aev	Parking guide line color and height control 6
pg_line7	A	D2	[6:0]	0x21	RW	aev	Parking guide line color and height control 7
pg_line8	A	D3	[6:0]	0x33	RW	aev	Parking guide line color and height control 8
pg_line9	A	D4	[6:0]	0x09	RW	aev	Parking guide line color and height control 9
pg_line10	A	D5	[6:0]	0x1E	RW	aev	Parking guide line color and height control 10
pg_a_h	A	D6	[1:0]	0x00	RW	aev	Parking guide line Init. x position 1 High Byte
pg_a_l	A	D7	[7:0]	0xFE	RW	aev	Parking guide line Init. x position 1 Low Byte
pg_b	A	D8	[7:0]	0x44	RW	aev	The slope of parking guide line control
pg_c	A	D9	[7:0]	0x47	RW	aev	The degree of parking guide line curve control
pg_d	A	DA	[7:0]	0x07	RW	aev	Parking guide line width control
pg_e	A	DB	[7:0]	0x0C	RW	aev	Parking guide line thickness control
pg_f	A	DC	[7:0]	0x15	RW	aev	Parking guide long line width control
pg_center_h	A	DD	[2:0]	0x02	RW	aev	PG center control High Byte
pg_center_l	A	DE	[7:0]	0x80	RW	aev	PG center control Low Byte
pg_line_info1	A	DF	[3:0]	0x03	RW	aev	Parking guide line information 1
pg_line_info2	A	E0	[3:0]	0x02	RW	aev	Parking guide line information 2
pg_line_info3	A	E1	[3:0]	0x02	RW	aev	Parking guide line information 3
pg_line_info4	A	E2	[3:0]	0x04	RW	aev	Parking guide line information 4

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
pg_line_info5	A	E3	[3:0]	0x04	RW	aev	Parking guide line information 5
pg_line_info6	A	E4	[3:0]	0x05	RW	aev	Parking guide line information 6
pg_line_info7	A	E5	[3:0]	0x04	RW	aev	Parking guide line information 7
pg_line_info8	A	E6	[3:0]	0x06	RW	aev	Parking guide line information 8
pg_line_info9	A	E7	[3:0]	0x07	RW	aev	Parking guide line information 9
pg_line_info10	A	E8	[3:0]	0x06	RW	aev	Parking guide line information 10
blink_frame	A	E9	[7:0]	0x00	RW		Parking guide line blink every "blink_frame" frame
pg_hl_en_h	A	EA	[1:0]	0x00	RW	aev	Parking guide horizontal line enable High Byte
pg_hl_en_l	A	EB	[7:0]	0x00	RW	aev	Parking guide horizontal line enable Low Byte
pg_opac	A	EC	[4:0]	0x10	RW		Parking guide line opacity
pg_hl_opac	A	ED	[4:0]	0x10	RW		Parking guide horizontal line opacity
pal_y_1	A	EE	[7:0]	0x90	RW		Palette_set_1 Y
pal_cb_1	A	EF	[7:0]	0x40	RW		Palette_set_1 Cb
pal_cr_1	A	F0	[7:0]	0x31	RW		Palette_set_1 Cr
pal_y_2	A	F1	[7:0]	0xD1	RW		Palette_set_2 Y
pal_cb_2	A	F2	[7:0]	0x21	RW		Palette_set_2 Cb
pal_cr_2	A	F3	[7:0]	0x8F	RW		Palette_set_2 Cr
pal_y_3	A	F4	[7:0]	0x50	RW		Palette_set_3 Y
pal_cb_3	A	F5	[7:0]	0x61	RW		Palette_set_3 Cb
pal_cr_3	A	F6	[7:0]	0xDF	RW		Palette_set_3 Cr
pal_y_4	A	F7	[7:0]	0xEB	RW		Palette_set_4 Y
pal_cb_4	A	F8	[7:0]	0xEB	RW		Palette_set_4 Cb
pal_cr_4	A	F9	[7:0]	0xEB	RW		Palette_set_4 Cr

PVI Encoder

PVI encoder receives input from digital video and outputs it on all kinds of analog HD video such as HD-CVI/HDT/HDA. It takes H/V Sync data, Luminance, and Chromance data from the Digital Video input and converts it to PVI video.

Color Subcarrier Selection

The PVI encoder can change the color subcarrier of several outputs by changing the register of Table 42, as shown in Table 43.

Table 42 Register Table - Subcarrier register

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
FSC_SEL	I	58	[7:0]	0x72	RW		Color subcarrier selection [6:4] : FSC_MD_SEL [2:0] : FSC_CLK_SEL

Table 43 Register Table - Subcarrier selection

FSC_MD_SEL FSC_CLK_SEL	0~3 (HD-PVI)	5 (HD-CVI)	6 (HD-HDT)	7 (HD-HDA)
0	x	x	x	x
1	x	x	x	x
2	720p@30	720p@30	x	720p@30
3	720p@25	x	x	720p@25
4	x	x	x	x
5	x	x	x	x
6	x	x	720p@30	x
7	x	x	720p@25	x

Video Tunning

Table 44 is a list of image-related tuning registers.

Table 44 Register Table - Video tunning

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
TST_IN_EN	I	11	[7]	1'b0	RW		Selection Test Pattern Enable 1'b0 : Normal Mode 1'b1 : Test Pattern Enable
TST_PT_SEL	I	13	[7:4]	4'b1110	RW		Selection of Test Pattern 4'd0 : Black 4'd1 : Blue 4'd2 : Red 4'd3 : Magenta 4'd4 : Green 4'd5 : Cyan 4'd6 : Yellow 4'd7 : White 4'd8 : Color Bar 4'd9 : Gray Bar 4'd10 : Hatch Pattern 4'd11 : Center Box Pattern 4'd12 : H Sweep Pattern 4'd13 : H/V Frequency Sweep Pattern 4'd14 : Complex Mixed Pattern0 4'd15 : Complex Mixed Pattern1
CONT_EN	I	13	[3]	1'b0	RW		Selection Contrast Control Enable 1'b0 : Bypass 1'b1 : Enable
BRT_EN	I	13	[2]	1'b0	RW		Selection Brightness Control Enable 1'b0 : Bypass 1'b1 : Enable
SAT_EN	I	13	[1]	1'b0	RW		Selection Saturation Control Enable 1'b0 : Bypass 1'b1 : Enable
HUE_EN	I	13	[0]	1'b0	RW		Selection Hue Control Enable 1'b0 : Bypass 1'b1 : Enable
CONT	I	14	[7:0]	0x80	RW		Contrast control value
BRT	I	15	[7:0]	0x80	RW		Brightness control value
SAT	I	16	[7:0]	0x80	RW		Color saturation control value
HUE	I	17	[7:0]	0x80	RW		Hue control value

Video Timing Tunning

Table 45 is a list of registers related to video timing.

Table 45 Register Table - PVI

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
Status	I	08	[7:0]		RO		Monitoring of PVI encoder internal status
Hsize	I	09	[7:0]		RO		Monitoring of PVI encoder internal status
Vsize	I	0A	[7:0]		RO		Monitoring of PVI encoder internal status
HVsize	I	0B	[7:0]		RO		Monitoring of PVI encoder internal status
Rev_ID	I	0F					Read Only Register 8'h10 : PV4109 PVI Tx IP update
ENC_LIM_EN	I	10	[4]	1'b0	RW		Enable Active Data Range Limitation 1'b0 : No Limit (1 ~ 254 Range) 1'b1 : 16 ~ 240 Range
ENC_CBCR_INV	I	11	[6]	1'b0	RW		Selection CB/CR Swapping Enable 1'b0 : Normal 1'b1 : Cb/Cr Swapping
ENC_FLD_POL	I	11	[5]	1'b0	RW		Selection Field Polarity Inversion 1'b0 : Normal 1'b1 : Field Polarity Inversion
ENC_YC_INV	I	11	[4]	1'b0	RW		Selection Y/C Swapping Enable 1'b0 : Normal 1'b1 : Y/C Swapping
TST_MODE	I	11	[3:0]	4'b0110	RW		Selection Mode for Test Pattern 4'd0 : 1280x720p@30Hz (37.125M) : 1650 x 750 4'd1 : 1280x720p@25Hz (37.125M) : 1980 x 750
CSC_MD	I	12	[1:0]	2'b10	RW		Selection Color Space Conversion Mode [1] : Color Space Conversion Enable 1'b0 : Bypass for CSC 1'b1 : Enable for CSC [0] : Color Space Conversion Mode 1'b0 : BT 601 to BT709 Conversion 1'b1 : BT709 to BT601 Conversion
INT_MD	I	18	[7]	1'b0	RW		Selection Interlace Mode 1'b0 : Progressive for HD 1'b1 : Interlace for SD
PHALT	I	18	[6]	1'b0	RW		Selection Phase Alternation for Color Burst 1'b0 : No Phase Alternation 1'b1 : Enable Phase Alternation
PDRST	I	18	[5]	1'b0	RW		Phase Alternation Clear Enable 1'b0 : No Reset 1'b1 : Enable Phase Reset @ Every 4 Frame
HS_STRT_DLY_L	I	1A	[7:0]	0x00	RW		Hsync start delay Low Byte
HS_STRT_DLY_H	I	1B	[5:0]	0x00	RW		Hsync start delay High Byte
FSC_SEL	I	58	[7:0]	0x72	RW		Color subcarrier selection

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							[6:4] : FSC_MD_SEL [2:0] : FSC_CLK_SEL
FLT_MD	I	5C	[7:0]	0x82	RW		Y/C filter characteristic selection
CHROMA_OFF	I	66	[6]	1'b0	RW		Selection Chroma Off Mode 1'b0 : Normal 1'b1 : Chroma Off

Electrical Characteristics

PV4109K does not have tolerant input pads. The input signal must have HVDD power level for stable operation. If the power of input signal is higher than the recommended level, leakage current may flow via short circuit path in the input pads.

DC Characteristics

Absolute maximum ratings [1]
AVDD supply voltage : -0.3 [V] to 4.0 [V]
CVDD supply voltage : -0.3 [V] to 4.0 [V]
HVDD supply voltage : -0.3 [V] to 4.0 [V]
DVDD supply voltage : -0.3 [V] to 1.8 [V]
DC VTG at any input pin : -0.3 [V] to HVDD+0.3 [V]
DC VTG at any output pin : -0.3 [V] to HVDD+0.3 [V]
Storage temperature : -40 [^{o}C] to + 125 [^{o}C]

Table 46 DC characteristics

Symbol	Descriptions	Min	Typ	Max	Unit
AVDD	Analog VDD(AVDD) voltage relative to GND(AGND) level	2.97	3.3	3.63	[V]
HVDD	High VDD(HVDD) voltage relative to GND(HGND) level	2.97	3.3	3.63	[V]
RVDD	Analog VDD2(RVDD) voltage relative to GND(RGND) level	2.97	3.3	3.63	[V]
DVDD	Digital VDD(DVDD) voltage relative to GND(DGND) level	1.08	1.2	1.32	[V]
I_{DDD}	HVDD=3.3 [V] @ HDA	-	27	44	[mA]
	AVDD, RVDD=3.3 [V] @ HDA	-	11	13	
	DVDD=1.2 [V] @ HDA	-	32	60	
	HVDD=3.3 [V] @ DVP	-	18	41	
	AVDD, RVDD=3.3 [V] @ DVP	-	10	12	
	DVDD=1.2 [V] @ DVP	-	24	47	
I_{DDS}	Standby supply current	-	0.15	6.1	[mA]
V_{IL1}	Input voltage low level	-	-	HVDD*0.3	[V]
V_{IH1}	Input voltage high level	HVDD*0.7	-	-	[V]
V_{IL2}	Input voltage low level for rClk, rData.	-	-	HVDD*0.3	[V]
V_{IH2}	Input voltage high level for rClk, rData .	HVDD*0.7	-	-	[V]
C_{IN}	Input pin capacitance	-	-	10	[pF]
V_{OL1}	Output voltage low	-	-	HVDD*0.2	[V]
V_{OH1}	Output voltage high	HVDD*0.8	-	-	[V]
V_{OL2}	Output voltage low level for rClk, rData.	-	-	HVDD*0.2	[V]
V_{OH2}	Output voltage high level for rData.	HVDD*0.8	-	-	[V]

[1]Excessive stresses may cause permanent damage to the device.

Symbol	Descriptions	Min	Typ	Max	Unit
I_{IN}	Input leakage current	-10	-	10	[uA]
I_{OT}	Output leakage current	-10	-	10	[uA]

AC Characteristics

Table 47 2-wire serial interface characteristics

Symbol	Descriptions	Min	Typ	Max	Unit
f_{SCL}	2-wire serial interface Clock frequency	-	-	400	kHz
T_{ic}	2-wire serial interface Clock period	2.5	-	-	us
T_{icl}	2-wire serial interface Clock low level width	1.66	-	-	us
T_{ich}	2-wire serial interface Clock high level width	0.83	-	-	us
T_{iss}	Setup time for start condition	0.83	-	-	us
T_{ihs}	Hold time for start condition	0.83	-	-	us
T_{isd}	Setup time for input data	266	-	-	ns
T_{ihd}	Hold time for input data	0	-	-	ns
T_{isp}	Setup time for stop condition	0.83	-	-	us
T_{buf}	Bus free time between a stop and a new start condition	1.66	-	-	us
T_{oaa}	Delay from SCL falling edge to output data transition	-	-	354	ns
T_r	10% to 90% rising time for SCL/SDA (load : 10pF)	-	-	46	ns
T_f	90% to 10% falling time for SCL/SDA (load : 10pF)	-	-	37	ns
R_p	SCL, SDA pull-up resistor	-	2	-	kΩ

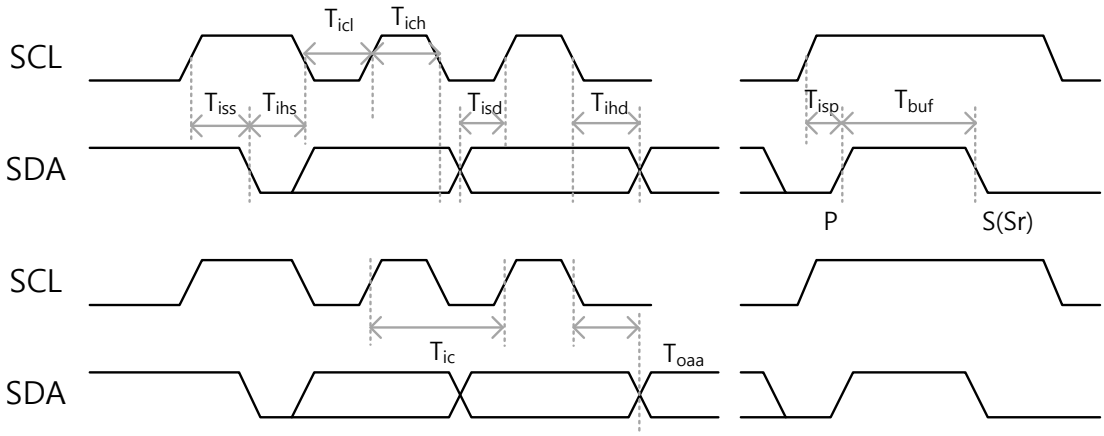


Figure 35 Timing diagram of SCL and SDA

Register Map

Table 48 Register Table - Group A

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
DeviceID_H	A	00	[7:0]	0x41	RO		Device ID High Byte
DeviceID_L	A	01	[7:0]	0x09	RO		Device ID Low Byte
bank	A	03	[7:0]	0x00	RW		Register group selector
mirror	A	05	[1:0]	0xx	RW	aev	Image Inversion mirror[1] : vertical inversion mirror[0] : horizontal inversion
framewidth_h	A	06	[2:0]	0x06	RW	aev	Framewidth High Byte (must be larger than window width)
framewidth_l	A	07	[7:0]	0x71	RW	aev	Framewidth Low Byte (must be larger than window width)
frameheight_h	A	08	[1:0]	0x02	RW	aev	Frameheight High Byte (must be larger than window height)
frameheight_l	A	09	[7:0]	0xED	RW	aev	Frameheight Low Byte (must be larger than window height)
windowx1_h	A	0C	[2:0]	0x00	RW	aev	Window horizontal start point High Byte
windowx1_l	A	0D	[7:0]	0x02	RW	aev	Window horizontal start point Low Byte
windowy1_h	A	0E	[2:0]	0x00	RW	aev	Window vertical start point High Byte
windowy1_l	A	0F	[7:0]	0x02	RW	aev	Window vertical start point Low Byte
windowx2_h	A	10	[2:0]	0x05	RW	aev	Window horizontal end point High Byte
windowx2_l	A	11	[7:0]	0x02	RW	aev	Window horizontal end point Low Byte
windowy2_h	A	12	[2:0]	0x02	RW	aev	Window vertical end point High Byte
windowy2_l	A	13	[7:0]	0xD2	RW	aev	Window vertical end point Low Byte
vsyncstartrow_f0_h	A	14	[4:0]	0x00	RW	aev	Vsync generation row 0 start point High Byte
vsyncstartrow_f0_l	A	15	[7:0]	0x0F	RW	aev	Vsync generation row 0 start point Low Byte
vsyncstoprow_f0_h	A	16	[4:0]	0x02	RW	aev	Vsync generation row 0 stop point High Byte
vsyncstoprow_f0_l	A	17	[7:0]	0xDF	RW	aev	Vsync generation row 0 stop point Low Byte
vsynccolumn_h	A	18	[4:0]	0x00	RW	aev	Vsync generation column point High Byte
vsynccolumn_l	A	19	[7:0]	0x00	RW	aev	Vsync generation column point Low Byte
sync_control_0	A	1C	[7:0]	0x00	RW		Sync control 0
sync_control_1	A	1D	[7:0]	0x02	RW		Sync control 1
sync_blankEAV	A	1E	[7:0]	0xB6	RW		blank EAV for frame data
sync_blankSAV	A	1F	[7:0]	0xAB	RW		blank SAV for frame data
sync_activeEAV	A	20	[7:0]	0x9D	RW		active EAV for frame data
sync_activeSAV	A	21	[7:0]	0x80	RW		active SAV for frame data
sync_CCIR_FF	A	22	[7:0]	0xFF	RW		SMPTE blank data format
sync_CCIR_00	A	23	[7:0]	0x00	RW		SMPTE blank data format
sync_CCIR_80	A	24	[7:0]	0x80	RW		SMPTE blank data format

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
sync_CCIR_10	A	25	[7:0]	0x10	RW		SMPTE blank data format
sync_data_min	A	26	[7:0]	0x01	RW		SMPTE data min value
sync_data_max	A	27	[7:0]	0xFE	RW		SMPTE data max value
init_fmask	A	29	[7:0]	0x01	RW		Initial frame masking after power on
stdby_fmask	A	2A	[7:0]	0x00	RW		Initial frame masking after standby
format	A	2E	[7:0]	0x00	RW	aev	Format control
i2c_control_1	A	35	[7:0]	0x50	RW		I2c control register 1
softreset	A	37	[0]	0x00	RW		Soft reset 1'b0 : disable 1'b1 : enable (after succesful reset value re-verts to 0)
pll_control2	A	55	[7:0]	0x72	RW		pll_control 2
pll_n_cnt	A	57	[7:0]	0x2C	RW		PLL multiplication factor
pll_r_cnt	A	58	[4:0]	0x04	RW		PLL division factor
clkdiv1	A	59	[7:0]	0x68	RW		Clock divider 1
clkdiv4	A	5C	[7:0]	0x0C	RW		Clock divider 4
pad_control1	A	5F	[7:0]	0x04	RW		Pad control 1
pad_control2	A	60	[7:0]	0x00	RW		Pad control 2
pad_control3	A	61	[7:0]	0x00	RW		Pad control 3
pad_control4	A	62	[7:0]	0x00	RW		Pad control 4
pad_control5	A	63	[7:0]	0x00	RW		Pad control 5
led_control1	A	80	[7:0]	0x00	RW		LED control 1
led_control2	A	81	[7:0]	0x01	RW		LED control 2
led_lvth1	A	82	[7:0]	0x00	RW		CdS level threshold for LED control via CdS
led_lvth2	A	83	[7:0]	0x00	RW		CdS level threshold for LED control via CdS
led_frame	A	84	[7:0]	0x80	RW		LED blink pulse width control
mirs_pw	A	85	[7:0]	0x64	RW		Moving filter control pulse width
mirs_pp	A	86	[7:0]	0xC8	RW		Moving filter control pulse period
mirs_cnt	A	87	[7:0]	0x01	RW		The number of moving filter control pulse
led_blink_frame	A	8A	[7:0]	0x00	RW		LED blinks per # frame
mirs_pad_en	A	8B	[0]	0x00	RW		MIRS pad enable
spi_osd_control0	A	BC	[7:0]	0xx	RW		SPI OSD control 0
spi_osd_control1	A	BD	[7:0]	0x01	RW		SPI OSD control 1
pg_control0	A	BF	[7:0]	0x08	RW	aev	Parking guide control 0
pg_yt	A	C0	[7:0]	0x7F	RW	aev	Control the position of straight line and curve boundary
pg_y1_h	A	C1	[2:0]	0x01	RW	aev	Parking guide line y position 1 Hgih Byte
pg_y1_l	A	C2	[7:0]	0x5A	RW	aev	Parking guide line y position 1 Low Byte
pg_y2	A	C3	[7:0]	0x04	RW	aev	Parking guide line y position 2

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
pg_y3	A	C4	[7:0]	0x0E	RW	aev	Parking guide line y position 3
pg_y4	A	C5	[7:0]	0x11	RW	aev	Parking guide line y position 4
pg_y5	A	C6	[7:0]	0x1A	RW	aev	Parking guide line y position 5
pg_y6	A	C7	[7:0]	0x20	RW	aev	Parking guide line y position 6
pg_y7	A	C8	[7:0]	0x07	RW	aev	Parking guide line y position 7
pg_y8	A	C9	[7:0]	0x2C	RW	aev	Parking guide line y position 8
pg_y9	A	CA	[7:0]	0x3E	RW	aev	Parking guide line y position 9
pg_y10	A	CB	[7:0]	0x0A	RW	aev	Parking guide line y position 10
pg_line1	A	CC	[6:0]	0x03	RW	aev	Parking guide line color and height control 1
pg_line2	A	CD	[6:0]	0x09	RW	aev	Parking guide line color and height control 2
pg_line3	A	CE	[6:0]	0x0C	RW	aev	Parking guide line color and height control 3
pg_line4	A	CF	[6:0]	0x12	RW	aev	Parking guide line color and height control 4
pg_line5	A	D0	[6:0]	0x18	RW	aev	Parking guide line color and height control 5
pg_line6	A	D1	[6:0]	0x06	RW	aev	Parking guide line color and height control 6
pg_line7	A	D2	[6:0]	0x21	RW	aev	Parking guide line color and height control 7
pg_line8	A	D3	[6:0]	0x33	RW	aev	Parking guide line color and height control 8
pg_line9	A	D4	[6:0]	0x09	RW	aev	Parking guide line color and height control 9
pg_line10	A	D5	[6:0]	0x1E	RW	aev	Parking guide line color and height control 10
pg_a_h	A	D6	[1:0]	0x00	RW	aev	Parking guide line Init. x position 1 High Byte
pg_a_l	A	D7	[7:0]	0xFE	RW	aev	Parking guide line Init. x position 1 Low Byte
pg_b	A	D8	[7:0]	0x44	RW	aev	The slope of parking guide line control
pg_c	A	D9	[7:0]	0x47	RW	aev	The degree of parking guide line curve control
pg_d	A	DA	[7:0]	0x07	RW	aev	Parking guide line width control
pg_e	A	DB	[7:0]	0x0C	RW	aev	Parking guide line thickness control
pg_f	A	DC	[7:0]	0x15	RW	aev	Parking guide long line width control
pg_center_h	A	DD	[2:0]	0x02	RW	aev	PG center control High Byte
pg_center_l	A	DE	[7:0]	0x80	RW	aev	PG center control Low Byte
pg_line_info1	A	DF	[3:0]	0x03	RW	aev	Parking guide line information 1
pg_line_info2	A	E0	[3:0]	0x02	RW	aev	Parking guide line information 2
pg_line_info3	A	E1	[3:0]	0x02	RW	aev	Parking guide line information 3
pg_line_info4	A	E2	[3:0]	0x04	RW	aev	Parking guide line information 4
pg_line_info5	A	E3	[3:0]	0x04	RW	aev	Parking guide line information 5
pg_line_info6	A	E4	[3:0]	0x05	RW	aev	Parking guide line information 6
pg_line_info7	A	E5	[3:0]	0x04	RW	aev	Parking guide line information 7
pg_line_info8	A	E6	[3:0]	0x06	RW	aev	Parking guide line information 8
pg_line_info9	A	E7	[3:0]	0x07	RW	aev	Parking guide line information 9
pg_line_info10	A	E8	[3:0]	0x06	RW	aev	Parking guide line information 10

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
blink_frame	A	E9	[7:0]	0x00	RW		Parking guide line blink every "blink_frame" frame
pg_hl_en_h	A	EA	[1:0]	0x00	RW	aev	Parking guide horizontal line enable High Byte
pg_hl_en_l	A	EB	[7:0]	0x00	RW	aev	Parking guide horizontal line enable Low Byte
pg_opac	A	EC	[4:0]	0x10	RW		Parking guide line opacity
pg_hl_opac	A	ED	[4:0]	0x10	RW		Parking guide horizontal line opacity
pal_y_1	A	EE	[7:0]	0x90	RW		Palette_set_1 Y
pal_cb_1	A	EF	[7:0]	0x40	RW		Palette_set_1 Cb
pal_cr_1	A	F0	[7:0]	0x31	RW		Palette_set_1 Cr
pal_y_2	A	F1	[7:0]	0xD1	RW		Palette_set_2 Y
pal_cb_2	A	F2	[7:0]	0x21	RW		Palette_set_2 Cb
pal_cr_2	A	F3	[7:0]	0x8F	RW		Palette_set_2 Cr
pal_y_3	A	F4	[7:0]	0x50	RW		Palette_set_3 Y
pal_cb_3	A	F5	[7:0]	0x61	RW		Palette_set_3 Cb
pal_cr_3	A	F6	[7:0]	0xDF	RW		Palette_set_3 Cr
pal_y_4	A	F7	[7:0]	0xEB	RW		Palette_set_4 Y
pal_cb_4	A	F8	[7:0]	0xEB	RW		Palette_set_4 Cb
pal_cr_4	A	F9	[7:0]	0xEB	RW		Palette_set_4 Cr
bank_m	A	FF	[7:0]	0x00	RW		Register group selector in master mode

Table 49 Register Table - Group B

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
inttime_h	B	6E	[7:0]	0x01	RW	wr_en	Integration time (line) High Byte
inttime_m	B	6F	[7:0]	0x40	RW	wr_en	Integration time (line) Low Byte
inttime_l	B	70	[7:0]	0x00	RW	wr_en	Iinteration time (column)
globalgain	B	71	[7:0]	0x00	RW	wr_en	Analog gain
wr_en	B	74	[0]	0x00	RW		Update exposure related register 1'b0 : no update 1'b1 : wr_en set
wr_en_off	B	75	[0]	0x01	RW		wr_en control register 1'b0 : wr_en enable 1'b1 : wr_en disable
real_led_data	B	E9	[7:0]		RO		Current CdS data

Table 50 Register Table - Group D

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
flicker_control1	D	55	[7:0]	0x08	RW		Flicker control
isp_func_0	D	66	[7:0]	0xF7	RW	aev	Isp function control 0
isp_func_1	D	67	[7:0]	0xC8	RW	aev	Isp function control 1
isp_func_6	D	6C	[7:0]	0x05	RW	aev	Isp function control 6
tp_control_0	D	70	[7:0]	0x00	RW		Test pattern selection
tp_control_1	D	71	[7:0]	0x00	RW		R[9:2] color for test pattern
tp_control_2	D	72	[7:0]	0x00	RW		G1[9:2] color for test pattern
tp_control_3	D	73	[7:0]	0x00	RW		G2[9:2] color for test pattern
tp_control_4	D	74	[7:0]	0x00	RW		B[9:2] color for test pattern
tp_control_5	D	75	[7:0]	0x00	RW		{R[1:0],G1[1:0],G2[1:0],B[1:0]} for test pattern
lens_scale	D	83	[7:0]	0x0C	RW		Lens shading compensation scale control
lens_x	D	84	[7:0]	0x00	RW		Lens shading compensation center horizontal control
lens_y	D	85	[7:0]	0x00	RW		Lens shading compensation center vertical control
lens_gainr	D	86	[7:0]	0x20	RW	aev	Lens shading compensation R gain
lens_gaing1	D	87	[7:0]	0x20	RW	aev	Lens shading compensation G1 gain
lens_gaing2	D	88	[7:0]	0x20	RW	aev	Lens shading compensation G2 gain
lens_gainb	D	89	[7:0]	0x20	RW	aev	Lens shading compensation B gain
wb_rgain_h	D	8F	[0]	0x00	RW	aev	Auto white balanc "R" gain High Byte
wb_rgain_l	D	90	[7:0]	0x5D	RW	aev	Auto white balanc "R" gain Low Byte
wb_ggain_h	D	91	[0]	0x00	RW	aev	Auto white balanc "G" gain High Byte
wb_ggain_l	D	92	[7:0]	0x40	RW	aev	Auto white balanc "G" gain Low Byte
wb_bgain_h	D	93	[0]	0x00	RW	aev	Auto white balanc "B" gain High Byte
wb_bgain_l	D	94	[7:0]	0x5E	RW	aev	Auto white balanc "B" gain Low Byte
wb_mrgain_h	D	96	[0]	0x00	RW	aev	Manual white balanc "R" gain High Byte
wb_mrgain_l	D	97	[7:0]	0x5D	RW	aev	Manual white balanc "R" gain Low Byte
wb_mggain_h	D	98	[0]	0x00	RW	aev	Manual white balanc "G" gain High Byte
wb_mggain_l	D	99	[7:0]	0x40	RW	aev	Manual white balanc "G" gain Low Byte
wb_mbgain_h	D	9A	[0]	0x00	RW	aev	Manual white balanc "B" gain High Byte
wb_mbgain_l	D	9B	[7:0]	0x5E	RW	aev	Manual white balanc "B" gain Low Byte
wb_manual	D	9C	[0]	0x00	RW		WB gain mode selection 1'b0 : auto WB gain 1'b1 : manual WB gain
edge_pgain	D	DE	[7:0]	0x10	RW	aev	Positive max edge clamp gain
edge_mgain	D	DF	[7:0]	0x20	RW	aev	Negative max edge clamp gain
dark_ec_pth	D	E0	[7:0]	0x10	RW	aev	Current edge clamp plus TH filter fitting value

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
dark_ec_mth	D	E1	[7:0]	0x10	RW	aev	Current edge clamp minus TH filter fitting value
dark_ec_pmax	D	E2	[7:0]	0x80	RW	aev	Current edge clamp plus max filter fitting value
dark_ec_mmax	D	E3	[7:0]	0x80	RW	aev	Current edge clamp minus max filter fitting value
isp_dgain	D	E6	[7:0]	0x40	RW	aev	Digital gain

Table 51 Register Table - Group E

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
gm1_y0	E	04	[7:0]	0x00	RW		gamma1 coefficient 0
gm1_y1	E	05	[7:0]	0x3B	RW		gamma1 coefficient 1
gm1_y2	E	06	[7:0]	0x49	RW		gamma1 coefficient 2
gm1_y3	E	07	[7:0]	0x52	RW		gamma1 coefficient 3
gm1_y4	E	08	[7:0]	0x5A	RW		gamma1 coefficient 4
gm1_y5	E	09	[7:0]	0x60	RW		gamma1 coefficient 5
gm1_y6	E	0A	[7:0]	0x65	RW		gamma1 coefficient 6
gm1_y7	E	0B	[7:0]	0x6A	RW		gamma1 coefficient 7
gm1_y8	E	0C	[7:0]	0x6F	RW		gamma1 coefficient 8
gm1_y9	E	0D	[7:0]	0x76	RW		gamma1 coefficient 9
gm1_y10	E	0E	[7:0]	0x7D	RW		gamma1 coefficient 10
gm1_y11	E	0F	[7:0]	0x83	RW		gamma1 coefficient 11
gm1_y12	E	10	[7:0]	0x88	RW		gamma1 coefficient 12
gm1_y13	E	11	[7:0]	0x92	RW		gamma1 coefficient 13
gm1_y14	E	12	[7:0]	0x9A	RW		gamma1 coefficient 14
gm1_y15	E	13	[7:0]	0xA1	RW		gamma1 coefficient 15
gm1_y16	E	14	[7:0]	0xA8	RW		gamma1 coefficient 16
gm1_y17	E	15	[7:0]	0xBE	RW		gamma1 coefficient 17
gm1_y18	E	16	[7:0]	0xCF	RW		gamma1 coefficient 18
gm1_y19	E	17	[7:0]	0xDD	RW		gamma1 coefficient 19
gm1_y20	E	18	[7:0]	0xEA	RW		gamma1 coefficient 20
gm1_y21	E	19	[7:0]	0xF5	RW		gamma1 coefficient 21
gm1_y22	E	1A	[7:0]	0xFF	RW		gamma1 coefficient 22
dark_y_gm	E	2E	[7:0]	0x00	RW	aev	Current Y gamma fitting value
ccr_m11	E	31	[7:0]	0x31	RW	aev	Color correction matrix value 1
ccr_m12	E	32	[7:0]	0xA6	RW	aev	Color correction matrix value 2
ccr_m13	E	33	[7:0]	0x82	RW	aev	Color correction matrix value 3
ccr_m21	E	34	[7:0]	0x90	RW	aev	Color correction matrix value 4
ccr_m22	E	35	[7:0]	0x44	RW	aev	Color correction matrix value 5
ccr_m23	E	36	[7:0]	0x94	RW	aev	Color correction matrix value 6
ccr_m31	E	37	[7:0]	0x84	RW	aev	Color correction matrix value 7
ccr_m32	E	38	[7:0]	0x9E	RW	aev	Color correction matrix value 8
ccr_m33	E	39	[7:0]	0x43	RW	aev	Color correction matrix value 9
dark_ccr	E	3A	[7:0]	0x00	RW	aev	Current color correction fitting value
dark_rgb_gm	E	66	[7:0]	0x00	RW	aev	Current RGB gamma fitting value
dark_dc	E	6B	[7:0]	0x00	RW	aev	Current de-color dark filter fitting value
ybrightness	E	72	[7:0]	0x00	RW	aev	Current Y brightness fitting value

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
y_cont_ay	E	73	[7:0]	0xC0	RW	aev	contrast 1st point Y axis
y_cont_by	E	74	[7:0]	0xC0	RW	aev	contrast 2nd point Y axis
cs11	E	76	[7:0]	0x20	RW	aev	Color saturation matrix value 1
cs12	E	77	[7:0]	0x80	RW	aev	Color saturation matrix value 2
cs21	E	78	[7:0]	0x80	RW	aev	Color saturation matrix value 3
cs22	E	79	[7:0]	0x20	RW	aev	Color saturation matrix value 4
user_cs	E	7A	[7:0]	0x28	RW		User CS gain
ae_fwx1_h	E	AD	[2:0]	0x00	RW		AE full window X start position High Byte
ae_fwx1_l	E	AE	[7:0]	0x04	RW		AE full window X start position Low Byte
ae_fwx2_h	E	AF	[2:0]	0x05	RW		AE full window X stop position High Byte
ae_fwx2_l	E	B0	[7:0]	0x04	RW		AE full window X stop position Low Byte
ae_fwy1_h	E	B1	[2:0]	0x00	RW		AE full window Y start position High Byte
ae_fwy1_l	E	B2	[7:0]	0x04	RW		AE full window Y start position Low Byte
ae_fwy2_h	E	B3	[2:0]	0x02	RW		AE full window Y stop position High Byte
ae_fwy2_l	E	B4	[7:0]	0xD4	RW		AE full window Y stop position Low Byte
ae_cwx1_h	E	B5	[2:0]	0x01	RW		AE center window X start position High Byte
ae_cwx1_l	E	B6	[7:0]	0xAD	RW		AE center window X start position Low Byte
ae_cwx2_h	E	B7	[2:0]	0x03	RW		AE center window X stop position High Byte
ae_cwx2_l	E	B8	[7:0]	0x5A	RW		AE center window X stop position Low Byte
ae_cwy1_h	E	B9	[2:0]	0x00	RW		AE center window Y start position High Byte
ae_cwy1_l	E	BA	[7:0]	0xF2	RW		AE center window Y start position Low Byte
ae_cwy2_h	E	BB	[2:0]	0x01	RW		AE center window Y stop position High Byte
ae_cwy2_l	E	BC	[7:0]	0xE5	RW		AE center window Y stop position Low Byte
ae_xaxis_h	E	BD	[2:0]	0x02	RW		AE window X axis High Byte
ae_xaxis_l	E	BE	[7:0]	0x84	RW		AE window X axis Low Byte
ae_yaxis_h	E	BF	[2:0]	0x01	RW		AE window Y axis High Byte
ae_yaxis_l	E	C0	[7:0]	0x6C	RW		AE window Y axis Low Byte
awb_wx1_h	E	C1	[2:0]	0x00	RW		AWB window X start position High Byte
awb_wx1_l	E	C2	[7:0]	0x04	RW		AWB window X start position Low Byte
awb_wx2_h	E	C3	[2:0]	0x05	RW		AWB window X stop position High Byte
awb_wx2_l	E	C4	[7:0]	0x04	RW		AWB window X stop position Low Byte
awb_wy1_h	E	C5	[2:0]	0x00	RW		AWB window Y start position High Byte
awb_wy1_l	E	C6	[7:0]	0x04	RW		AWB window Y start position Low Byte
awb_wy2_h	E	C7	[2:0]	0x02	RW		AWB window Y stop position High Byte
awb_wy2_l	E	C8	[7:0]	0xD4	RW		AWB window Y stop position Low Byte

Table 52 Register Table - Group F

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
sif_control0	F	64	[7:0]	0x04	RW		Serial Interface control 0

Table 53 Register Table - Group H

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
nr2d_ctrl_0	H	04	[7:0]	0x94	RW	aev	NR control register 0

Table 54 Register Table - Group I

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
Status	I	08	[7:0]		RO		Monitoring of PVI encoder internal status
Hsize	I	09	[7:0]		RO		Monitoring of PVI encoder internal status
Vsize	I	0A	[7:0]		RO		Monitoring of PVI encoder internal status
HVsize	I	0B	[7:0]		RO		Monitoring of PVI encoder internal status
Rev_ID	I	0F					Read Only Register 8'h10 : PV4109 PVI Tx IP update
MS_HDATX_control0	I	10	[7:0]	0x43	RW		PVI encoder control 0
MS_HDATX_control1	I	11	[7:0]	0x06	RW		PVI encoder control 1
MS_HDATX_control2	I	12	[7:0]	0x02	RW		PVI encoder control 2
MS_HDATX_control3	I	13	[7:0]	0xE0	RW		PVI encoder control 3
CONT	I	14	[7:0]	0x80	RW		Contrast control value
BRT	I	15	[7:0]	0x80	RW		Brightness control value
SAT	I	16	[7:0]	0x80	RW		Color saturation control value
HUE	I	17	[7:0]	0x80	RW		Hue control value
MS_HDATX_control4	I	18	[7:0]	0x00	RW		PVI encoder control 4
HS_STRT_DLY_L	I	1A	[7:0]	0x00	RW		Hsync start delay Low Byte
HS_STRT_DLY_H	I	1B	[5:0]	0x00	RW		Hsync start delay High Byte
FSC_SEL	I	58	[7:0]	0x72	RW		Color subcarrier selection [6:4] : FSC_MD_SEL [2:0] : FSC_CLK_SEL
FLT_MD	I	5C	[7:0]	0x82	RW		Y/C filter characteristic selection
MS_HDATX_control9	I	66	[7:0]	0x01	RW		PVI encoder control 9

Table 55 Register Table - Group O

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
exposure_mode	O	08	[7:0]	0x00	RW	autov	Exposure mode selection
ext_inttime_h	O	20	[7:0]	0x00	RW	autov	Manual integration time High Byte @ external AE mode
ext_inttime_m	O	21	[7:0]	0x80	RW	autov	Manual integration time Middle Byte @ external AE mode
ext_inttime_l	O	22	[7:0]	0x00	RW	autov	Manual integration time Low Byte @ external AE mode
ext_glbg_h	O	23	[7:0]	0x01	RW	autov	Manual analog gain High Byte @ external AE mode
ext_glbg_l	O	24	[7:0]	0x00	RW	autov	Manual analog gain Low Byte @ external AE mode
exposure_t	O	25	[7:0]	0x00	RW	autov	Exposure value 1
exposure_h	O	26	[7:0]	0x01	RW	autov	Exposure value 2
exposure_m	O	27	[7:0]	0x40	RW	autov	Exposure value 3
exposure_l	O	28	[7:0]	0x00	RW	autov	Exposure value 4
filter_ctrl_1	O	69	[7:0]	0xFE	RW	autov	Filter control 1

Table 56 Register Table - Control register map

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
pad_control1	A	5F	[5:4]	2'b00	RW		**stdby_lv** Output data pad stdby level selector 2'b00 : low 2'b01 : high 2'b1x : hi-z
	A	5F	[3]	1'b0	RW		**clkoff** Clock pad kill enable 1'b0 : disable (not kill) 1'b1 : enable (kill)
	A	5F	[2]	1'b1	RW		**osc_pad_en** OSC pad enable 1'b0 : disable 1'b1 : enable
	A	5F	[1:0]	2'b00	RW		**osc_pad_drv** OSC pad drivability control
pad_control2	A	60	[7]	1'b0	RW		**pclk_pol** PCLK pad polarity control 1'b0 : disable 1'b1 : enable
	A	60	[6]	1'b0	RW		**pclk_pad_en** PCLK pad enable 1'b0 : disable 1'b1 : enable
	A	60	[5:4]	2'b00	RW		**pclk_pad_drv** PCLK pad drivability control
	A	60	[3:0]	4'b0000	RW		**digi_pclk_delay** PCLK timing delay delay = dly_digi_PCLK*0.4 ns
pad_control3	A	61	[7]	1'b0	RW		**vsync_pad_en** Digital video pad enable 1'b0 : disable 1'b1 : enable
	A	61	[6:5]	2'b00	RW		**hsync_pad_drv** Hsync Pad drivability control
	A	61	[4]	1'b0	RW		**hsync_pad_en** Hsync pad enable 1'b0 : disable 1'b1 : enable
	A	61	[3:2]	2'b00	RW		**pad_drv** Data pad drivability control
	A	61	[1]	1'b0	RW		**dpad_swap** Data pad swap option 1'b0 : [MSB:LSB] 1'b1 : [LSB:MSB]
pad_control4	A	62	[7]	1'b0	RW		**d7_pad_en** D7 pad control 1'b0 : disable

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							1'b1 : enable
	A	62	[6]	1'b0	RW		**d6_pad_en** D6 pad control 1'b0 : disable 1'b1 : enable
	A	62	[5]	1'b0	RW		**d5_pad_en** D5 pad control 1'b0 : disable 1'b1 : enable
	A	62	[4]	1'b0	RW		**d4_pad_en** D4 pad control 1'b0 : disable 1'b1 : enable
	A	62	[3]	1'b0	RW		**d3_pad_en** D3 pad control 1'b0 : disable 1'b1 : enable
	A	62	[2]	1'b0	RW		**d2_pad_en** D2 pad control 1'b0 : disable 1'b1 : enable
	A	62	[1]	1'b0	RW		**d1_pad_en** D1 pad control 1'b0 : disable 1'b1 : enable
	A	62	[0]	1'b0	RW		**d0_pad_en** D0 pad control 1'b0 : disable 1'b1 : enable
pad_control5	A	63	[6]	1'b0	RW		**led_pad_sel** D0 pad selection 1'b0 : D0 pad 1'b1 : LED pad
	A	63	[5:4]	1'b0	RW		**led_pad_drv** LED pad drivability contro
	A	63	[1:0]	1'b0	RW		**mirs_pad_drv** MIRS pad drivability contro
sync_control_0	A	1C	[6:5]	2'b00	RW		**sync_drop** Vsync, hsync drop control 2'b00 : No drop 2'b01 : hsync drop 2'b10 : vsync drop 2'b11 : hsync and vsync drop
sync_control_1	A	1D	[6]	1'b0	RW		**vsync_polarity** Vsync polarity change 1'b0 : disable 1'b1 : enable
	A	1D	[5]	1'b0	RW		**hsync_all_line** Hsync output all lines enable(black and

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							active) 1'b0 : No hsync during vertical blank 1'b1 : hsync during vertical blank
	A	1D	[4]	1'b0	RW		**hsync_polarity** Hsync polarity change 1'b0 : disable 1'b1 : enable
	A	1D	[3:2]	2'b00	RW		**data_seq** Data sequence selection
	A	1D	[1]	1'b1	RW		**data_clamp** Data clamping enable 1'b0 : disable 1'b1 : enable
	A	1D	[0]	1'b0	RW		**bt1120** Data header control 1'b0 : CCIR656 1'b1 : BT1120
i2c_control_1	A	35	[7:4]	4'b0101	RW		**updatecontrol** [7:6] : Control I2C Register Update by auto_vsync update_autov <= reg_updatecontrol[3] or (autov_update and reg_updatecontrol[2]) [5:4] : Control I2C Register Update by ae_vsync update_aev <= reg_updatecontrol[1] or (aev_update and reg_updatecontrol[0])
clkdiv1	A	59	[7:6]	2'b01	RW		**adcclk_div** ADC clock divider isp_clk =vco1/(2^adcclk_div)
	A	59	[5:4]	2'b10	RW		**ispclk1_div** ISP clock divider isp_clk =vco1/(2^ispclk_div)
clkdiv4	A	5C	[7]	1'b0	RW		**dclk_div** D clk divider 1'b0 : 1/1 1'b1 : 1/2
	A	5C	[3]	1'b1	RW		**tx_rclk_en** tx_rclk clock gate enable 1'b0 : disable 1'b1 : enable
	A	5C	[2]	1'b1	RW		**pll_clk_en** pll_clk clock gate enable 1'b0 : disable 1'b1 : enable
pll_control2	A	55	[5]	1'b1	RW		**plltg_pd** PLL power down mode 1'b0 : pll power on 1'b1 : pll power down
	A	55	[4]	1'b1	RW		**pll_bypass**

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							PLL bypass 1'b0 : use pll mode 1'b1 : pll bypass mode
led_control1	A	80	[7]	1'b0	RW		**ledctrl_en** LED control enable 1'b0 : disable 1'b1 : enable
	A	80	[6]	1'b0	RW		**ledctl_manual** LED manual enable 1'b0 : disable 1'b1 : enable
	A	80	[5]	1'b0	RW		**ledctl_pol** LED control polarity enable 1'b0 : disable 1'b1 : enable
	A	80	[4]	1'b0	RW		**bwled_en** BWLED enable 1'b0 : disable 1'b1 : enable
	A	80	[3]	1'b0	RW		**mirs_en** MIRS control enable 1'b0 : disable 1'b1 : enable
	A	80	[2:1]	2'b00	RW		**mirs_manual** MIRS manual control 2'b00 : MIRS1 Low / MIRS0 Low 2'b01 : MIRS1 Low / MIRS0 High 2'b10 : MIRS1 High / MIRS0 Low 2'b11 : MIRS1 High / MIRS0 High
	A	80	[0]	1'b0	RW		**mirs_pol** MIRS control polarity enable 1'b0 : disable 1'b1 : enable
led_control2	A	81	[6]	1'b0	RW		**bwled_manual** BWLED manual enable 1'b0 : disable 1'b1 : enable
	A	81	[5]	1'b0	RW		**mirs_swap** MIRS control swap enable 1'b0 : disable 1'b1 : enable
	A	81	[4]	1'b0	RW		**mirs_manual_mode** MIRS manual mode enable 1'b0 : enable 1'b1 : disable
	A	81	[3]	1'b0	RW		**led_blink_en** LED blink enable 1'b0 : disable 1'b1 : enable

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
isp_func_0	D	66	[7]	1'b1	RW	aev	**lens_en** Lens shading compensation enable 1'b0 : disable 1'b1 : enable
	D	66	[1]	1'b1	RW	aev	**ccr_en** Color correction enable 1'b0 : disable 1'b1 : enable
isp_func_1	D	67	[7]	1'b1	RW	aev	**cgm_en** RGB gamma enable 1'b0 : disable 1'b1 : enable
	D	67	[6]	1'b1	RW	aev	**ygm_en** Y gamma enable 1'b0 : disable 1'b1 : enable
	D	67	[3]	1'b1	RW	aev	**edge_en** Edge enhancement enable 1'b0 : disable 1'b1 : enable
isp_func_6	D	6C	[2]	1'b1	RW	aev	**dc_en** De-color enable 1'b0 : disable 1'b1 : enable
nr2d_ctrl_0	H	04	[7]	1'b1	RW	aev	**nr_en** NR enable 1'b0 : disable 1'b1 : enable
flicker_control1	D	55	[6]	1'b0	RW		**fd_en** Flicker detection enable 1'b0 : disable 1'b1 : enable
	D	55	[3]	1'b1	RW		**fd_manual_A** manual A mode enable 1'b0 : disable 1'b1 : enable
	D	55	[2]	1'b0	RW		**fd_manual_B** manual B mode enable 1'b0 : disable 1'b1 : enable
format	A	2E	[7:0]	8'h00	RW	aev	**format_control** 1'b0 : yuv422 1'b1 : raw_bayer
filter_ctrl_1	O	69	[3]	1'b1	RW	autov	**Y/C gm fitting** Y/RGB gamma fitting enable 1'b0 : disable 1'b1 : enable
spi_osd_control0	A	BC	[3]	1'b0	RW		**pg_enable** PG enable

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							1'b0 : disable 1'b1 : enable
spi_osd_control1	A	BD	[7]	1'b0	RW		**manual_chrm_zero** Always encoder chroma signal 0'd 1'b0 : disable 1'b1 : enable
	A	BD	[6]	1'b0	RW		**bw_chrm_zero** If bwled is, encoder chroma signal 0'd 1'b0 : disable 1'b1 : enable
pg_control0	A	BF	[5]	1'b0	RW	aev	**pg_blink** PG blink enable 1'b0 : disable 1'b1 : enable
	A	BF	[4]	1'b0	RW	aev	**pg_hlight** PG hlight enable 1'b0 : disable 1'b1 : enable
	A	BF	[3]	1'b1	RW	aev	**pg_rm_ych** Remove yochul line of PG 1'b0 : disable 1'b1 : enable
	A	BF	[2:1]	2'b00	RW	aev	**pg_rm** pg_rm[1] : remove left side of PG 1'b0 : disable 1'b1 : enable pg_rm[0] : remove right side of PG 1'b0 : disable 1'b1 : enable
sif_control0	F	64	[6:5]	2'b00	RW		**sif_chip_mode** Chip mode selection 2'b00 : Chipmode 00 else : Chipmode 01
MS_HDATX_control0	I	10	[4]	1'b0	RW		**ENC_LIM_EN** Enable Active Data Range Limitation 1'b0 : No Limit (1 ~ 254 Range) 1'b1 : 16 ~ 240 Range
MS_HDATX_control1	I	11	[7]	1'b0	RW		**TST_IN_EN** Selection Test Pattern Enable 1'b0 : Normal Mode 1'b1 : Test Pattern Enable
	I	11	[6]	1'b0	RW		**ENC_CBCR_INV** Selection CB/CR Swapping Enable 1'b0 : Normal 1'b1 : Cb/Cr Swapping
	I	11	[5]	1'b0	RW		**ENC_FLD_POL** Selection Field Polarity Inversion 1'b0 : Normal 1'b1 : Field Polarity Inversion

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
	I	11	[4]	1'b0	RW		**ENC_YC_INV** Selection Y/C Swapping Enable 1'b0 : Normal 1'b1 : Y/C Swapping
	I	11	[3:0]	4'b0110	RW		**TST_MODE** Selection Mode for Test Pattern 4'd0 : 1280x720p@30Hz (37.125M) : 1650 x 750 4'd1 : 1280x720p@25Hz (37.125M) : 1980 x 750
MS_HDATX_control2	I	12	[1:0]	2'b10	RW		**CSC_MD** Selection Color Space Conversion Mode [1] : Color Space Conversion Enable 1'b0 : Bypass for CSC 1'b1 : Enable for CSC [0] : Color Space Conversion Mode 1'b0 : BT 601 to BT709 Conversion 1'b1 : BT709 to BT601 Conversion
MS_HDATX_control3	I	13	[7:4]	4'b1110	RW		**TST_PT_SEL** Selection of Test Pattern 4'd0 : Black 4'd1 : Blue 4'd2 : Red 4'd3 : Magenta 4'd4 : Green 4'd5 : Cyan 4'd6 : Yellow 4'd7 : White 4'd8 : Color Bar 4'd9 : Gray Bar 4'd10 : Hatch Pattern 4'd11 : Center Box Pattern 4'd12 : H Sweep Pattern 4'd13 : H/V Frequency Sweep Pattern 4'd14 : Complex Mixed Pattern0 4'd15 : Complex Mixed Pattern1
	I	13	[3]	1'b0	RW		**CONT_EN** Selection Contrast Control Enable 1'b0 : Bypass 1'b1 : Enable
	I	13	[2]	1'b0	RW		**BRT_EN** Selection Brightness Control Enable 1'b0 : Bypass 1'b1 : Enable
	I	13	[1]	1'b0	RW		**SAT_EN** Selection Saturation Control Enable 1'b0 : Bypass 1'b1 : Enable
	I	13	[0]	1'b0	RW		**HUE_EN** Selection Hue Control Enable 1'b0 : Bypass

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							1'b1 : Enable
MS_HDATX_control4	I	18	[7]	1'b0	RW		**INT_MD** Selection Interlace Mode 1'b0 : Progressive for HD 1'b1 : Interlace for SD
	I	18	[6]	1'b0	RW		**PHALT** Selection Phase Alternation for Color Burst 1'b0 : No Phase Alternation 1'b1 : Enable Phase Alternation
	I	18	[5]	1'b0	RW		**PDRST** Phase Alternation Clear Enable 1'b0 : No Reset 1'b1 : Enable Phase Reset @ Every 4 Frame
MS_HDATX_control9	I	66	[6]	1'b0	RW		**CHROMA_OFF** Selection Chroma Off Mode 1'b0 : Normal 1'b1 : Chroma Off

Revision History

Version	Date [D/M/Y]	Notes	Writer
0.0	21/12/2020	(Preliminary)	Jaedong Park
0.1	04/01/2021	• Update Initialization. - P.27 – Deleted FRAME MODE.	Jaedong Park
0.2	29/06/2021	• Update General Description. - P.8 – Operating temp. • Update Register. - P.64 – DeviceID.	Jaedong Park
0.3	08/07/2021	• Update General Description. - P.8 – Dark signal. – Sensitivity. – Power consumption – Dynamic range – SNR – Package type • Update DC Characteristics. - P.61	Jaedong Park
0.4	26/08/2021	• Update Features. - P.7 – Auto LED control with CdS	Jaedong Park
0.5	15/10/2021	• Update DC Characteristics. - P.61 – IDDD, Max	Jaedong Park