1.3Mp CMOS Digital Image Sensor

MT9M413

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Features

- Output data rate: 660 Mb/s (master clock 66 MHz, ~500 fps)
- Output: 10-bit digital through 10 parallel ports
- Conversion gain: 13 µV/e^-
- Shutter efficiency: >99.9%
- Shutter exposure time: 2µs to >33msec
- Programmable controls: open architecture,
  - On-chip: ADC controls, output multiplexing, and ADC calibration
  - Off-chip: window size and location, frame rate and data rate, shutter exposure time (integration time), and ADC reference

Applications

- Machine vision
- Automotive testing
- Motion analysis
- Film special effects
- Animation
- 3D imaging

Ordering Information

Table 1: Available Part Numbers

Part Number	Description
MT9M413C36STC	280-pin ceramic PGA (color)
MT9M413C36STM	280-pin ceramic PGA (monochrome)

Table 2: Key Performance Parameters

Parameter	Value
Optical format	1-inch
Active imager size	15.36mm(H) x 12.29mm(V) 19.67mm diagonal
Active pixels	1280H x 1024V
Pixel size	12.00 x 12.00µm
Color filter array	Color RGB Bayer pattern, or monochrome
Shutter type	TrueSNAP freeze-frame electronic shutter
Maximum data rate	660 Mb/s
Frame rate	0–500+ fps at 1280 x 1024, >10,000 fps with partial scan
ADC resolution	On-chip, 10-bit column-parallel
Responsivity	Mono: 1600 LSB per lux-sec at 550nm
Dynamic range	59dB
Supply voltage	+3.3V
Power consumption	<500mW at 500 fps <150mW at 60 fps
Operating temperature	–5°C to +60°C
Package	280-pin ceramic PGA

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General Description

The MT9M413 is a 1280H x 1024V (1.3 megapixel) CMOS digital image sensor capable of 500 frames-per-second (fps) operation. Its TrueSNAP™ electronic shutter allows simultaneous exposure of the entire pixel array. Available in color or monochrome, the sensor has on-chip 10-bit analog-to-digital converters (ADCs), which are self-calibrating, and a fully digital interface. The input clock rate of the chip is 66 MHz at approximately 500 fps, providing compatibility with many off-the-shelf interface components, as shown in Figure 1.

The sensor has ten (10) 10-bit-wide digital output ports. The open architecture design provides access to internal operations and the ADC timing and pixel read control are integrated on-chip. At 60 fps, the sensor dissipates less than 150mW, and at 500 fps less than 500mW, operating on a 3.3V supply. The pixel size is 12 microns square and the digital responsivity is 1600 LSB per lux-second.

A complete camera system can be built by using the chip in conjunction with the following external devices:

- An FPGA/CPLD/ASIC controller, to manage the timing signals needed for sensor operation.
- A 20mm diagonal lens.
- Biasing circuits and bypass capacitors.

Figure 1: A Camera System Using the MT9M413 CMOS Image Sensor

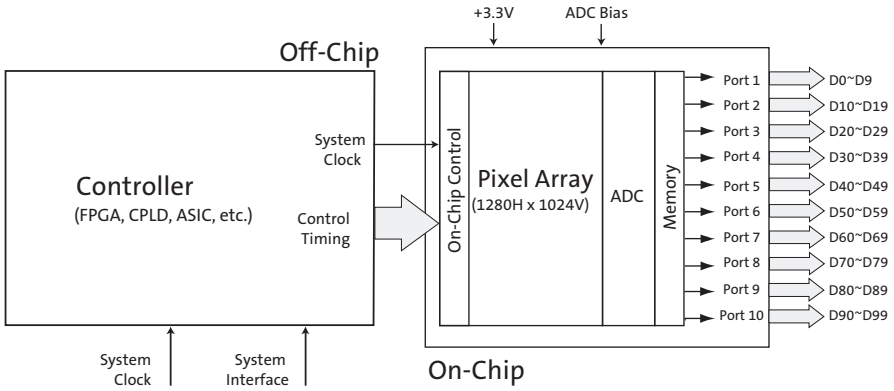
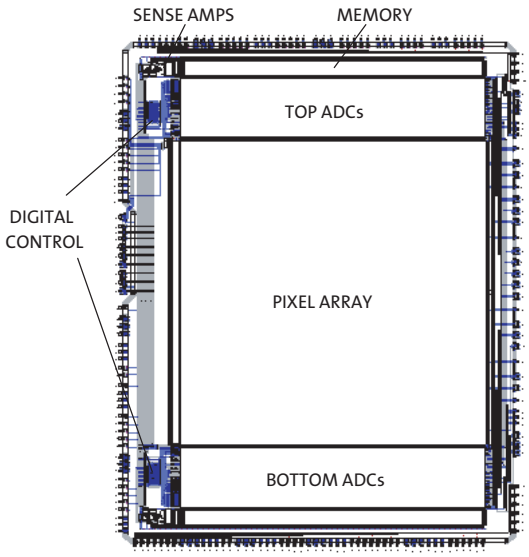


Figure 2: Sensor Architecture



Notes: 1. Not to scale.

Figure 3: Signal Path Diagram

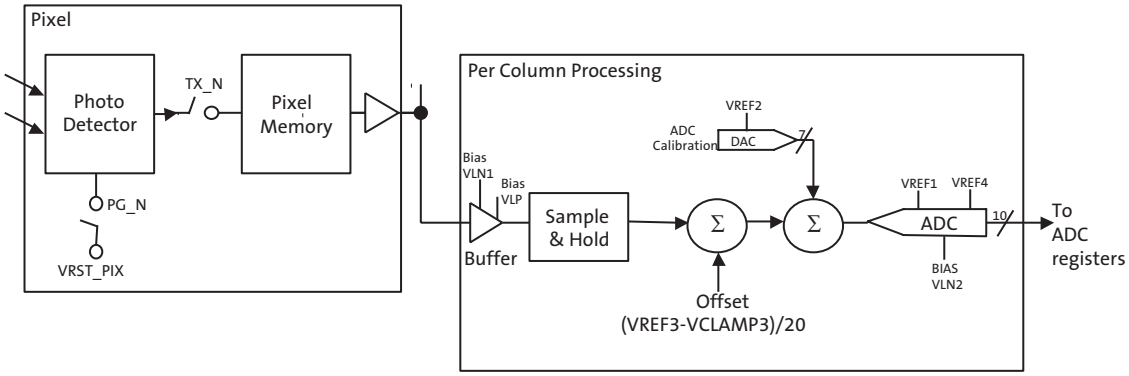
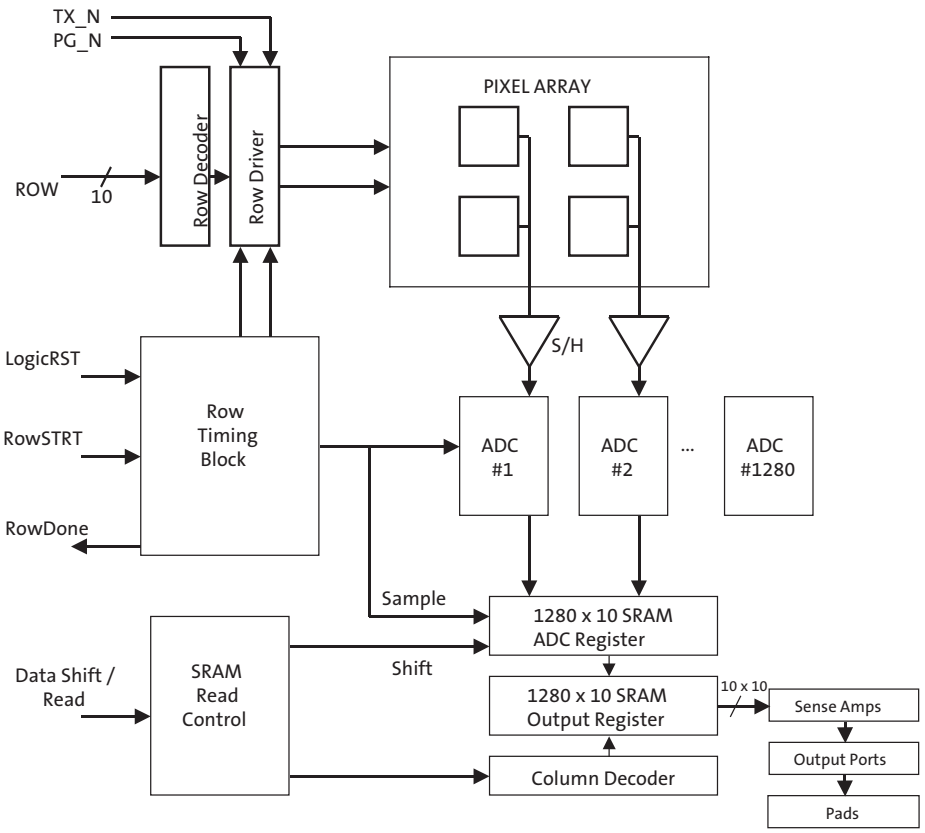


Figure 4: Functional Block Diagram



External Control Sequence

The MT9M413 includes on-chip timing and control circuitry to control most of the pixel, ADC, and output multiplexing operations. However, the sensor still requires a controller (FPGA, CPLD, ASIC) to guide it through the full sequence of its operation.

With the TrueSNAP freeze-frame electronic shutter, signal charges are integrated in all pixels in parallel. The charges are then sampled into pixel analog memories (one memory per pixel) and subsequently, row by row, are digitized and read out of the sensor.

The integration of the photosignal is controlled by two control signals:

- PG_N
- TX_N

To clear pixels and start new integration, PG_N is LOW. To transfer the data into pixel memory, TX_N is LOW. The time difference between the two procedures is the exposure time. It should be noted that neither the PG_N or TX_N pulses clear the pixel analog memory. Pixel memory can be cleared during the previous readout (that is, the readout process resets the pixel analog memory), or by applying PG_N and TX_N together (clearing both pixel and pixel memory at the same time).

With the TrueSNAP freeze-frame electronic shutter, the sensor can operate in either simultaneous or sequential mode, generating continuous video output. In simultaneous mode, as a series of frames is being captured, the PG_N and TX_N signals are exercised while the previous frame is being read out of the sensor. In simultaneous mode, the end of integration occurs in the last row of the frame (row #1023) or in the last row of the window of interest. The position of the start integration is then calculated from the desired integration time. In sequential mode, the PG_N and TX_N signals are exercised to control the integration time, and then digitization and readout of the frame take place. Alternatively, the sensor can run in single frame or snapshot mode in which one image is captured.

The sensor has a column-parallel ADC architecture that allows the array of 1,280 ADCs on the chip to digitize the analog data from an entire pixel row simultaneously. Table 3 shows the input signals utilized to control the conversion and readout process.

Table 3: Conversion and Readout Process

Signal Name	Description	Input Bus Width
ROW_ADDR	Row address	10-bit
ROW_STRT_N	Row start	1-bit
LD_SHFT_N	Load shift register	1-bit
DATA_READ_EN_N	Data read enable	1-bit

The 10-bit ROW_ADDR (row address) input bus selects the pixel row to be read for each readout cycle. The ROW_STRT_N signal starts the process of reading the analog data from the pixel row, the ADC, and the storage of the digital values in the ADC registers. When these actions are completed, the sensor sends a response back to the system controller using the ROW_DONE_N. Row address must be valid for the first half of the row processing time (the period between ROW_START_N and ROW_DONE_N).

The MT9M413 contains a pipeline style memory array, which is used to store the data after digitization. This memory also allows the data from the previous row conversion cycle to be read while a new conversion is taking place.

The digital readout is controlled by lowering the LD_SHFT_N signal, followed by the DATA_READ_EN_N signal. LD_SHFT_N transfers the digitized data from the ADC register to the output register. DATA_READ_EN_N is used to enable the data output from the output register. A new pixel row readout and conversion cycle can be started two clock cycles after DATA_READ_EN_N is pulled LOW. The output register allows the reading of the digital data from the previous row to be performed at the same time as a new conversion (pipeline mode).

The total row time will be only that between when:

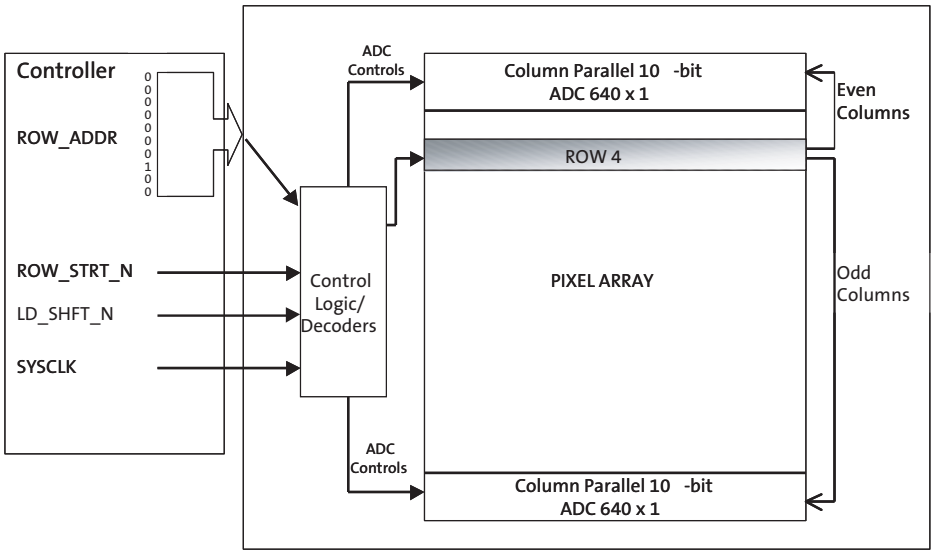
1. The ROW_STRT_N signal is applied and ROW_DONE_N is returned.

   and

2. LD_SHFT_N and DATA_READ_EN_N are applied plus two clock cycles.

In the pipelined operation, there will always be one row of latency at the start of sensor operation. The alternative to pipelined operation is burst data operation in which a new pixel row conversion is not initiated until after the output register is emptied (and LD_SHFT_N has been taken HIGH). The ratio of line active and blanking times can be adjusted to easily match a variety of display and collection formats. See Figure 7 on page 12.

Figure 5: Example 1—Row 4 of the MT9M413 Being Digitized



Notes:
1. Reads the contents of pixel row specified by ROW_ADDR.
2. Converts pixel row signals to digital values.
3. Stores digital values in ADC register (1280 x 10-bit).

PG_N and TX_N

To start integration, the PG_N signal simultaneously resets the photodetectors for the entire pixel array. To end integration, the TX_N signal simultaneously transfers a charge from the photodetector to memory inside each pixel for the entire pixel array. In sequential mode, the PG_N and the TX_N pulses must have a minimum duration of 64 SYSCLK cycles. In simultaneous mode, the PG_N and TX_N pulses must have a duration of 64 SYSCLK cycles and be applied in the window between the 66th and 129th SYSCLK cycles. Additionally, in simultaneous mode between exposures, a single SYSCLK duration pulse must be applied each row during the 130th clock cycle.

ROW_ADDR

The address for the pixel row to be read is input externally through the 10-bit ROW_ADDR input bus. This address must be valid for at least 66 SYSCLK cycles, and must be valid when ROW_STRT_N is pulled LOW.

ROW_STRT_N

ROW_STRT_N reads the contents of the pixel row specified by ROW_ADDR, converts the pixel row signal to digital value, and stores the digital value in ADC register (1280 x 10-bit).

This process is completed in 128–129 SYSCLK cycles; it must be valid for a minimum of 2 clock cycles and a maximum of 100 clock cycles.

Note: To minimize the sensor power consumption, the row processing circuitry operates at SYSCLK/2. Therefore, depending on the user's implementation, there will be either 128 or 129 SYSCLK cycles between the start of ROW_STRT_N and ROW_DONE_N.

ROW_DONE_N

For 128–129 SYSCLK cycles after ROW_STRT_N has been pulled LOW, the sensor acknowledges the completion of a row read operation/digitization by pulling the ROW_DONE_N pin LOW for two clock cycles.

LD_SHFT_N

LD_SHFT_N transfers the digitized data from the ADC register to the output register (1280 x 10-bit) and gates the power to the sense amplifiers. The first data (columns 1–10) are available for output at the third rising edge of SYSCLK after LD_SHFT_N is pulled LOW. This may be enabled simultaneously with or after the falling edge of ROW_DONE_N, but must remain LOW the entire time the data is being read out.

DATA_READ_EN_N

DATA_READ_EN_N is used to enable the data output from the output register (1280 x 10-bit) to the ten 10-bit output ports. It may be initiated simultaneously with or after LD_SHFT_N is selected and has a minimum width of one clock cycle.

Table 4: Pixel Array

	CLK 1	CLK 2	...	CLK128
Port 1	Col. 1	Col. 11	...	Col. 1271
Port 2	Col. 2	Col. 12	...	Col. 1272
Port 3	Col. 3	Col. 13	...	Col. 1273
Port 4	Col. 4	Col. 14	...	Col. 1274
Port 5	Col. 5	Col. 15	...	Col. 1275
Port 6	Col. 6	Col. 16	...	Col. 1276
Port 7	Col. 7	Col. 17	...	Col. 1277
Port 8	Col. 8	Col. 18	...	Col. 1278
Port 9	Col. 9	Col. 19	...	Col. 1279
Port 10	Col. 10	Col. 20	...	Col. 1280

Output Register

The use of an output register allows the processing of a row to be performed while the digital data from the previous operation is being read out of the sensor. A new pixel readout and conversion cycle can be started two clock cycles after DATA_READ_EN_N is pulled LOW.

Figure 6: Frame Timing

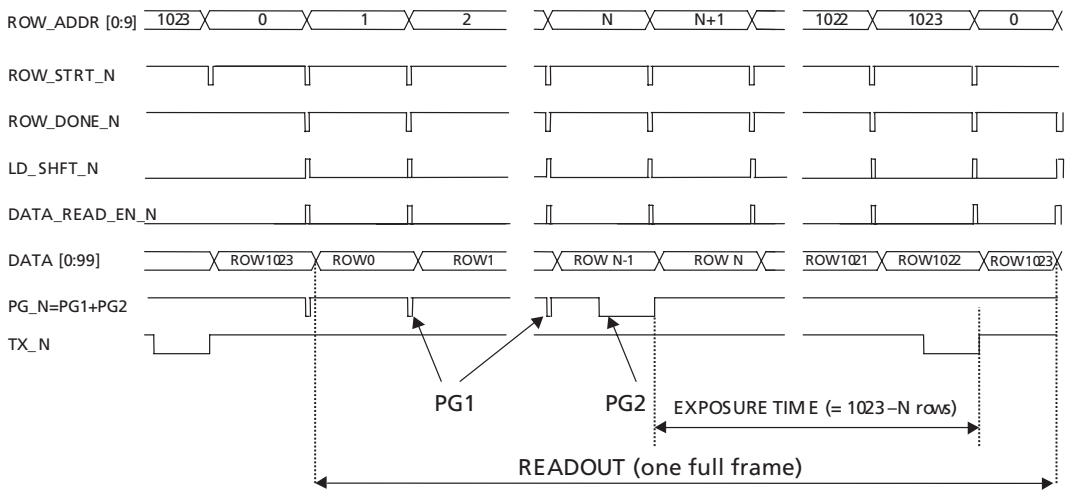
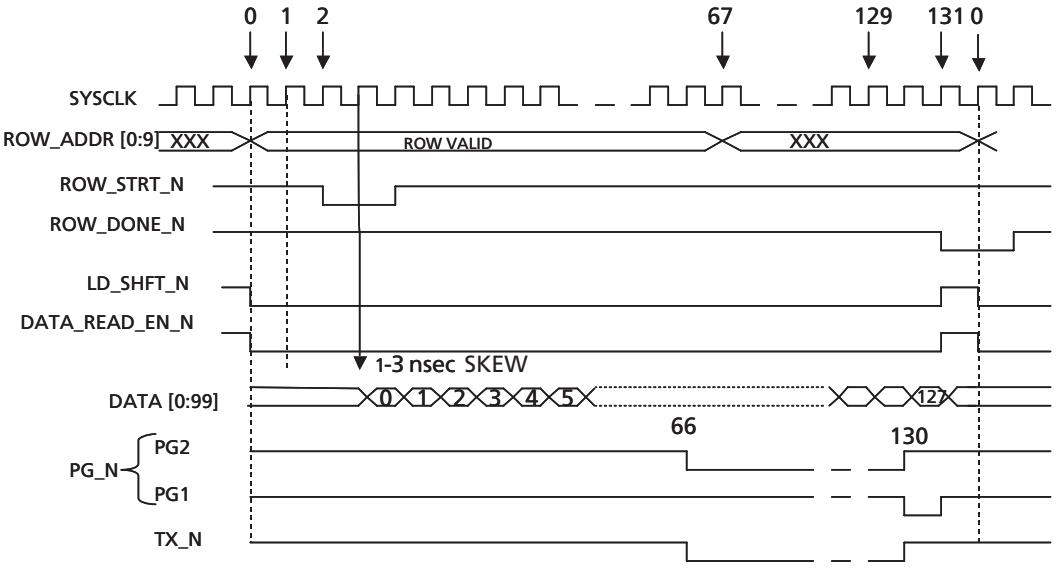


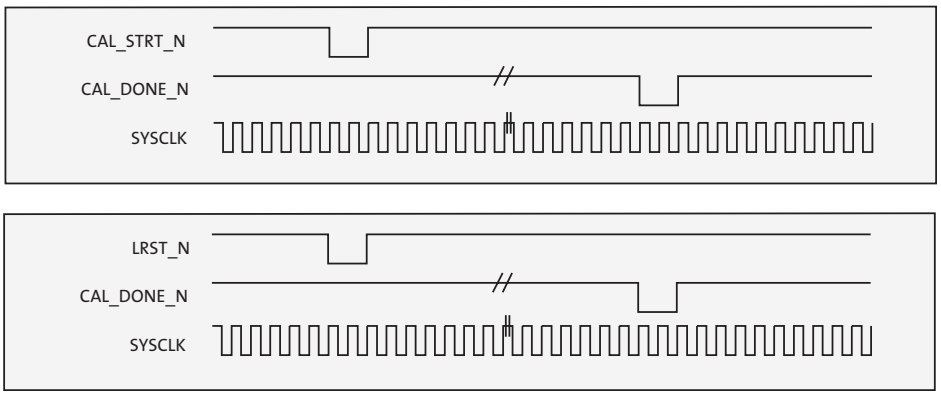
Figure 7: Timing Diagram for One Row



Calibration

The MT9M413 contains special self-calibrating circuitry that enables it to reduce its own column-wise fixed pattern noise (FPN). This calibration process consists of connecting a calibration signal (VREF2) to each of the ADC inputs, and estimating and storing these offsets (7 bits) to subtract from subsequent samples. Figure 8 on page 12 shows the timing sequence to calibrate the sensor. Calibration occurs automatically after logic reset (LRST_N) but it can also be started by the user by pulling CAL_STRT_N LOW. When calibration is finished, the sensor generates the active LOW CAL_DONE_N. Significant ambient temperature drift may justify recalibration (see Figure 6 on page 11 and Figure 8 on page 12).

Figure 8: Typical I/O Signal Timing (Initialization Sequence)



CAL_STRT_N

CAL_STRT_N is a two-clock cycle-wide active-low pulse that initiates the ADC calibration sequence. The pulse must not be actuated for 1 microsecond after either power-up or removal of the sensor from a power-down state. Aptina recommends calibrating using the logic reset.

CAL_DONE_N

CAL_DONE_N is a two-clock cycle-wide active-low output pulse that is asserted when the ADC calibration is complete. The device will automatically initiate a calibration sequence upon a logic reset. Completion of this sequence, in cases where it is initiated by a reset, is still with the CAL_DONE_N signal. This process is complete within 112 SYSCLK cycles of CAL_STRT_N. This process is complete within 112 SYSCLK cycles of LRST_N.

LRST_N

LRST_N is a two-clock cycle-wide active-low pulse that resets the digital logic. It puts all logic into a known state (all flip-flops are reset). This signal also initiates an ADC calibration sequence.

Electronic Shutter

The MT9M413 is intended to be operated primarily with the TrueSNAP freeze-frame electronic shutter, but is also capable of operating in electronic rolling shutter (ERS) mode. With TrueSNAP the shutter can be operated to generate continuous video output (simultaneous mode or sequential mode) or capture single images (single-frame mode).

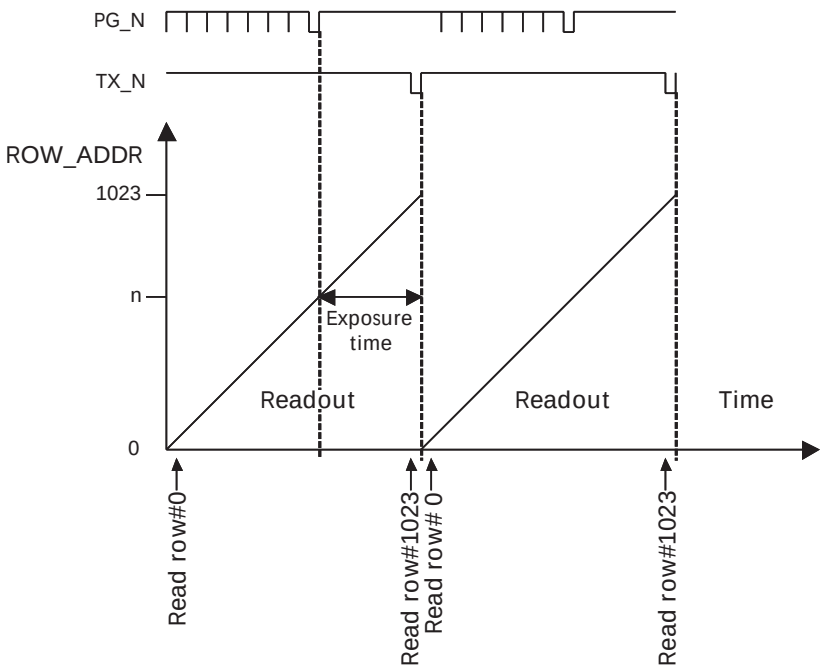
When considering timing for the various shutter modes, keep in mind the functionality of PG_N and TX_N. When PG_N is LOW, the photodetector is shorted to a reset voltage source. When PG_N is HIGH, the switch is open. When TX_N is LOW, the photodetector is shorted to pixel memory; when TN_N is HIGH, the photodetector is disconnected from pixel memory (refer to the switches shown in Figure 3: "Signal Path Diagram," on page 6). The memory is also reset during readout, occurring for the selected row in the middle of the 0–66 clock interval after application of ROW_STRT_N (approximately clocks 20 through 40).

TrueSNAP Simultaneous Mode

In simultaneous mode, as a series of frames are being captured, the PG_N and TX_N signals are exercised while the previous frame is being read out of the sensor. Typically in simultaneous mode, the "end of integration" occurs in the last row of the frame (row #1023) or in the last row of the window of interest. The position of the "start integration" is then calculated from the desired integration time.

Note: The pixel memory is cleared during the readout process, as shown in Figure 9.

Figure 9: Typical Example of TrueSNAP Simultaneous Mode—Exposure During Readout

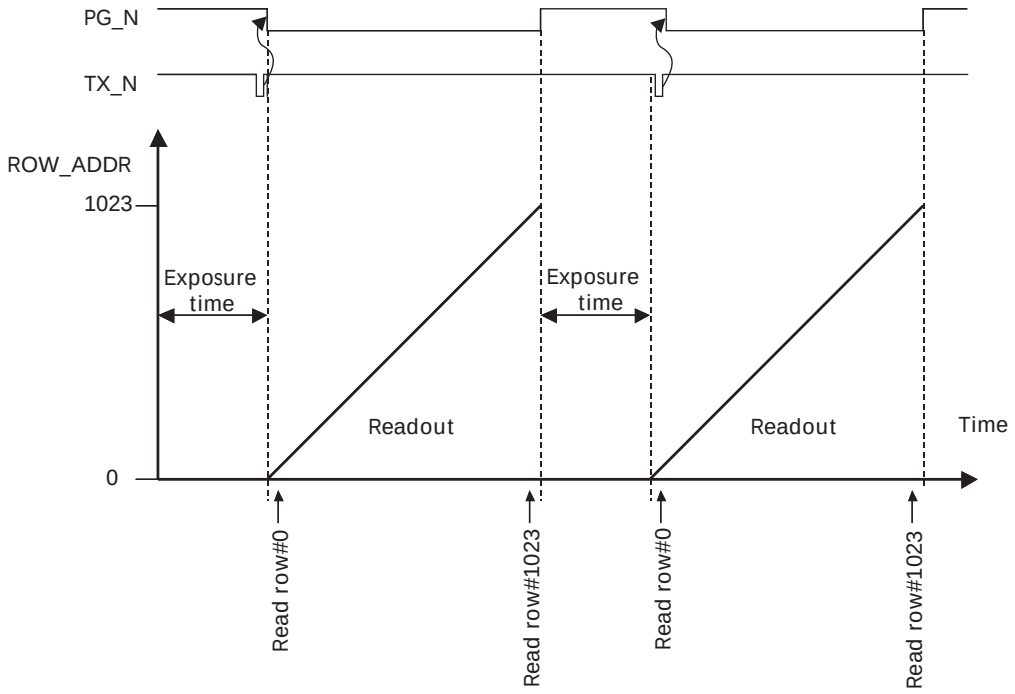


TrueSNAP Sequential Mode

In sequential mode the, PG_N and TX_N signals are exercised to control the integration time, and then digitization and readout of the frame takes place. The photodetector is reset when PG_N is LOW. Raising PG_N starts integration, and lowering TX_N while PG_N is still HIGH ends integration by sampling the signal into memory. There must be at least 1 SYSCLK cycle after returning TX_N to the high state until PG_N is lowered (Figure 10 on page 15).

Note: Pixel memory is cleared during readout process.

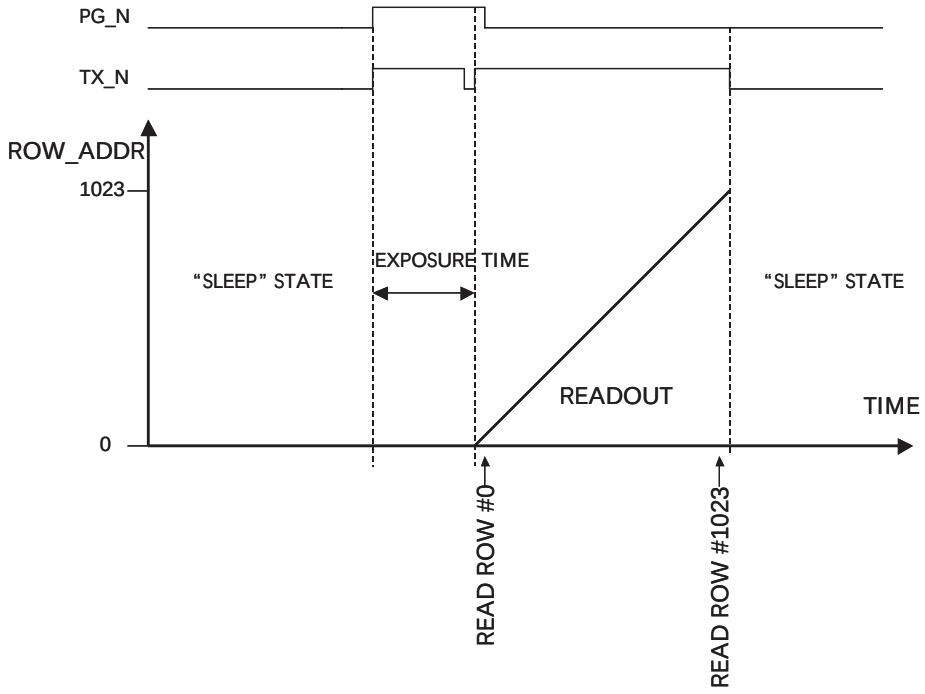
Figure 10: Typical Example of TrueSNAP Sequential Mode—Exposure Following Readout



TrueSNAP Single Frame

The MT9M413 can run in single-frame or snapshot mode in which one image is captured. In single frame mode, integration must be preceded by a void frame read (selecting all addresses and applying ROW_STRT_N) or PG_N and TX_N must be applied together (for a minimum of 10 SYSCLK cycles) to clear pixel and pixel memory. Holding PG_N and TX_N LOW resets the photodioide (PG_N) and the analog memory which is shorted to the photodiode by the TX_N switch. To start integration, both TX_N and PG_N are released; to end integration and sample the signal into memory, TX_N is made LOW again for 10 clocks minimum, up to 64 clocks (see Figure 7 on page 12). After TX_N is returned to the HIGH state there must be a delay of >1 SYSCLK prior to lowering PG_N again to erase charge in the photodetector.

Figure 11: Typical Example of TrueSNAP Single Frame Mode



ERS Mode

ERS mode is enabled by pulling PG_N HIGH and TX_N LOW.

Partial Scan Examples

The MT9M413 can be partially scanned by subsampling rows. The user may select which rows and how many rows to include in a partial scan. For example, with a 66 MHz clock, a row time is approximately 2 microseconds (µs), resulting in the following possibilities:

- 1 row in frame: 500,000 frames per second
- 2 rows in frame: 250,000 frames per second
- 10 rows in frame: 50,000 frames per second
- 100 rows in frame: 5,000 frames per second
- 256 rows in frame: 2,000 frames per second
- 512 rows in frame: 1,000 frames per second
- 1,024 rows in frame: 500 frames per second ... and so on

Table 5: Pin Descriptions

Pin Number(s)	Signal Name	Function
	DATA [99:0]	Pixel data output bus that is 10 pixels (100 bits) wide. Bit 0 is the LSB (least significant bit) of the lowest order pixel (see Table 4, "Pixel Array," on page 11). In the group of 10 pixels being output, bit 9 is the MSB (most significant bit).
T13	DATA0	
U14	DATA1	
V15	DATA2	
T14	DATA3	
V16	DATA4	
T15	DATA5	
U16	DATA6	
R14	DATA7	
V18	DATA8	
P15	DATA9	
D14	DATA10	
A16	DATA11	
C16	DATA12	
E13	DATA13	
D15	DATA14	
A18	DATA15	
E14	DATA16	
B18	DATA17	
D17	DATA18	
E16	DATA19	
W11	DATA20	
U10	DATA21	
V11	DATA22	
R11	DATA23	
V12	DATA24	
W13	DATA25	

Table 5: Pin Descriptions (continued)

Pin Number(s)	Signal Name	Function
U12	DATA26	
V13	DATA27	
R12	DATA28	
V14	DATA29	
B11	DATA30	
C12	DATA31	
A12	DATA32	
B12	DATA33	
E11	DATA34	
B13	DATA35	
C14	DATA36	
D13	DATA37	
E12	DATA38	
C15	DATA39	
U6	DATA40	
V7	DATA41	
T8	DATA42	
R9	DATA43	
V8	DATA44	
U8	DATA45	
V9	DATA46	
T9	DATA47	
V10	DATA48	
R10	DATA49	
C8	DATA50	
A7	DATA51	
D9	DATA52	
E9	DATA53	
A8	DATA54	
C10	DATA55	
A9	DATA56	
D10	DATA57	
B10	DATA58	
C11	DATA59	
T4	DATA60	
R6	DATA61	
V3	DATA62	
W3	DATA63	
R7	DATA64	
W4	DATA65	
T6	DATA66	
V5	DATA67	
R8	DATA68	
V6	DATA69	
E6	DATA70	
D5	DATA71	

Table 5: Pin Descriptions (continued)

Pin Number(s)	Signal Name	Function
C5	DATA72	
D6	DATA73	
A3	DATA74	
C6	DATA75	
D7	DATA76	
A5	DATA77	
E8	DATA78	
A6	DATA79	
M5	DATA80	
P2	DATA81	
N3	DATA82	
T1	DATA83	
P3	DATA84	
U1	DATA85	
P4	DATA86	
T2	DATA87	
V1	DATA88	
R4	DATA89	
H5	DATA90	
E3	DATA91	
E2	DATA92	
D1	DATA93	
D3	DATA94	
E4	DATA95	
C2	DATA96	
A1	DATA97	
F5	DATA98	
B2	DATA99	
L3	CAL_DONE_N	A two-clock cycle-wide active-low pulse that indicates the ADC has completed its calibration operation.
L2	CAL_STRT_N	Starts the calibration process for the ADC. This is a two-clock cycle-wide active-low pulse.
F1	DARK_OFF_EN_N	A low input enables common mode dark offset to all pixels. The value of the offset is defined by VREF3 and VCLAMP3. Subtracts a fixed offset pre-ADC. Signal is pulled-up on-chip.
J4, N15, J16	VDD	Power supply for core digital circuitry.
H3, H18, T18	DGND	Ground for core digital circuitry.
K2	LD_SHFT_N	An active-low envelope signal that places the recently converted row of data into output register for output, enables the sense amps and resets the column counter.
J3	DATA_READ_EN_N	An active-low envelope signal that enables the column counter and causes the 10 10-bit output ports to be updated with data on the rising edge of the system clock. Column counter skips data when this input is HIGH.
L1	LRST_N	Global logic reset function (asynchronous). Active-low pulse.
	ROW_ADDR [9:0]	A 10-bit bus (0 to 1023, bottom to top) that controls which pixel row is being processed or read out. An asychronous (unclocked) digital input. Bit 9 is the MSB.
G18	ROW_ADDR0	
H16	ROW_ADDR1	
H15	ROW_ADDR2	

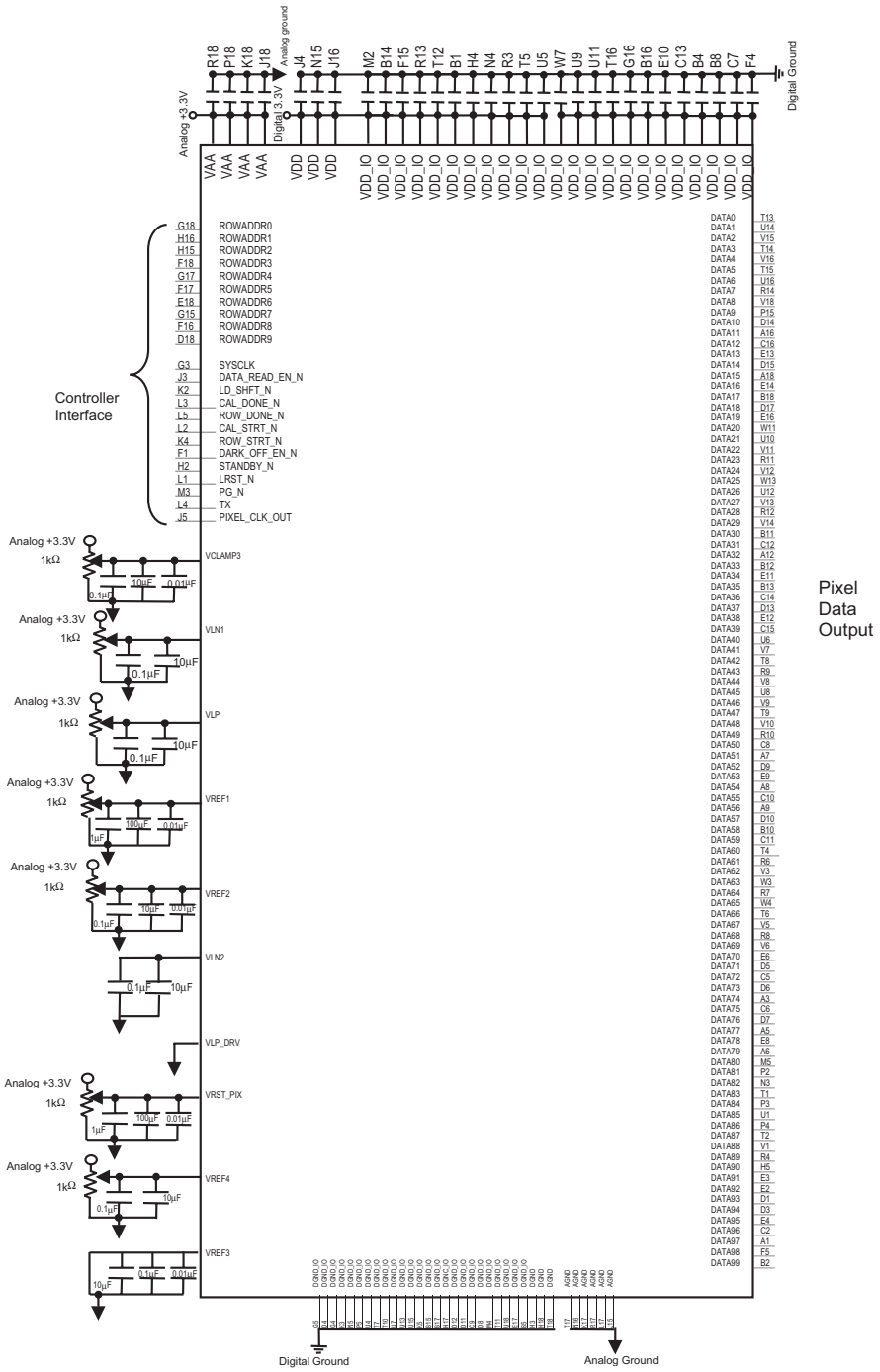
Table 5: Pin Descriptions (continued)

Pin Number(s)	Signal Name	Function
F18	ROW_ADDR3	
G17	ROW_ADDR4	
F17	ROW_ADDR5	
E18	ROW_ADDR6	
G15	ROW_ADDR7	
F16	ROW_ADDR8	
D18	ROW_ADDR9	
L5	ROW_DONE_N	A two-cycle-wide pulse that indicates that processing of the currently addressed row has been completed.
K4	ROW_STRT_N	Starts ADC conversion of the pixel row (defined by the row address) content. A two-clock cycle-wide active-low pulse.
H2	STANDBY_N	A low input sets the sensor in a low power mode (allow 1 microsecond before calibrating, after coming out of this mode). Signal is pulled-up on-chip.
J5	PIXEL_CLK_OUT	Data synchronous output. User may prefer to use this pin as data clock instead of SYSCLK.
G3	SYSCLK	Clock input for entire chip. Maximum design frequency is 66 MHz (50%, ±5%, duty cycle).
G16, E10, C13, B4, B8, C7, F4, M2, B14, F15, R13, T12, B1, H4, N4, R3, T5, U5, W7, U9, U11, T16, B16	V_{DD}_IO	Power supply for digital pad ring.
G5, D4, G4, K3, N5, P5, U4, T7, T10, U7, U13 K5, B15, B17, H17, D12, D11, E17, C9, D8 M4, T11,U18, B5,U15	D_{GND}_IO	Digital ground for pad ring.
R18, P18, K18,J18	V_{AA}	Power supply for analog processing circuitry (column buffers, ADC, and support).
T17, N16, L17, K17, J15, R17	A_{GND}	Ground for analog signal processing circuitry.
L15	VLN1	Bias setting for pixel source follower operating current. Impedance: 3kΩ, 10pF. Aptina recommends decoupling capacitors.
M18	VLN2	The bias setting for the ADC is generated on-chip. Aptina recommends a decoupling capacitor to ground. External biasing may be preferable to optimize performance. Impedance: 3kΩ, 10pF.
N17	VLP	Bias setting voltage for the column source follower operating current. Impedance: 3kΩ, 10pF. Aptina recommends a decoupling capacitor.
K16, M15	V_{REF}1	ADC reference input voltage that sets the maximum input signal level (defines the level where the FF code occurs) and thus sets the size of the least significant bit (LSB) in the analog to digital conversion process. A smaller V_{REF}1 produces a smaller LSB, which means a smaller analog signal level input is required to produce the same digital code out. Likewise, a larger V_{REF}1 produces a larger LSB, which means a larger analog signal level input is required to produce the same digital code out. Thus the reference value can be used like a global gain adjustment (halving this voltage doubles the gain). This signal has two pin connections to minimize internal losses during high speed operation. User voltage source must supply a transient current of 100mA at a frequency of 500 kHz with a 2% duty cycle. Decoupling capacitors to A_{GND} of ~1?F (ceramic) and 100?F (electrolytic) placed as close to the package pins as possible are usually sufficient to filter out this required current transient.

Table 5: Pin Descriptions (continued)

Pin Number(s)	Signal Name	Function
P17	VREF2	ADC reference used for the calibration operation. User voltage source must supply a transient current of 20mA at a frequency of 500 kHz with a 2% duty cycle. A ceramic decoupling capacitor to AGND of ~0.1µF is usually sufficient to filter out this required current transient.
M16	VREF3	Dark offset cancellation positive input reference, tied to the pedestal voltage to be added to the signal.
K15	VCLAMP3	Dark offset cancellation negative input reference. User voltage source must supply a transient current of 40mA at a frequency of 500 kHz with a 2% duty cycle. A ceramic decoupling capacitor to AGND of ~0.1µF to 1µF is usually sufficient to filter out this required current transient.
R16	VLP_DRV	Should be connected to AGND.
L4	TX_N	This is an active low pulse that controls transfer of charge from photodetector to memory inside each pixel for entire pixel array.
M3	PG_N	This is an active low pulse that resets the photodetectors and thereby starts new integration cycle.
L18, P16, J17	VRST_PIX	Power supply for pixel array. There is no noticeable DC power consumption by this pin (<100?A). User voltage source must supply a transient current of 10mA at a frequency of 500 kHz, once a frame. Decoupling capacitors to AGND ~1µF (ceramic) and 100?F (electrolytic) are usually sufficient to filter out this required current transient.
L16	VREF4	ADC reference input value should be 1/4 VREF1. User voltage source must supply a transient current of 100mA at a frequency of 500 kHz with a 2% duty cycle. A ceramic decoupling capacitor to AGND of ~0.1µF is usually sufficient to filter out this required current transient.
E5,C3,C1, D2, E1,F2, F3, G1, H1, J2, J1, K1, M1, N1, N2, P1,R1, R2, T3, U2, R5, U3, V2, W2, W1, V4, W5, W6, W8, W9, W10,W12, W14, W15, W17, W18, V17, R15, U17, V19, W19, U19, T19, R19, P19, N18, N19, M19, M17, L19, K19, J19, H19, G19, F19, E19, D19, C19, B19, C18, E15, C17, D16, A19, A17, A15, A14, A13, A11, A10, B9, B7, B6, A4, E7, A2, C4, B3, W16, G2		No connect.

Figure 12: Board Connections



Notes:
1. Aptina recommends that 0.01µF and 0.1µF capacitors be placed as physically close as possible to the MT9M413's package.
2. Alternatively, the analog voltages depicted as being generated from potentiometers could be supplied from DACs.
3. The analog voltages VLN1, VLN2, VLP, and VREF4 are generated on-chip, but user may supply voltages to override the internal biases.

Analog Voltage Setting Considerations

The values suggested in the Typical Values column in the "AC Electrical Characteristics" on page 34 should be the starting point for setting the analog voltages. Additionally, it is useful to refer to the "Signal Path Diagram" on page 6, which indicates how the analog voltages affect the image. Other considerations are as follows:

- VREF1:
  This ADC reference voltage can also be utilized as a gain. A lower value will increase gain, but also results in amplification of nonuniformities.

- VREF4:
  Should always be set to ¼ of VREF1.

- VREF2:
  Reference used for the ADC calibration to remove column-wise FPN. If set much lower than the typical value there is a possibility that some column nonuniformities will not be corrected. Setting higher than typical will result in more column-wise FPN. When debugging analog voltage settings it may be useful to temporarily set VREF2 to zero, effectively stopping the ADC calibration process and adjusting the VLN/VLP settings.

- VLN1:
  The on-chip generated voltage should be used as the starting point; increasing above typical will result in an increase in current, speed, and FPN in the first buffer.

- VLN2:
  The on-chip generated voltage should be used as the starting point. Controls the current in the ADC comparators (there is a safe range where this voltage has no effect); above or below this range will cause the comparators to fail. If vertical white stripes appear in the center of the imaging area or random white spots appear in contour areas, it is an indication that VLN2 needs to be adjusted.

- VLP
  The on-chip generated voltage should be used as the starting point.

- VRST_PIX
  Voltage for pixel reset. If this is too close to VAA the image will be degraded and is not recommended to be above 2.9V, but if it is set too low the pixel dynamic range may decrease.

- VREF3 and VCLAMP3
  These control the offset as shown in the "Signal Path Diagram" on page 6. This must be enabled through DARK_OFF_EN_N; Offset is ~ (VREF3-VCLAMP3)/20.

Lens Selection

Much of the specific information in this section is explained in detail at http://www.aptina.com/products/imaging/technology/index.html on our Web site. The following information applies specifically to the MT9M413 megapixel image sensor.

Format

The diagonal of the image sensor array, 19.67mm, fits most closely, but not exactly, within the optical format corresponding to the 1–inch specification. Some 1-inch optical format lenses have been shown to work well with this sensor. Typical 1-inch lens examples are Computer V2513, V5013, and V7514. F–mount lenses provide another possible lens solution due to their large image circle.

Mounting

Several lens mounting standards exist that specify the threading of the lens' barrel as well as the distance the back flange of the lens should be from the image sensor for the lens to properly form an image. Typical lens mounting standards for the MT9M413 are shown in Table 6.

Table 6: Lens Mounting Standards

Mount	Mounting	
Name	Threads	Back-Flange-to-Image Sensor
C	1–32	17.526mm
CS	1–32	12.5mm

Another option is to use a C–mount together with a C– to F–mount adapter for greater lens flexibility.

Field of View and Focal Length

The field of view of an imaging system will depend on both the focal length of the imaging lens and the width of the image sensor. As most of the image information humans pay attention to generally falls within a 45–degree horizontal field of view, many camera systems attempt to imitate this field of view. However, in some cases a telephoto system (with a narrow field of view, say less than 20 degrees), or a wide angle system (with a wide field of view, say more than 60 degrees) may be desired. The approximate field of view that an imaging system can achieve is shown in Equation 1:

(EQ 1)

$$\theta \approx 2\tan^{-1}\left(\frac{w}{2f}\right)$$

where θ is the field of view, $\tan^{-1}$ is the trigonometric function arc-tangent, w is the width of the image sensor, and f is the focal length of the imaging lens. For example, the imaging system's diagonal field of view can be determined by using the diagonal of the image sensor (19.67 mm) for w and a particular lens' focal length for f. Alternatively, the imaging system's horizontal field of view can be determined by using the horizontal of

the image sensor (15.36 mm) for w and a particular lens' focal length for f. A lens with an approximately 50 mm focal length will provide an 18-degree horizontal field of view with a MT9M413 (keep in mind that the above equation is a simplified approximation).

F-Number

The f-number, or f-stop, of an imaging lens is the ratio of the lens' focal length to its open aperture diameter. Every doubling in f-number reduces the light to the sensor by a factor of four. For example, a lens set at f/1.4 lets in four times more light than that same lens when it is set at f/2.8. Low f-number lenses capture a lot of light for delivery to the image sensor, but also require careful focus. Higher f-number lenses capture less light for delivery to the image sensor, and do not require as much effort to bring the imaging system to focus. Low f-number lenses generally cost more than high f-number lenses of similar overall performance. Typical f-numbers for various imaging systems are:

Table 7: Typical F-Numbers

F-Stop	Imaging Application
1.4	Low-light level imaging, manual focus systems.
2.0	Typical for PC and other small form cameras.
2.8	Common in digital still cameras.
4.0+	Often used in machine vision applications.

MTF

Modulation Transfer Function (MTF) is a technical term that quantifies how well a particular system propagates information. For cameras, the “system” is the lens and the sensor, and the “information” is the picture they are capturing. MTF ranges from zero (no information gets through) to 100 (all information gets through), and is always specified in terms of information density. In most imaging systems, the MTF is limited by the performance of the imaging lens. A lens must be able to transfer enough information to the image sensor to be able to resolve details in the image that are as small as the pixels in the image sensor. The pixels are set on a 12-micron pitch (the center of one pixel is 12 microns from the center of its neighboring pixel). Thus, a lens used should be able to resolve image features as small as 12 microns. Typically, a lens' MTF is plotted as a function of the number of line pairs per millimeter the lens is attempting to resolve (more line pairs per millimeter mean higher information densities). For an electronic imaging system, one line pair will correspond to two image sensor pixels (each pixel can resolve one line). This is equated as shown in Equation 2:

(EQ 2)

$$\frac{LP}{mm} = \frac{1}{2z}$$

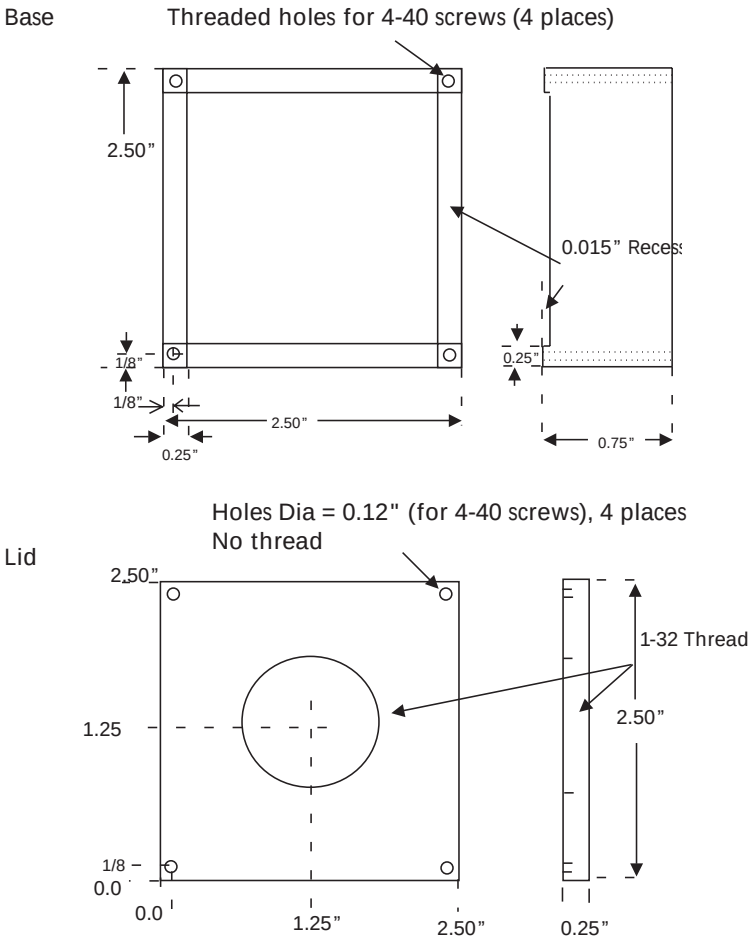
where LP/mm means line pairs per millimeter and z is the image sensor's pixel pitch, in millimeters. For the MT9M413, z = 0.012 mm, such that the MT9M413 has 42 LP/mm. Thus, a lens should provide an acceptable level of MTF all the way out to 42 LP/mm. For

most lenses, the MTF will be highest in the center of the images they form, and gradually drop off toward the edges of the images they form. As well, MTFs at low values of LP/mm will generally be larger than MTFs at high values of LP/mm. One of the many trade-offs that must be decided by the end user is how high the MTF needs to be for a particular imaging situation. Generally, near an image sensor's LP/mm good MTFs are higher than 40, moderate MTFs are from 20 to 40, and poor MTFs are less than 20.

Infrared Cut-Off Filters

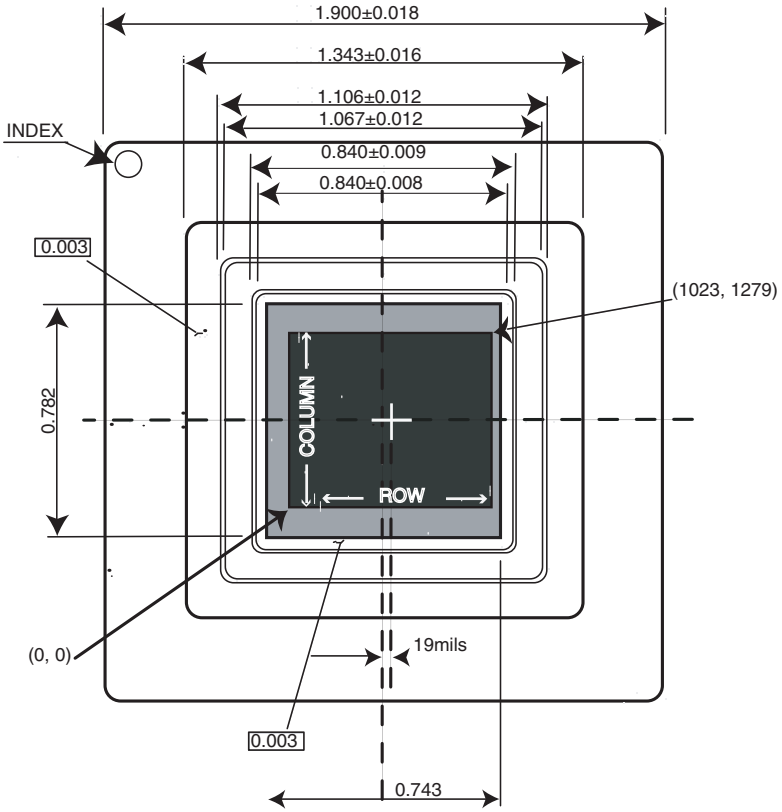
In most visible imaging situations it is necessary to include a filter in the imaging path that blocks infrared (IR) light from reaching the image sensor. This filter is called an IR cut-off filter. Various forms of IR cut-off filters are available, some absorptive (like Hoya's CM500 or Schott's BG18) and some reflective (for example, dielectric stacks). Infrared light poses a problem to visible imaging because its presence blurs and decreases the MTF in the images formed by a lens. Since human vision only extends across a narrow range of the electromagnetic spectrum, camera systems hoping to capture images that look like the images our eyes capture must not capture light outside of our vision range. Silicon-based light detectors (like the ones in the MT9M413's pixels) detect light from the very deep blue to the near infrared. Thus, a filter must exist in the light's path that keeps the infrared from reaching the image sensor's pixels. In most cases, it is important that such a filter begin blocking light around 650 nm (in the deep red) and continue blocking it until at least 1100 nm (in the near IR). In most camera systems, the IR cut-off filter is included in the imaging lens. However, this point must be verified by a lens vendor when a particular lens is chosen for use with an image sensor.

Figure 13: C-Mount Lens Shroud for MT9M413 and Socket



Notes: 1. This shroud is designed to accommodate the MT9M413 when it is inserted into a PGA socket. These dimensions are based on the MILL MAX #510-93-281-19-081003 socket (www.mill-max.com).

Figure 14: 280-Pin Ceramic PGA Package Top View



Notes:
1. Sensor is centered on package, pixel array is off-center.
2. Die offset is ±10 mils in both the X and Y directions.
3. Die rotation is ±2 degrees.

Figure 15: 280-Pin Ceramic PGA Package Side View

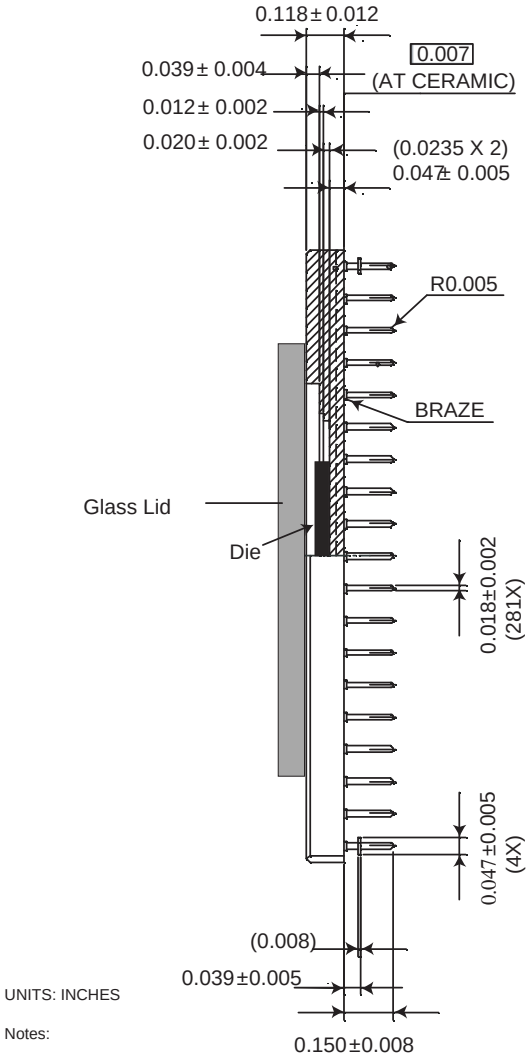
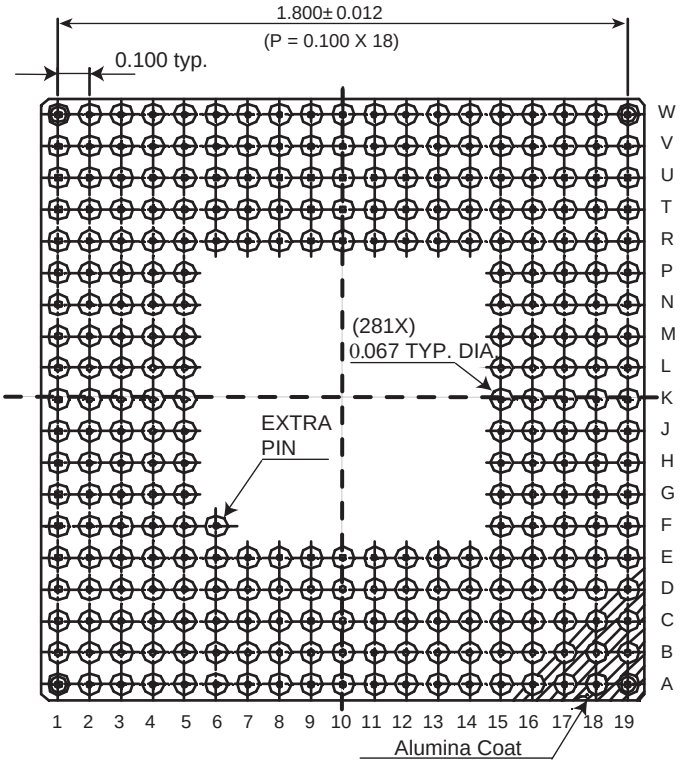


Figure 16: 280-Pin Ceramic PGA Package Bottom View



Optical Specification

Table 8: Image Sensor Characteristics
T_A = 25°C

Symbol	Parameter	Typ	Unit	Note
^{R}I	Responsivity (ADC VREF = 1V)	1600	LSB/lux-sec	
Nsat	Pixel saturation level	63,000	e^-	
NADC	DC noise + DNL	±2	LSB p-p	
DSNU, HF	Dark signal non-uniformity, high spatial frequency	<0.4	% rms	1
DSNU, LF	Dark signal non-uniformity, low spatial frequency	<1.5	% p-p	2
Vdrk	Output referred dark signal	50	mV/sec	
NE	Input referred noise	70	e^-	
Dyn_I	Internal dynamic range	59	dB	
PRNU, HF	Photo response non-uniformity, high spatial frequency	<0.6	% rms	1
PRNU, LF	Photo response non-uniformity, low spatial frequency	<10	% p-p	2
Kdrk	Dark current temperature coefficient	100	%/8°C	
Cg	Conversion gain	13	$\mu V/e^-$	

Notes:
1. Calculation method for high frequency PRNU and DSNU:
   For PRNU, uniformly adjust illumination so that the average voltage across a sensor partition is Full Scale/2.
   For DSNU, block illumination to sensor. Integration time = 2ms.
   Calculate spatially-filtered average using 64 pixel square window.
   Calculate r.m.s. difference between pixel values and corresponding filtered average values. Calculate average r.m.s. between windows.
2. Calculation method for low frequency PRNU and DSNU:
   For PRNU, uniformly adjust illumination so that the average voltage across a sensor partition is Full Scale/2.
   For DSNU, block illumination to sensor. Integration time = 2ms.
   Calculate spatially-filtered average using 64 pixel square window
   Calculate difference between the center pixel value and corresponding filtered average values. Report peak-to-peak values between windows.

Figure 17: Pixel Array Layout

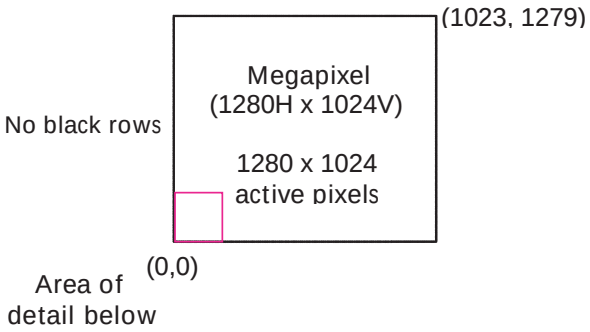


Figure 18: Bayer Pattern (Pixel Color Pattern Detail)

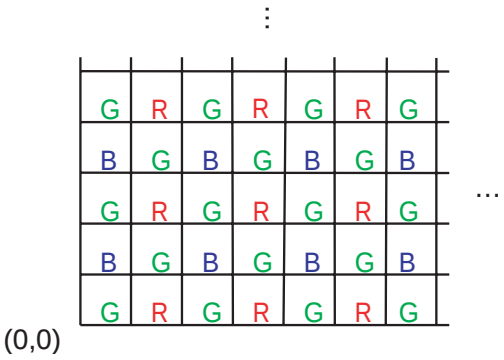


Figure 19: Quantum Efficiency (color)

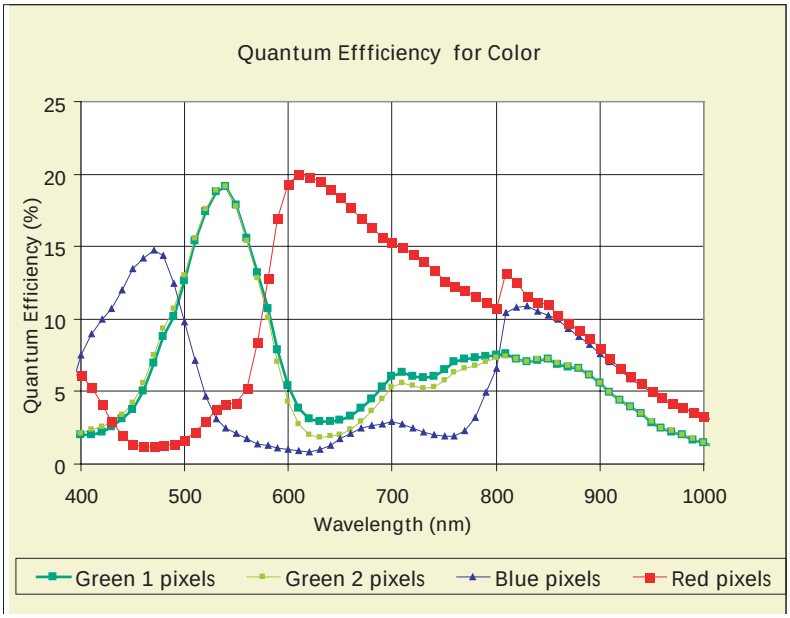
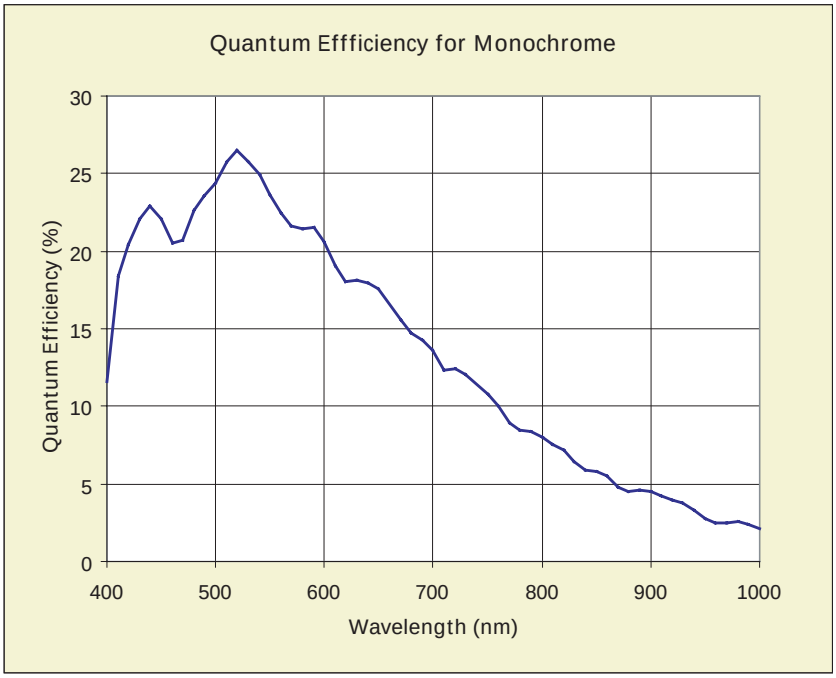


Figure 20: Quantum Efficiency (monochrome)



Electrical Specifications

Table 9: AC Electrical Characteristics
V_{SUPPLY} = 3.3V ± 0.3V

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
T_{PLH}	Data output propagation delay for LOW to HIGH trans.		1	2	3	ns
T_{PHL}	Data output propagation delay or HIGH to LOW trans.		1	2	3	ns
T_{SETUP}	Setup time for input to SYSCLK	V_{IN} = V_{PWR} or V_{GND}	3	4		ns
T_{HOLD}	Hold time for input to SYSCLK	V_{PWR} = Min, V_{OH} min	3	4		ns

Figure 21: Set Up and Hold Time

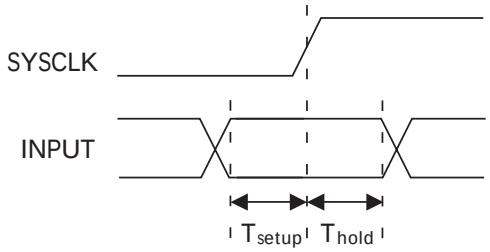


Figure 22: Clock to Data Propagation Delay

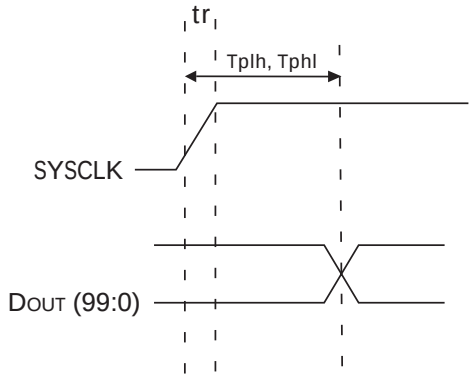


Table 10: DC Electrical Characteristics
Vsupply = 3.3V ± 0.3V

Symbol	Characteristic	Condition	Min	Typ	Max	Unit	Note
V_{LP}	Bias for column buffers		0.5	1.9	2.7	V	
VREF1	Reference for ADC		0.2	1.0	1.5	V	
VREF2	Reference for ADC calibration		0.3	0.8	1.5	V	
VREF3	Dark offset		0	0.6	2.5	V	
VLN1	Bias for pixel source follower		0.8	1.0	1.1	V	
VLN2	Bias for ADC		0.8	1.0	1.1	V	
VCLAMP3	Dark offset		0	0	3.0	V	
VLP_DRV	Row driver control	Grounded	0	0	0	V	
VRST_PIX	Pixel array power		2.2	2.7	2.9	V	
VREF4	Reference for ADC			0.25		V	
V_{IH}	Input HIGH voltage		2.0		V_{PWR} + 0.3	V	
V_{IL}	Input LOW voltage		–0.3		0.8	V	
I_{IN}	Input leakage current, no pull-up resistor	V_{IN} = V_{PWR} or V_{GND}	–5		5	?A	
V_{OH}	Output HIGH voltage	V_{PWR} = Min, I_{OH} = 100?A			V_{PWR} – 0.2	V	
V_{OL}	Output LOW voltage	V_{PWR} = Min, I_{OL} = 100?A			0.2	V	
I_{PWR}	Maximum supply current	66 MHz clock, 5pF load on outputs		165		mA	1

Notes: 1. I_{PWR} = I (V_{DD}_IO) + I (V_{DD}) + I (V_{AA}).

Table 11: Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{PWR}	DC supply voltage	3.00	3.6	V
T_A	Commercial operating temperature	–5	60	°C

Note: This device contains circuitry to protect the inputs against damage from high static voltages or electric fields, but the user is advised to take precautions to avoid the application of any voltage higher than the maximum rated.

Table 12: Power Dissipation
V_{PWR} = 3.3V; T_A = 25°C at 500 fps

Symbol	Parameter	Min	Typ	Max	Unit
P_{AVG}	Average power	250	350	500	mW

Environmental

Caution **Stresses greater than those listed may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**

Table 13: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{PWR}	DC supply voltage	–0.5 to 3.6	V
V_{IN}	DC input voltage	–0.5 to V_{PWR} + 0.5	V
V_{OUT}	DC output voltage	–0.5 to V_{PWR} + 0.5	V
I	DC current drain per pin (any I/O)	±50	mA
I	DC current drain, V_{PWR} and V_{GND}	±100	mA
$T_{STORAGE}$	Storage temperature range	–40 to 125	°C
T_{LEAD}	Lead temperature (10 second soldering)	235 max.imum	°C

Notes:
1. V_{PWR} = V_{DD} = V_{AA} = V_{DD_IO} (V_{DD} is supply to digital circuit, V_{AA} to analog circuit).
   V_{GND} = D_{GND} = A_{GND} (D_{GND} is the ground to the digital circuit, A_{GND} to the analog circuit).
2. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Revision History

Rev. C 9/10

- Updated to non-confidential

Rev. B 5/10

- Updated to Aptina template

Rev. A 1/8/2008

- Initial release.

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