Ambarella A5s66

High-Performance Digital Media System-On-Chip (SoC)

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Confidentiality Notice:

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1 General Description

1.1 Overview

The A5s family of digital media system-on-chip (SoC) solutions represents the state-of-the-art in embedded video processing. It offers ultra-low power operations while integrating an image sensor processor (ISP), high-quality H.264 encoding/decoding, and a high-performance ARM11 CPU.

The A5s66 is the performance value member of the A5s family, delivering H.264 encoding at full HD (1920x1080p30), providing an efficient platform for 1080p IP cameras.

For IP Camera designers, the A5s family enables a low-power, small-footprint system where a rich set of peripheral I/O simplifies interconnectivity and a fully-featured SDK provides the basis for efficient product development. A high-speed image sensor interface supports a wide range of CMOS sensors, while a powerful image pipeline applies innovative processing to deliver clear images even in challenging conditions. Such innovations include 14-bit processing, Local Exposure Correction for improved dynamic range, and 3D noise reduction using Motion Compensated Temporal Filter (MCTF) for improved low-light capabilities.

The video compression subsystem features low-delay, high-quality H.264 and MJPEG encode/decode with multiple independent video streams. Based on Ambarella's award-winning broadcast encoder technology, A5s offers industry-leading video quality at very low bitrates.

The A5s CPU is a 528 MHz ARM1136J-S that controls high-level operations and supervises the image sensor and video compression subsystems. All these computationally intensive functions are implemented in special hardware units (which can be programmed to user specifications), allowing the ARM to be free for user applications

1.2 Feature Summary

- ARM1136J-S Processor Core
  - Clock frequency up to 528 MHz
  - 16 KB Data Cache, 16 KB Instruction Cache
  - Internal memory management unit (MMU)
- Image Sensor Processing Subsystem (iDSP)
  - 3D noise reduction with MCTF
  - Local Exposure Correction
  - AE and AWB with histograms and statistics
  - Video stabilization support
  - Smooth digital zoom
  - OSD with alpha-blending for text, time, logo and privacy masking

- Video Processing Subsystem (vDSP)
  - Baseline and Main Profile H.264 @ L4.1 encode /decode
  - Simultaneous1920x1080p30 and VGAp30 H.264 encode
  - MJPEG at 10 fps
  - JPEG processing up to 90 Megapixels/s
- Sensor /Video Input Interface
  - Parallel interface
  - MIPI CSI-2 interface, up to 3 lanes
  - CCIR601 / CCIR656 video input
- Video Output Interface
  - NTSC/PAL analog output
  - CCIR601 type YUV output (16-bit mode)
  - HDMI 1.3a transmitter
- Memory Interface
  - Single 16-bit SDRAM for full feature set
  - Support for DDR2 / DDR3
- Flexible Storage Media Interface (SMIO)
  - NAND, CF, SD/MMC
  - Additional SDIO interface
  - Support for Micro Drive hard drive (IDE)
  - NAND or USB initiated Boot
- I2S Audio Interface
  - AAC, G.711 and G.726
- USB2.0 HS device supported with embedded transceiver
- 16-bit Parallel Host Interface to connect to optional system host
- General Interface Ports
  - SSI/SPI interface (3)
  - UART (2)
  - Two wire serial interface, IDC (3)
  - JTAG for debugging (1)
- 5 PWM control outputs
- 4 input ADC channels
- Real Time Clock (RTC)
- Built-in power controller for power up/down sequencing
- GPIO - Up to 88 GPIO pins
- Stepper Motor Interface (3 sets)
- Watchdog Timer (1)
- General Purpose Timers for Waveform Generation and Event Monitoring (3)
- 404-ball FBGA Package, 15mm x 15mm

2 Block Diagram

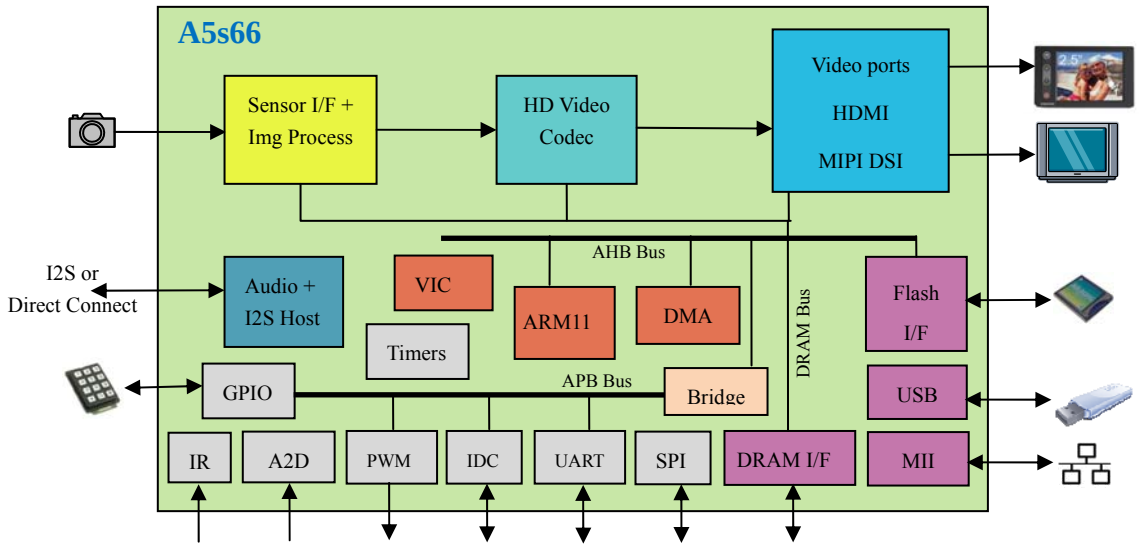


Figure 1. A5s66 Block Diagram

3 Interface Description

3.1 DRAM

The A5s66 supports DDR2 or DDR3 SDRAM interface with a 16-bit data bus up to 336MHz. A5s66 supports programmable IO strength.

3.2 Video Output

There are 5 video output ports on A5s66 (1 Analog, 1 HDMI and 2 Digital YUV/RGB, 1 MIPI DSI). These 5 physical ports are fed by 2 logical video channels as shown below.

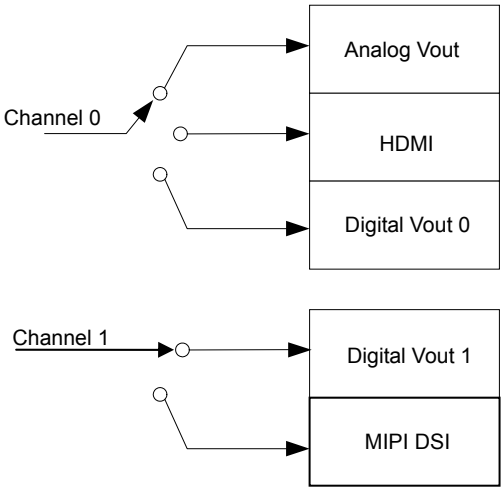


Figure 2. Video Channels and Ports

Channel 1 can drive only one of either the Digital Vout1 port or the MIPI DSI port. Channel 0 may drive all the ports it is feeding at the same time.

Channel 0 can drive resolutions up to 1920x1080i60 while channel 1 can drive 1280x720p30 or lower. Please see port specific restrictions below.

3.2.1 Analog Video Output

The A5s66 video DAC can drive standard-definition video outputs in Composite format. Care should be taken to make sure the output signals are not overloaded causing the picture to be darker.

3.2.2 Digital Video Output

There are two digital video output ports (24-bit parallel output for Channel 1 and 16-bit parallel for channel 0), which can be used simultaneously. One output (port 1) is dedicated for LCD display (preview screen), and the other (port 0) can be enabled for TV out. A5s66 supports various output modes: 16-bit {CbY, CrY} , LCD-RGB, CCIR601 and CCIR656.

For 16b YCbCr mode the following mapping of pins is applied:

Bit field	Mapped To Signal	Notes
VD*_OUT[15:8]	Y	
VD*_OUT[7:0]	Cb, Cr	4:2:2 output format

For 8b YCbCr modes the following mapping of pins is applied:

Bit field	Mapped To Signal	Notes
VD*_OUT[7:0]	Cb, Y, Cr, Y	Output pixel rate is ½ the output clock rate

For 8b RGB modes the following mapping of pins is applied:

Bit field	Mapped To Signal	Notes

VD*_OUT[7:0]	R, G, B	

For 24-bits RGB output to LCD the following mapping of pins is applied:

Bit field	Mapped To Signal	Notes
VD1_OUT[23:16]	R or Cr	
VD1_OUT[15:8]	G or Y	
VD1_OUT[7:0]	B or Cb	

Please refer to the software programmer's manual for more detailed information.

3.2.3 HDMI Output

A5s66 has an embedded HDMI 1.3a Transmitter. 3 lanes of differential TMDS data plus one clock lane for a data rate of 742.5Mbps.

3.2.4 MIPI DSI Output/Input

The A5s66 supports 1 single lane MIPI DSI output interface to external devices. An additional MIPI DSI input lane is provided to bypass inputs from this input channel to the MIPI DSI output channel. This bypass path may be used to connect the system host to the MIPI devices connected to the output interface.

3.2.5 Summary of Supported Video Format Per Output Port

√ – supported; x – not supported.

Video Format		Analog	HDMI	Digital Video		MIPI DSI
		Composite		Output 0	Output 1	
SD	720x480i60	√	√	√	√	√
	720x480i59.94	√	√	√	√	√
	720x576i50	√	√	√	√	√
	720x480p30/29.97	x	x	√	√	√
ED	720x480p60	x	√	√	√	√

	720x480p59.94	x	√	√	√	√
	720x576p50	x	√	√	√	√
HD	1280x720P30	x	√	√	√	√
	1920x1080P30	x	√	√	x	x
	1280x720p60	x	√	√	x	x
	1280x720p59.94	x	√	√	x	x
	1280x720p50	x	√	√	x	x
	1920x1080i60	x	√	√	x	x
	1920x1080i59.94	x	√	√	x	x
	1920x1080i50	x	√	√	x	x

3.3 Video Input

A5s66 has two video input ports, Sensor Video Input (LVDS/LVCMOS) and MIPI Serial Input. Both ports connect to the same video input channel and so cannot be used at the same time, even though the MIPI and LVDS pins can be hooked up to different video sources on the board.

3.3.1 Sensor Input

Sensor interface supports parallel (1.8V LVCMOS, single or dual pixel) and multi-lane serial (SLVS/MLVS or LVDS) signaling. Note that the sensor inputs can range from 1.8V to 3.3V in LVCMOS mode. However, when the sensor interface clock and sync signals are driven by A5s66, their voltage range is 2.8V to 3.3V. For 1.8V sensors, an external voltage divider must be used to limit the swing to 1.8V.

For the LVDS/SLVS interface, 1 clock is used for every 4 lanes of data (in general, see exception* below). The mapping of the clocks to the lanes is:

Number of Data Lanes Used	Mapping	
	Clock	Data Lanes
2	SPCLK_LVDS_P/N_0	SP_LVDS_P/N_[1:0]
4	SPCLK_LVDS_P/N_0	SP_LVDS_P/N_[3:0]
8	SPCLK_LVDS_P/N_0 SPCLK_LVDS_P/N_1	SP_LVDS_P/N_[7:0]

*Sensors with only one clk (e.g. Sony IMX039)	SPCLK_LVDS_P/N_0	SP_LVDS_P/N_[7:0]

The A5s66 sensor input port supports 4 video input modes, with the configurations described below.

1. **1-pixel LVCMOS**

   Source: Micron 10M, Micron 5M and OV2715 etc.

   Port: Sensor Input

   - Pixel clock: SPCLK_LVDS_P_0 (_0 is master clk; leave _1 unconnected)
   - Pixel data[7:0] : SD_LVDS_P_7 : SD_LVDS_P_0
   - Pixel data[13:8]: SD_LVDS_N_5 : SD_LVDS_N_0
   - Hsync: SD_LVDS_N_6
   - Vsync: SD_LVDS_N_7
   - Sfield: SDCLK_LVDS_N_1
   - If the sensor is in slave mode, the Hsync and Vsync outputs from A5s66 are on SHSYNC and SVSYNC.

2. **External 8-bit YUV Source (LVCMOS mode only)**

   Source: HDMI daughter card

   Port: Sensor Input

   - Connect pixel data [7:0] to SD_LVDS_P_[7:0]
   - Use SPCLK_LVDS_P_0 for pixel clock (_0 is master; leave _1 unconnected)
   - Hsync and Vsync in SP_LVDS_N_6/7.
   - Sfield is in SPCLK_LVDS_N_1.

3. **External 16-bit YUV Source (LVCMOS mode only)**

   - Use SPCLK_LVDS_P_0 for pixel clock (_0 is master; leave _1 unconnected)
   - Connect pixel data [7:0] to SD_LVDS_P_[7:0]
   - Connect pixel data [15:8] to SD_LVDS_N_[7:0]
   - Sfield is in SPCLK_LVDS_N_1.
   - A5s66 only supports 16-bit YUV input with embedded sync (656 mode only, no 601 mode)

3.3.2 MIPI Serial Input

The A5s66 supports 1, 2 or 3-lane MIPI interface to compatible sensors. Raw-8, raw-10,

raw-12, raw14, yuv-422-8, and generic-8 data formats are supported.

- Connect clock to S_DPCLK/S_DNCLK
- Connect data lanes to S_DPDATA/S_DNDATA[2:0]

3.4 Audio I2S

A5s66 supports up to 6 channels of audio through the I2S digital audio interface to connect to an external analog codec or other audio device. 3 lanes of data are provided clocked by the same clock signal.

3.5 Ethernet

A5s66 provides an Ethernet Media Independent Interface (MII) interface to adapt to external PHY.

3.6 Host Interface

A5s66 has a Host Interface to connect to Intel or Motorola type host devices when the A5s66 is used as a coprocessor or support chip. The interface can be configured to run in burst mode (multiple words are transferred) or single word access mode. It is a 16-bit wide asynchronous interface that can achieve transfer rates up to 40MB/s.

3.7 USB

This is a USB 2.0 high-speed device interface with embedded transceiver. It is backward compatible to USB 1.1. The 24 Mhz system reference clock is used for USB PHY reference.

3.8 SMIO

Smart Media I/O supports any one of the following memory card interfaces: SD, SDIO, MMC, Memory Stick and CF. The same interface may be used to connect to NAND storage or to IDE Micro Drives.

3.9 ADC

A5s66 provides 4 channels of analog-to-digital converters.

3.10 SSI

A5s66 supports 3 different SSI interfaces.

- One SSI0 (Synchronous Serial Interface up to 27MHz) interface with 2 separate enable pins can control two different SSI devices.
- A high speed SSI2 (up to 54MHz) interface can control one additional SSI device.

- A slave-only SSI interface is also provided for external masters to connect to A5s66.

The interface timing is programmable. Please refer to the software programmer's manual for detailed information.

3.11 IDC

The IDC is a two-wire, bi-directional bus that provides data communication between the chip and peripheral devices with protocol speeds up to 400kbps. Two IDC ports are present. Note that the A5s66 IDC interface supports single master mode only.

3.12 UART

The two UARTs support asynchronous serial communication to Serial Ports. UART0 is normally used for debugging purposes and does not support hardware flow control. UART1 does support hardware flow control. Both support up to 115.2kbps baud rate, depending on software setting.

3.13 IR

One IR receiver interface for remote control. The IR pin receives in signals from IR module, and A5s66 decodes it through software programming.

3.14 GPIO

There are 88 GPIO pins which can be programmed to be general purpose in/out pins. Please refer to Appendix A for a full pin map and multiplexing information.

All GPIO pins are in Hi-Z state during reset assertion. All the GPIO pins are initialized to be inputs.

3.15 JTAG

A5s66 works with JTAG-ICE through this interface and doesn't support JTAG chaining.

3.16 RTC

A5s66 includes one 30-bit embedded RTC (Real Time Clock) with the following features: current time; alarm set; power-on and power-off sequence generation. A5s66 can keep the clock with the use of one dedicated always-on power supply pin. This block remains active even when the core power shuts off.

3.17 Power-On Configuration

Power-on-configuration may be done by settings on the pins, settings in an internal EEPROM

or by choosing a preconfigured option as described below. A total of 32 pins are utilized for setting the power-on configuration on the pins. They are multiplexed with the VD0_OUT[15:0] and VD1_OUT[15:0] pins. A5s66 latches the initial hardware setting at these pins right after POR_L deassertion. Alternately, one of 2 preconfigured power-on-config states, or the internal EEPROM state may be picked by setting only the pins VD1_OUT[14:13] as indicated below.

Initial Configuration Settings

PIN	Function	Setting
VD0_OUT0	Boot Media select	0:NAND flash 1: reserved, do not use
VD0_OUT[3:1]	IDSP/CORE/DRAM/SD/XM CLOCK CONFIG	**000:** 126 / 108 / 300 / 40.5 / 18.6 MHz **001:** 120 / 96 / 300 / 43.2 / 19.6 MHz **010:** 108 / 108 / 240 / 40.5 / 18.6 MHz **011:** 96 / 96 / 192 / 43.2 / 19.6 MHz **100:** 117 / 108 / 300 / 40.5 / 18.6 MHz **101:** 117 / 96 / 300 / 43.2 / 19.6 MHz **110:** 117 / 108 / 240 / 40.5 / 18.6 MHz **111:** 96 / 96 / 192 / 43.2 / 19.6 MHz
VD0_OUT4	PLL_UNLOCK_TRIG_RESET	0: disable generating grst when core pll out of lock(default) 1: enable generating grst when core pll out of lock.
VD0_OUT5	NAND Flash page size	See boot settings table below
VD0_OUT6	NAND read confirm	See boot settings table below
VD0_OUT7	Select ENET MII	0: disable 1: enable
VD0_OUT8	BOOT Bypass	0:disable (no boot bypass) 1:enable
VD0_OUT9	Flash fast boot mode	0:disable 1:enable
VD0_OUT10	IO FLASH BOOT	See boot settings table below
VD0_OUT11	SD BOOT	0: Use loader in EEPROM for SD Boot 1: Bypass the loader in EEPROM for SD Boot
VD0_OUT12	EMA_SEL	Set to 0 (default)
VD0_OUT13	ARM SYNC LOCK Mode	1: enable 0: disable
VD0_OUT14	ARM MODE CHANGE TRIG RESET	1: ARM mode change triggers grst
VD0_OUT15	Reserved	Set to 0 (Default)
VD1_OUT0	SPI_BOOT	See boot settings table below
VD1_OUT1	HIF_EN	0: disable 1:enable host interface
VD1_OUT2	Reserved	NC

VD1_OUT3	HIF_TYPE	0: Intel 1: Motorola
VD1_OUT4	RDY_PL	0:hif_rdy active low 1:hif_rdy active high
VD1_OUT5	RCT_AHB_HIF_SECURE_MODE	0: normal 1: secure mode
VD1_OUT6	Reserved	NC
VD1_OUT7	SELECT USBP EXT CRYSTAL	0: Choose internal clock for USBPHY 1: Choose external clock for USBPHY
VD1_OUT[9:8]	Reserved	Set to 0: default
VD1_OUT[10]	REF_CLK FOR USB	Uses ref_clk for gclk_usbphy
VD1_OUT[11]	BIRA EFUSE ENABLE	0 – normal bira efuse loading 1 – disable loading of bira efuse values
VD1_OUT[12]	Reserved	Set to 0: default
VD1_OUT[14:13]	SYS_CONFIG	Preprogrammed power-on option; Set to 00 to use power-on-config as described above.
VD1_OUT[15]	Config SOURCE	0: set on pins; 1: set on internal EEPROM

Boot Settings Table

Boot Mode	VD0_OUT5	VD0_OUT6	VD0_OUT10	VD1_OUT0	VD0_OUT11	Remarks
NAND	NAND Flash page size 0: 512Byte 1: 2K Byte	NAND Flash read confirm 0:NAND does not use read confirm. 1:NAND needs read confirm.	1	0	x	Also set VD0_OUT0=0
USB	x	x	0	0	x	Also set VD1_OUT7=1/0
Reserved	x	x	1	1	x	
BootROM (SSI0 + loader in EEPROM)	Length of SPI EEPROM addresses 0: 2 bytes (SPI2) 1: 3 bytes (SPI3)	0	0	1	0	
Host Boot	x	1	0	1	0	Also set VD1_OUT1=1
Boot Bypass	All the above settings require VD0_OUT8=0; Set this pin to 1 to bypass normal boot.					

4 Pin Description

There are a total of 404 physical pins including power and ground balls. A single physical pin may be mapped to multiple virtual pins as indicated in the tables below. Please refer to Appendix A (sorted by physical pin number) for the overall pin list, ball location, and full functional multiplexing information for each physical pin.

4.1 DRAM Interface

Pin Name	Dir	Phys Pin Number	Pad Type	Description
DDR_DQ[15:0]	I/O	16:1	sstl18/sstl15/lvcmos18/lvcmos12	Bi-directional data bus
DDR_DQS[1:0]	I/O	20:19	sstl18/sstl15/lvcmos18/lvcmos12	Data strobe. 1 per 8 data bits. Output with write data, center aligned Input with read data, edge aligned
DDR_DQS#[1:0]	I/O	18:17	sstl18/sstl15/lvcmos18/lvcmos12	DQS[n] and DQS#[n] are differential signals
DDR_DM[1:0]	OUT	22:21	sstl18/sstl15/lvcmos18/lvcmos12	Data write mask. 1 bit per 8 data bits.
DDR_CK	OUT	23	sstl18/sstl15/lvcmos18/lvcmos12	DRAM clock
DDR_CK#	OUT	24	sstl18/sstl15/lvcmos18/lvcmos12	CK and CK# are differential clocks
DDR_A[13:0]	OUT	38:25	sstl18/sstl15/lvcmos18/lvcmos12	Address for RAS and CAS
DDR_BA[2:0]	OUT	41:39	sstl18/sstl15/lvcmos18/lvcmos12	Bank Address
DDR_RAS	OUT	42	sstl18/sstl15/lvcmos18/lvcmos12	Row Address Strobe. Active low
DDR_CAS	OUT	43	sstl18/sstl15/lvcmos18/lvcmos12	Column Address strobe. Active low
DDR_WE	OUT	44	sstl18/sstl15/lvcmos18/lvcmos12	Write Enable. Active low
DDR_CKE	OUT	45	sstl18/sstl15/lvcmos18/lvcmos12	Clock Enable
DDR_ODT	OUT	46	sstl18/sstl15/lvcmos18/lvcmos12	SDRAM on-die termination control signal
DDR_CALIBR	I/O	48	-	For ZQ calibration
DDR_RESET	OUT	47	-	For DDR3 – asynchronous RESET
DDR_CS	OUT	50		DRAM chip select
DDR_VREF	I/O	49	Analog	Reference voltage for DDR2/DDR3 (VDDQ/2)
DDR_VSSQ	Supply	402:393	Ground	
DDR_VDDQ	Supply	351:342	Power	DDR IO power

4.2 Analog Video Out

Pin Name	Dir	Phys Pin Number	Pad Type	Description
DAC_IO	I/O	128	Analog	Composite CVBS Output
DAC_RSET		126	Analog	Reference resistor
DAC_VREFIN	I/O	127	Analog	Voltage reference input.
DAC_COMP	I/O	129	Analog	Compensation pin. This pin should be connected through a 0.1uF ceramic capacitor to DAC_AHVDD externally.
DAC_AHVDD	Supply	130	Power	Analog power
DAC_AHVSS	Supply	131	Ground	Analog ground

4.3 Digital Video Output: Port0

Pin Name	Dir	Phys Pin	Pad Type	Description
VD0_OUT0	I/O	132	CMOS	VOUT data
VD0_OUT1	I/O	133	CMOS	VOUT data
VD0_OUT2	I/O	134	CMOS	VOUT data
VD0_OUT3	I/O	135	CMOS	VOUT data
VD0_OUT4	I/O	136	CMOS	VOUT data
VD0_OUT5	I/O	137	CMOS	VOUT data
VD0_OUT6	I/O	65	CMOS	VOUT data
VD0_OUT7	I/O	66	CMOS	VOUT data
VD0_OUT8	I/O	67	CMOS	VOUT data
VD0_OUT9	I/O	68	CMOS	VOUT data
VD0_OUT10	I/O	69	CMOS	VOUT data
VD0_OUT11	I/O	70	CMOS	VOUT data
VD0_OUT12	I/O	71	CMOS	VOUT data
VD0_OUT13	I/O	72	CMOS	VOUT data
VD0_OUT14	I/O	73	CMOS	VOUT data
VD0_OUT15	I/O	74	CMOS	VOUT data
VD0_CLK	OUT	138	CMOS	VideoOut Clock
VD0_VSYNC	OUT	139	CMOS	VideoOut Vsync signal
VD0_HSYNC	OUT	140	CMOS	VideoOut Hsync signal
VD0_HVLD	I/O	58	CMOS	Video Output Interface H valid (active pixels)

4.4 Digital Video Output: Port1

Pin Name	Dir	Phys Pin	Pad Type	Description

VD1_OUT[23:0]	I/O	164:141	CMOS	VOUT data
VD1_CLK	OUT	165	CMOS	VideoOut Clock
VD1_HSYNC	OUT	167	CMOS	VideoOut Hsync signal
VD1_VSYNC	OUT	166	CMOS	VideoOut Vsync signal
VD1_HVLD	OUT	168	CMOS	Line Valid signal

4.5 HDMI Out

Pin Name	Dir	Phys Pin	Pad Type	Description
HDMI_CH0_M	I/O	170	Analog	Differential TMDS data out (open drain)
HDMI_CH1_M	I/O	172	Analog	
HDMI_CH2_M	I/O	174	Analog	
HDMI_CH0_P	I/O	169	Analog	
HDMI_CH1_P	I/O	171	Analog	
HDMI_CH2_P	I/O	173	Analog	
HDMI_CLK_M	I/O	176	Analog	Differential TMDS clock (open drain)
HDMI_CLK_P	I/O	175	Analog	
HDMI_REXT	I/O	177	Analog	Reference resistor
HDMI_CEC	I/O	183	CMOS	CEC control pin
IDC2_CLK	I/O	185	CMOS	Second IDC port – clock
IDC2_DATA	I/O	186	CMOS	Second IDC port - data
HDMI_HPD	I/O	184	CMOS	Hot plug detect, 5V tolerant
HDMI_VDD	Supply	180	Power	VDD
HDMI_VDDA	Supply	179:178	Power	
HDMI_VSSA	Supply	182:181	Ground	

4.6 MIPI DSI Video Output/Input

Pin Name	Dir	Phys Pin	Pad Type	Description
MIPI1_MDATA_P	I/O	225	Analog	
MIPI1_MDATA_N	I/O	226	Analog	
MIPI1_MCLK_P	I/O	227	Analog	
MIPI1_MCLK_N	I/O	228	Analog	
MIPI1_SDATA_P	I/O	229	Analog	
MIPI1_SDATA_N	I/O	230	Analog	
MIPI1_SCLK_P	I/O	231	Analog	
MIPI1_SCLK_N	I/O	232	Analog	

M_VDD11_PLL	Supply	233	Power	VDDA_PLL
MIPI1_VREG	Analog	234		

4.7 MIPI Sensor Interface

Pin Name	Dir	Phys Pin Number	Pad Type	Description
S_DPDATA_0	I/O	214	Analog	
S_DNDATA_0	I/O	217	Analog	
S_DPDATA_1	I/O	215	Analog	
S_DNDATA_1	I/O	218	Analog	
S_DPDATA_2	I/O	216	Analog	
S_DNDATA_2	I/O	219	Analog	
S_DPCLK	I/O	220	Analog	
S_DNCLK	I/O	221	Analog	
MS_VDD11	Supply	222	Power	VDD
MS_VDD18	Supply	223	Power	1.8V
MS_VSS	Supply	224	Ground	Analog Ground

4.8 Sensor Input

Pin Name	Dir	Phys Pin	Pad Type	Description
SD_LVDS_N[7:0]	IN	202:195	CMOS	Sensor data. Differential for LVDS/subLVDS/SLVS, single ended for LVCMOS mode. 100 Ohm termination resistor is required close to the device for LVDS, subLVDS and SLVS mode. 1.8V – 3.3V LVCMOS modes are supported. Both single data rate and double data rate are supported.
SD_LVDS_P[7:0]	IN	194:187	CMOS	Sensor data. Differential for LVDS/subLVDS/SLVS, single ended for LVCMOS mode. 100 Ohm termination resistor is required close to the device for LVDS, subLVDS and SLVS mode. 1.8V – 3.3V LVCMOS modes are supported. Both single data rate and double data rate are supported.
SPCLK_LVDS_N[1:0]	IN	206:205	CMOS	Sensor pixel clock. Differential for LVDS /subLVDS/SLVS, single ended for LVCMOS mode (use only _N_*). 100 Ohm termination resistor is required

SPCLK_LVDS_P[1:0]	IN	204:203	CMOS	close to the device for LVDS, subLVDS and SLVS mode. 1.8V – 3.3V LVCMOS modes are supported. Please see note in section 3.3.1.
VDDA_LVDS	Sup	212	Power	2.5V for LVDS; 1.8 – 3.3V for LVCMOS
VSSA_LVDS	Sup	213	Ground	Ground
CLK_SI	I/O	209	CMOS	Sensor clock out. When driven from A5s66, the voltage level matches VDD33
STRIG[1:0]	I/O	211:210	CMOS	Flash Strobe Trigger (in sync with Vsync)
SVSYNC	I/O	208	CMOS	Video In VSYNC signal; Shared with Sensor Input port. When driven from A5s66, the voltage level matches VDD33
SHSYNC	I/O	207	CMOS	Video In HSYNC signal; Shared with Sensor Input port. When driven from A5s66, the voltage level matches VDD33

4.9 Digital Audio Interface (I2S and I2S Host Interface)

Pin Name	Dir	Phys Pin Number	Pad Type	Description
I2S0_WS	I/O	120	CMOS	I2S_WordSelect for all ports
I2S0_CLK	OUT	117	CMOS	I2S_Clock for all ports
I2S[2:0]_SO	OUT	124,122,118	CMOS	I2S_SerialDataOut
I2S[2:0]_SI	IN	125,123,119	CMOS	I2S_SerialDataIn
CLK_AU	I/O	121	CMOS	Audio master clock

4.10 Ethernet MII

Pin Name	Dir	Phys Pin Number	Pad Type	Description
GMII_MDC_O	O	132	CMOS	MII clock
GMII_MDO_O	O	133	CMOS	MII data bus
PHY_TXEN_O	O	134	CMOS	Transmit ready
PHY_TXER_O	O	135	CMOS	Transmit error
PHY_TXD_O[3:0]	O	66,65,137,136	CMOS	Transmit data
CLK_TX_I	I	140	CMOS	Transmit clock
CLK_RX_I	I	139	CMOS	Receive clock
PHY_RXDV_I	I	81	CMOS	Receive data valid
PHY_RXER_I	I	82	CMOS	Receive error
PHY_CRS_I	I	83	CMOS	Carrier sense
PHY_COL_I	I	84	CMOS	Collision detect
PHY_RXD_I[3:0]	I	90,89,88,85	CMOS	Receive data

4.11 USB

Pin Name	Dir	Phys Pin Num	Pad Type	Description
DETECT_VBUS	IN	105	Analog	5.0V I/O tolerance
USB_DM	I/O	106	Analog	DP/DM are differential signals
USB_DP	I/O	107	Analog	DP/DM are differential signals
USB_REXT	I/O	108	Analog	43.2 ohm pull low
XIN_USB	I/O	109	Analog	Crystal input.
XOUT_USB	I/O	110	Analog	Crystal output.
USB_HVDD	Supply	111	Power	3.3V
USB_HVSS	Supply	112,113	Ground	Ground
USB_DVDD	Supply	114	Power	
USB_VDD25	Supply	116	Power	
USB_DVSS	Supply	115	Ground	Ground

4.12 SMIO

Pin Name	Dir	Phys Pin Num	Pad Type	NAND	SD (MMC)	CF (PCMem)	CFA (IDE)	HIF	MS
SMIO0	I/O	260	CMOS	CE				D0	
SMIO1	I/O	261	CMOS	R /-B				D1	

SMIO2	NC	262	-	-	-	-	-	-	-
SMIO3	I/O	263	CMOS		CLK				CLK
SMIO4	I/O	264	CMOS		CMD				BS
SMIO5	I/O	265	CMOS		CD				
SMIO6	I/O	266	CMOS		WP				
SMIO7	I/O	267	CMOS			CD1	CD1	D7	
SMIO8	I/O	268	CMOS			WAIT	IORDY	D8	
SMIO9	I/O	269	CMOS			INPACK	DMARQ	D9	
SMIO10	I/O	270	CMOS			WP	IOCS16	D10	
SMIO11	I/O	271	CMOS			OE	ATASEL	D11	
SMIO12	I/O	272	CMOS			RESET	RESET	D12	
SMIO13	I/O	273	CMOS			CE1	CS1	D13	
SMIO14	I/O	274	CMOS			CE2	CS2	D14	
SMIO15	I/O	275	CMOS	RE		IOWR	IOWR	D15	
SMIO16	I/O	276	CMOS			IORD	IORD	RDY	
SMIO17	I/O	277	CMOS			REG	DMACK	A0	
SMIO18	I/O	278	CMOS			WE	WE	A1	
SMIO19	I/O	279	CMOS	WE		D0	D0	A2	
SMIO20	I/O	280	CMOS	ALE		D1	D1	OE	
SMIO21	I/O	281	CMOS	D0		D2	D2	WE	
SMIO22	I/O	282	CMOS	D1		D3	D3	CS	
SMIO23	I/O	283	CMOS	D2		D4	D4	D2	
SMIO24	I/O	284	CMOS	D3		D5	D5	D3	
SMIO25	I/O	285	CMOS	D4		D6	D6	D4	
SMIO26	I/O	286	CMOS	D5		D7	D7	D5	
SMIO27	I/O	287	CMOS	D6		D8	D8	D6	
SMIO28	I/O	288	CMOS	D7		D9	D9		
SMIO29	I/O	289	CMOS	CLE		D10	D10		
SMIO30	I/O	290	CMOS		D0	D11	D11		D0
SMIO31	I/O	291	CMOS		D1	D12	D12		D1
SMIO32	I/O	292	CMOS		D2	D13	D13		D2
SMIO33	I/O	293	CMOS		D3	D14	D14		D3
SMIO34	I/O	294	CMOS		D4	D15	D15		D4
SMIO35	I/O	295	CMOS		D5	A0	A0		D5
SMIO36	I/O	296	CMOS		D6	A1	A1		D6
SMIO37	I/O	297	CMOS		D7	A2	A2		D7

SMIO38	I/O	298	CMOS		SDIO_CLK	A3			
SMIO39	I/O	299	CMOS		SDIO_CMD	A4			
SMIO40	I/O	300	CMOS		SDIO_D0	A5			
SMIO41	I/O	301	CMOS		SDIO_D1	A6			
SMIO42	I/O	302	CMOS		SDIO_D2	A7			
SMIO43	I/O	303	CMOS		SDIO_D3	A8			
SMIO44	I/O	304	CMOS		SDIO_CD	A9			
SMIO45	I/O	305	CMOS		SDIO_WP	A10			
CF_CD2	I/O	75	CMOS			CD2	CD2		
STSCHG	I/O	77	CMOS			CF status change flag	CF status change flag		
CF_PULL_CTL	I/O	78	CMOS			CF PCcard mode and ide mode pullup /down control	CF PCcard mode and ide mode pullup /down control		
PWRCYC	I/O	79	CMOS			CF card power cycling control			
NAND_WP	I/O	80	CMOS	WP					
A11	I/O	132	CMOS						
A12	I/O	133	CMOS						
A13	I/O	134	CMOS						
A14	I/O	135	CMOS						
A15	I/O	136	CMOS						
A16	I/O	137	CMOS						
A17	I/O	65	CMOS						
A18	I/O	66	CMOS						
A19	I/O	67	CMOS						
A20	I/O	68	CMOS						
A21	I/O	69	CMOS						
A22	I/O	70	CMOS						
NAND_CE1	I/O	88	CMOS	CE1					
NAND_CE2	I/O	93	CMOS	CE2					
NAND_CE3	I/O	94	CMOS	CE3					

4.13 Stepper Controller

Pin Name	Dir	Phys Pin Num	Pad Type	Description

SC_A[4:0]	I/O	85:81	CMOS	Stepper ControllerA
SC_B[4:0]	I/O	90:86	CMOS	Stepper ControllerB
SC_C[4:0]	I/O	95:91	CMOS	Stepper ControllerC

4.14 JTAG

Pin Name	Dir	Phys Pin Num	Pad Type	Description
JTAG_CLK	IN	100	CMOS	Clock, pull high to vdd33
JTAG_RST_L	IN	101	CMOS	Reset
JTAG_TEST_MODE	IN	104	CMOS	Test mode select
JTAG_TDI	IN	102	CMOS	Data in
JTAG_TDO	OUT	103	CMOS	Data out

4.15 Other Serial Interface Pins (SSI/SPI, IDC and UART)

Pin Name	Dir	Phys Pin	Pad Type	Description
SSI0_CLK	I/O	53	CMOS	SSI0 bit clock (27MHz, programmable)
SSI0_MOSI	I/O	54	CMOS	SSI0 serial data out
SSI0_MISO	I/O	55	CMOS	SSI0 serial data in
SSI0_EN0	I/O	56	CMOS	SSI0 device select 0
SSI0_EN1	I/O	57	CMOS	SSI0 device select 1
SSI2_CLK	I/O	96	CMOS	SSI2 bit clock (54MHz, programmable)
SSI2_MISO	IN	97	CMOS	SSI2serial data in;
SSI2_MOSI	OUT	98	CMOS	SSI2 serial data out;
SSI2_OEN	I/O	99	CMOS	SSI2 device select;
SSIs_CLK	I/O	94	CMOS	SSI slave only port clock
SSIs_MISO	I/O	91	CMOS	SSI slave data out
SSIs_MOSI	I/O	93	CMOS	SSI slave data in
SSIs_EN	I/O	92	CMOS	SSI slave only port enable
IDC_CLK	I/O	51	CMOS	IDC is for communicating with I2C devices
IDC_DATA	I/O	52	CMOS	IDC data
IDC3_CLK	I/O	78	CMOS	IDC3 is for communicating with I2C devices
IDC3_DATA	I/O	77	CMOS	IDC3 data

UART0_TX	OUT	62	CMOS	UART transmit (up to 115.2kbps)
UART0_RX	IN	63	CMOS	UART receive
UART1_TX	OUT	91		Transmit
UART1_RX	IN	93		Receive
UART1_RTS	OUT	92		Hw flow control signal
UART1_CTS	IN	94		Hw flow control signal
IR_IN	IN	76	CMOS	InfraRed interface

4.16 ADC

Pin Name	Dir	Phys Pin	Pad Type	Description
ADC_CH[3:0]	IN	235:238	Analog	Housekeeping ADC analog input (4 channels)
ADC_AVDD	Supply	239	Power	3.3V
ADC_AVSS	Supply	240	Ground	Analog ground

4.17 Other Miscellaneous Function Pins

Pin Name	Dir	Phys Pin	Pad Type	Description
TIMER0	I/O	59	CMOS	Interval Timer0 external clock source
TIMER1	I/O	60	CMOS	Interval Timer1 external clock source
TIMER2	I/O	61	CMOS	Interval Timer2 external clock source
VD_PWM0	I/O	64	CMOS	Pulse Width Modulator output 0
PWM1	I/O	86	CMOS	Pulse Width Modulator output 1
PWM2	I/O	87	CMOS	Pulse Width Modulator output 2
PWM3	I/O	91	CMOS	Pulse Width Modulator output 3
PWM4	I/O	92	CMOS	Pulse Width Modulator output 4

4.18 GPIO

Pin Name	Dir	Phys Pin	Pad Type	Primary Function Description
GPIO0	I/O	51	CMOS	
GPIO1	I/O	52	CMOS	
GPIO2	I/O	53	CMOS	
GPIO3	I/O	54	CMOS	
GPIO4	I/O	55	CMOS	
GPIO5	I/O	56	CMOS	

GPIO6	I/O	57	CMOS	
GPIO7	I/O	58	CMOS	
GPIO11	I/O	59	CMOS	
GPIO12	I/O	60	CMOS	
GPIO13	I/O	61	CMOS	
GPIO14	I/O	62	CMOS	
GPIO15	I/O	63	CMOS	
GPIO16	IN	64	CMOS	
GPIO18	I/O	65	CMOS	
GPIO19	I/O	66	CMOS	
GPIO20	I/O	67	CMOS	
GPIO21	I/O	68	CMOS	
GPIO22	I/O	69	CMOS	
GPIO23	I/O	70	CMOS	
GPIO24	I/O	71	CMOS	
GPIO25	I/O	72	CMOS	
GPIO26	I/O	73	CMOS	
GPIO27	I/O	74	CMOS	
GPIO28	I/O	161	CMOS	
GPIO29	I/O	162	CMOS	
GPIO30	I/O	163	CMOS	
GPIO31	I/O	164	CMOS	
GPIO32	I/O	75	CMOS	
GPIO35	I/O	76	CMOS	
GPIO36	I/O	77	CMOS	
GPIO37	I/O	78	CMOS	Output is inverted from programmed value;
GPIO38	I/O	79	CMOS	
GPIO39	I/O	80	CMOS	
GPIO40	I/O	81	CMOS	
GPIO41	I/O	82	CMOS	
GPIO42	I/O	83	CMOS	
GPIO43	I/O	84	CMOS	
GPIO44	I/O	85	CMOS	
GPIO45	I/O	86	CMOS	
GPIO46	I/O	87	CMOS	
GPIO47	I/O	88	CMOS	

GPIO48	I/O	89	CMOS	
GPIO49	I/O	90	CMOS	
GPIO50	I/O	91	CMOS	
GPIO51	I/O	92	CMOS	
GPIO52	I/O	93	CMOS	
GPIO53	I/O	94	CMOS	
GPIO54	I/O	95	CMOS	
GPIO55	I/O	132	CMOS	
GPIO56	I/O	133	CMOS	
GPIO57	I/O	134	CMOS	
GPIO58	I/O	135	CMOS	
GPIO59	I/O	136	CMOS	
GPIO60	I/O	137	CMOS	
GPIO61	I/O	139	CMOS	
GPIO62	I/O	140	CMOS	
GPIO65	I/O	263	CMOS	
GPIO66	I/O	264	CMOS	
GPIO67	I/O	265	CMOS	
GPIO68	I/O	266	CMOS	
GPIO69	I/O	298	CMOS	
GPIO70	I/O	299	CMOS	
GPIO71	I/O	300	CMOS	
GPIO72	I/O	301	CMOS	
GPIO73	I/O	302	CMOS	
GPIO74	I/O	303	CMOS	
GPIO75	I/O	304	CMOS	
GPIO76	I/O	305	CMOS	
GPIO77	I/O	120	CMOS	
GPIO78	I/O	117	CMOS	
GPIO79	I/O	118	CMOS	
GPIO80	I/O	119	CMOS	
GPIO81	I/O	121	CMOS	
GPIO82	I/O	122	CMOS	
GPIO83	I/O	123	CMOS	
GPIO84	I/O	124	CMOS	
GPIO85	I/O	125	CMOS	

GPIO86	I/O	185	CMOS	
GPIO87	I/O	186	CMOS	
GPIO88	I/O	96	CMOS	
GPIO89	I/O	98	CMOS	
GPIO90	I/O	97	CMOS	
GPIO91	I/O	99	CMOS	
GPIO92	I/O	157	CMOS	
GPIO93	I/O	158	CMOS	
GPIO94	I/O	159	CMOS	
GPIO95	I/O	160	CMOS	

4.19 RTC and Power Management

Pin Name	Dir	Phys Pin	Pad Type	Description
XI_RTC	IN	246	Xosc pad	RTC clock (32kHz oscillator for RTC)
XO_RTC	OUT	247	Xosc pad	RTC clock output
PWC_RTC_CP	Supply	248	Power	Power for RTC module and on-chip RTC oscillator (3.3V nominal). When less than minimum value (1.2V), the power controller will be shut down and all the registers will reset.
PWC_PC_VDD	Supply	249	Power	Power for power management module Connected to external battery/adaptor clamping circuit. The maximum voltage is 3.6V. Standby current is TBC.
PWC_PC_REF		250	IN	Used to detect whether battery level is too low. Connect to voltage divided version of PWC_PC_VDD. The division ratio should be ≥ 75%.
PWC_WKUP[3:0]	IN	254:251	CMOS	In power-off state, a positive pulse of PWC_WKUP will trigger the power-on sequences. Connect to external power switch to go to power-on state when PWC_PC_VDD is above 2.4V (if PWC_RTC_CP charged by PWC_PC_VDD) or above 1.8V (if charged by dedicated battery) and PWC_RTC_CP is above 1.8V. The power-on sequence consists of PSEQ1 state followed by the PSEQ2 state followed by the PSEQ3 state followed by the power-on state. The core is held in reset until the power-on state is reached. The power-off sequences can be triggered by 1. By software or 2. By removing PWC_PC_VDD.
PWC_RSTINB	IN	255	CMOS	PWC reset, pull high to PWC_RTC_CP
PWC_PSEQ1	OUT	256	CMOS	1st power up/down control signal
PWC_PSEQ2	OUT	257	CMOS	2nd power up/down control signal

PWC_PSEQ3	OUT	258	CMOS	3rd power up/down control signal
PWC_RSTOB	OUT	259	CMOS	Reset signal out (can also be used as power up/down control signal)

4.20 Global and Test

Pin Name	Dir	Phys Pin Num	Pad Type	Description
XIN	IN	241	Xosc pad	System clock (24MHz crystal oscillator)
XOUT	OUT	242	Xosc pad	System clock output
TEST_MODE	IN	243	CMOS	0: Normal Mode 1: Test Mode
POR_L	IN	244	CMOS	Global system reset pin (active low)
PLL_VFLTR	I/O	245	Analog	
VDD	Supply	337:318	Power	Core power
VDD_BYP	Supply	341:339	Power	Core power for bypass mode
VDD33	Supply	309:306	Power	I/O power
VDD33_BYP	Supply	313:310	Power	IO power for bypass mode
VDDA_PLL	Supply	315:314	Power	PLL power
VDDA18_PLL	Supply	317:316	Power	PLL power
VSS	Supply	338, 384:352	Ground	Ground
VSS33	Supply	392:385	Ground	Ground
VSSA_PLL	Supply	404:403	Ground	PLL ground

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Parameter	Min	Max
Analog supply voltage (3.3V)	-0.3	3.6
Digital supply voltage (3.3V)	-0.3	3.6
Analog supply voltage (1.3V)	-0.3	1.35
Digital supply voltage (1.2V)	-0.3	1.32
Digital in range	-0.3	3.6
Analog in range	-0.3	3.6
Operating temperature (case) (^{o}C)	-20	85

5.2 Recommended Operating Conditions

5.2.1 Power Rails DC Characteristics

Parameters		Min	Typical	Max
VDD		1.15	1.2	1.25
VDD33		2.8	3.3	3.5
VDDA_PLL		1.25	1.3	1.35
VDDA18_PLL		1.7	1.8	1.9
DDR_VDDQ	DDR2 Mode	1.7	1.8	1.9
	DDR3 Mode	1.43	1.5	1.57
VDDA_LVDS	LVDS Mode	tbd	2.5	tbd
	1.8V LVCMOS	tbd	1.8	tbd
	2.5V LVCMOS	tbd	2.5	tbd
	2.8V LVCMOS	tbd	2.8	tbd
	3.3V LVCMOS	Tbd	3.3	tbd
USB_HVDD		3.0	3.3	3.46
USB_VDD25		2.375	2.5	2.625
USB_DVDD		1.15	1.2	1.25
ADC_AVDD		3.0	3.3	3.46
DAC_AHVDD		3.0	3.3	3.46
HDMI_VDDA		2.375	2.5	2.625
HDMI_VDD		1.25	1.3	1.35
M_VDD11_PLL		VDDA_PLL		
MS_VDD18		1.7	1.8	1.9

5.2.2 Digital I/O Characteristics

Parameter		Min	Typ	Max
VIL	In low voltage	-0.3V		0.7V
VIH	In high voltage	2.0V		3.6V
VOL	Out low voltage			0.4V
VOH	Out high voltage	2.4V		

5.2.3 DRAM I/O

DC Voltage Levels

Parameter		Min	Typ	Max
VTT	Termination voltage	DDR_VREF-40mV	DDR_VREF	DDR_VREF+40mV
DDR_VREF	In reference level	0.49 * DDR_VDDQ	0.5 * DDR_VDDQ	0.51 * DDR_VDDQ

SSTL18 I/O DC Specifications

Parameter		Min	Typ	Max
VIHT	DC in logic threshold high			DDR_VREF + 50mV
VILT	DC in logic threshold low	DDR_VREF-50mV		
VIH	DC in voltage high			DDR_VDDQ +0.3V
VIL	DC in voltage low	-0.3V		
VOH	DC out logic high	DDR_VDDQ		
VOL	DC out logic low			0
RTT1	RTT effective impedance value	60 Ohms	75 Ohms	90 Ohms
RTT2	RTT effective impedance value	120 Ohms	150 Ohms	180 Ohms

5.2.4 RTC & Power Management Module Power Supply

Parameter		Min	Typ	Max
PWC_RTC_CP	RTC module supply	1.2V	3.3V	3.6V
PWC_PC_VDD	Power management supply	2.4V	3.3V	3.6V
PWC_PC_REF	Reference voltage	1.8V	75% of PWC_PC_VDD	3.6V
VIH	For PWC_WKUP	0.7 * PWC_RTC_CP		

VIL	For PWC_WKUP			0.3*PWC_RTC_CP		
VOH	For PWC_PSEQ1/2/3 and PWC_RSTOB	PWC_RTC_CP*0.8				

5.2.5 MIPI PHY

MIPI Transmitter DC Specification

Parameter	Symbol	Min	Typical	Max	Unit	Condition
HS transmit static commonmode voltage	VCMTX	150	200	250	mV	
VCMTX mismatch when output is Differential-1 or Differential-0	|ΔVCMTX(1,0)|			5	mV	
HS transmit differential voltage	|VOD|	140	200	270	mV	
VOD mismatch when output is Differential-1 or Differential-0	|ΔVOD|			10	mV	
HS output high voltage	VOHHS			360	mV	
Single ended output impedance	ZOS	40	50	62.5	Ω	
Single ended output impedance mismatch	ΔZOS			10	%	

MIPI Transmitter AC Specification

Parameter	Symbol	Min	Typical	Max	Unit	Condition
Common-level variations above 450MHz				15	mV_{RMS}	>450MHz
				25	mV_{RMS}	50 - 450 MHz
20%-80% rise time and fall time		150			ps	

MIPI Receiver DC Specification

Parameter	Symbol	Min	Typical	Max	Unit	Condition
Logic 1 input voltage	VIH	880			mV	
Logic 0 input voltage, not in ULP State	VIL			550	mV	
Logic 0 input voltage, ULP State	VIL-ULP			300	mV	
Input hysteresis	VHYST	25			mV	

MIPI Receiver AC Specification

Parameter	Symbol	Min	Typical	Max	Unit	Condition
Input pulse rejection				300	V-ps	
Minimum pulse width response		20			ns	
Peak interference amplitude				200	mV	
Interference frequency		450			MHz	

MIPI DP/DN Pin Characteristic

Parameter	Symbol	Min	Typical	Max	Unit	Condition
Pin signal voltage range	V_{PIN}	-50		1350	mV	
Pin leakage current	I_{LEAK}	-10		10	uA	
Ground shift		-50		50	mV	
Transient pin voltage level	$V_{PIN(absmax)}$	-0.15		1.45	V	
Maximum transient time above VPIN(max) or below VPIN(min)		20			ns	

5.2.6 Parallel LVCMOS I/O

Parameter		Min	Typ	Max
VIL	VDDA_LVDS=1.8V			0.6V
	VDDA_LVDS=3.3V			0.7V
VIH	VDDA_LVDS=1.8V	1.62V		
	VDDA_LVDS=3.3V	2.4V		

5.2.7 Video DAC Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Condition*
Operating digital supply voltage	VDD	tbd	1.2	tbd	V	--
Operating analog supply voltage	DAC_AHVDD	3.0	3.3	3.46	V	--
IO out current	IO_{FS}		34.6		mA	
Operating Current	I_{OP}		36		mA	
Out voltage range	V(IO)	1.17	1.28	1.43	V	
DAC resolution	--	--	--	10	bits	

Differential non-linearity error	DNL	--	--	±1	LSB	
Integral non-linearity error	INL	--	--	±2	LSB	
Reference Voltage	VREF			1.22	V	

*T_A=25°C, R_{SET}=1.2kΩ, R_{LOAD}=37.5Ω; Full Scale Output Voltage = 1.3V; unless otherwise specified

5.2.8 ADC Electrical Specifications

DC Spec

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating digital supply voltage	VDD	tbd	1.2	tbd	V	--
Operating analog supply voltage	ADC_AVDD	3.0	3.3	3.46	V	--
Operating current	Ivdda		2		mA	Fclk=12MHz; Fs=1MS/s
	ADC_AVSS		0		V	Analog Ground
Reference Voltage	VREF		ADC_AVSS		V	0.0V
Analog input voltage	VIN	ADC_AVSS		ADC_AVDD		
Resolution	N		10		Bits	
INL	INL		±1	±2	LSB	
DNL	DNL		±0.5	±1	LSB	
In impedance	CIN				pF	

AC Spec

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Effective resolution	ENOB	8			bits	
Sampling rate	Fs			1000	KS/s	
Sampling clock	Fclk			12	MHz	
Signal-to-noise & distortion ratio	SNDR	48	54		dB	Fclk=12MHz; AIN= 50KHZ*

*AIN= Analog input max frequency

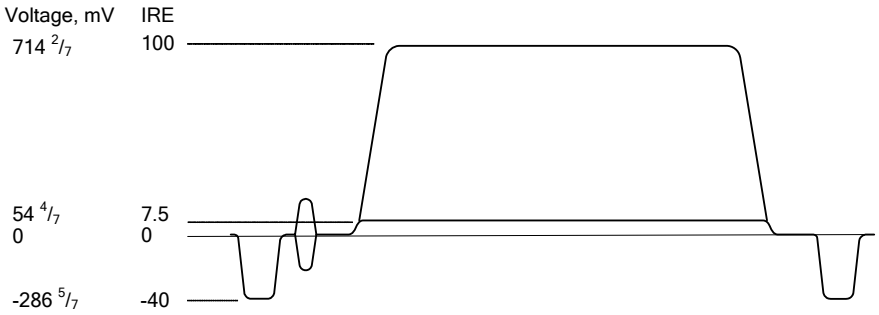
5.2.9 Jitter Specifications

Parameter	Min	Typ	Max
Crystal frequency		24MHz	
Crystal accuracy			+-30PPM
Cycle to cycle jitter			+-200ps
Long term jitter			+-500ps

5.3 Video Signal Waveforms and Timing

This section contains the analog video output waveforms as required by the standard. System designers need to make sure the analog video output from the system board meets the desired/standard specifications.

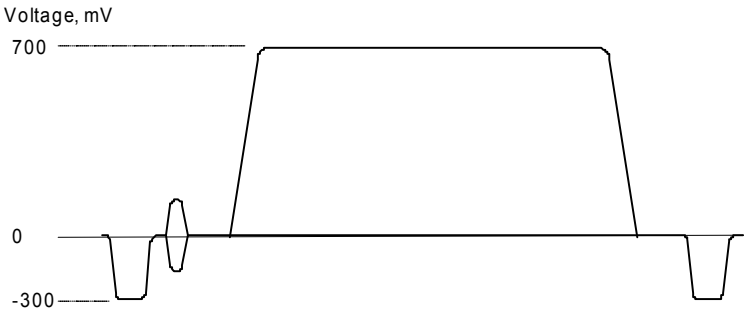
5.3.1 SD - NTSC (480i/525i)



Including a maximum chroma excursion to about 131 IRE, the maximum excursion of the composite NTSC signal is about 1.221Vpp

Figure 3. NTSC Waveform

5.3.2 SD - PAL (576i/625i)



The maximum excursion of the composite PAL signal is about 1.2335Vpp

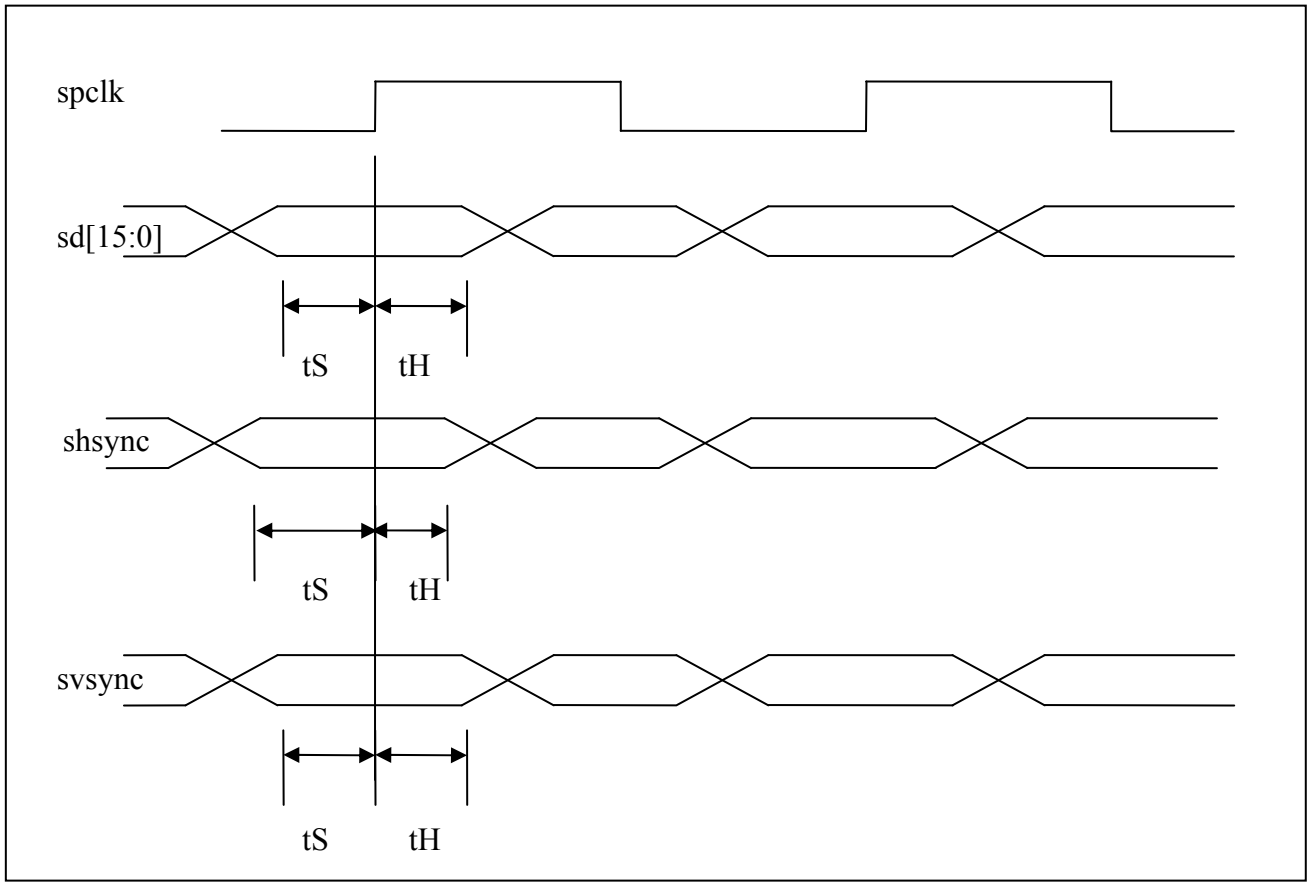
Figure 4. PAL Waveform

5.3.3 Waveform Summary Table

Format	Standard/Display Resolution	Signal Element	Max. Video Amplitude (Vpp/V)

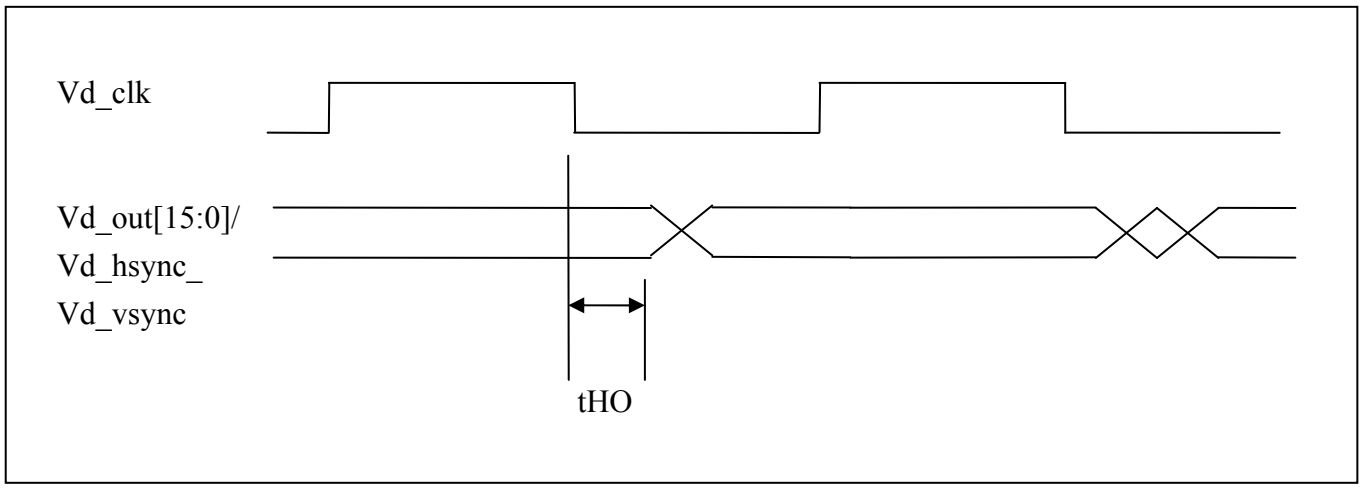
NTSC	CVBS	CVBS	1.221
PAL	CVBS	CVBS	1.2335

5.3.4 Video Input Timing



Setup/Hold wrt spclk	Setup (tS)	Hold (tH)	Comment
Sd[15:0]	2ns	2ns	Assume rising edge of spclk is used to latch data
Shsync	2ns	2ns	
Svsync	2ns	2ns	
Sfield	2ns	2ns	

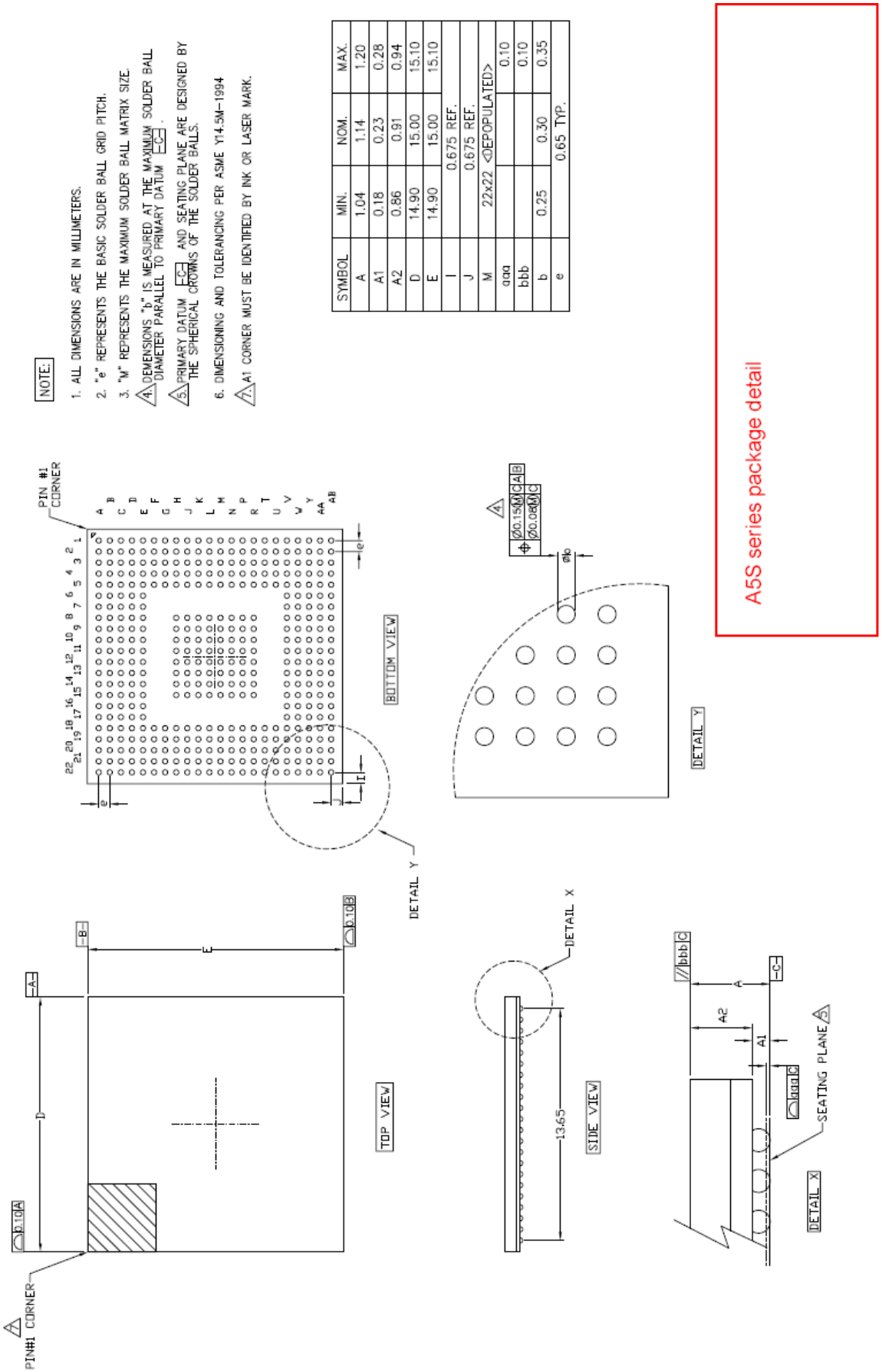
5.3.5 Video Out Timing



Output hold timing (tHO)	min	max	Comment
vd_out[15:0]	1ns	4ns	Assume data is latched out at the falling edge of vd_clk
vd_hsync	1ns	4ns	
vd_vsync	1ns	4ns	

6 Package

Type: 404 pin TFBGA (15x15mm, 0.65mm ball pitch)


A5S series package detail
NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE.
4. DEMENSIONS "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM -C- .
5. PRIMARY DATUM -C- AND SEATING PLANE ARE DESIGNED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
7. A1 CORNER MUST BE IDENTIFIED BY INK OR LASER MARK.
SYMBOL | MIN. | NOM. | MAX.
A | 1.04 | 1.14 | 1.20
A1 | 0.18 | 0.23 | 0.28
A2 | 0.86 | 0.91 | 0.94
D | 14.90 | 15.00 | 15.10
E | 14.90 | 15.00 | 15.10
I | 0.675 REF.
J | 0.675 REF.
M | 22x22 <DEPOPULATED>
ggg | 0.10
bbb | 0.10
b | 0.25 | 0.30 | 0.35
e | 0.65 TYP.
PIN #1 CORNER
BOTTOM VIEW
DETAIL Y
TOP VIEW
SIDE VIEW
DETAIL X
SEATING PLANE

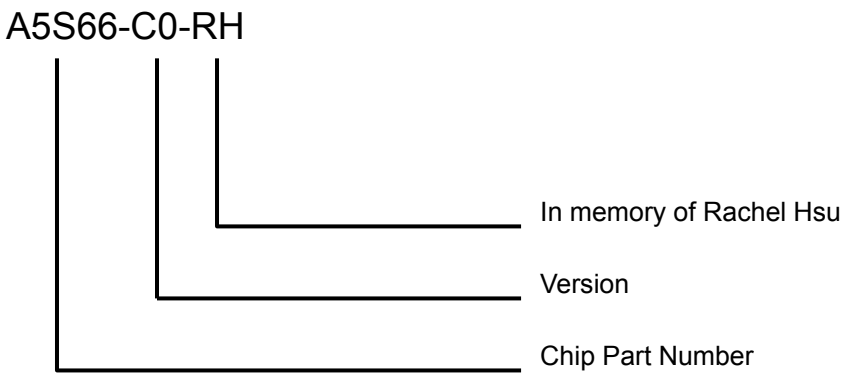
6.1 SM Opening

The detailed substrate SM openning information is available from Ambarella, please contact your local technical sales representative.

6.2 Reflow Profile

TBC. Please contact Ambarella.

7 Ordering Information



*All chips in the A5s series are Lead-Free and RoHS compliant

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Appendix A: Pin List and Mapping Table

Phys. Pin No.	Group	Ballmap	Pin name	(Multi-functions)
1	DDR	A12	DDR_DQ0	
2		C12	DDR_DQ1	
3		B12	DDR_DQ2	
4		B11	DDR_DQ3	
5		C11	DDR_DQ4	
6		A11	DDR_DQ5	
7		C10	DDR_DQ6	
8		C9	DDR_DQ7	
9		B7	DDR_DQ8	
10		C7	DDR_DQ9	
11		C8	DDR_DQ10	
12		A6	DDR_DQ11	
13		B6	DDR_DQ12	
14		A7	DDR_DQ13	
15		B5	DDR_DQ14	
16		A5	DDR_DQ15	
17		A10	DDR_DQS#0	
18		A8	DDR_DQS#1	
19		B10	DDR_DQS0	
20		B8	DDR_DQS1	
21		A9	DDR_DM0	
22		B9	DDR_DM1	
23		B18	DDR_CK	
24		A18	DDR_CK#	
25		B17	DDR_A0	
26		C16	DDR_A1	
27		A17	DDR_A2	
28		C17	DDR_A3	
29		C19	DDR_A4	
30		A20	DDR_A5	
31		B19	DDR_A6	
32		A21	DDR_A7	

33	DDR	A22	DDR_A8				
34		B20	DDR_A9				
35		B16	DDR_A10				
36		C20	DDR_A11				
37		B21	DDR_A12				
38		C21	DDR_A13				
39		A15	DDR_BA0				
40		B15	DDR_BA1				
41		C15	DDR_BA2				
42		B13	DDR_RAS				
43		A16	DDR_CAS				
44		A13	DDR_WE				
45		A19	DDR_CKE				
46		B14	DDR_ODT				
47		A14	DDR_RESET				
48		C6	DDR_CALIBR				
49		C14	VREF_DDR	0.5 * VDD18			
50		C18	DDR_CS				
51	GPIO	AA1	GPIO_0	IDC_CLK			
52		Y1	GPIO_1	IDC_DATA			
53		H19	GPIO_2	SSI0_CLK			
54		H18	GPIO_3	SSI0_MOSI			
55		G22	GPIO_4	SSI0_MISO			
56		G21	GPIO_5	SSI0_EN0			
57		G20	GPIO_6	SSI0_EN1			
58		Y18	GPIO_7	VD0_HVLD			
59		Y2	GPIO_11	TIMER_0			
60		AA3	GPIO_12	TIMER_1			
61		AA2	GPIO_13	TIMER_2			
62		F20	GPIO_14	UART0_TX			
63		F19	GPIO_15	UART0_RX			
64		W18	GPIO_16	VD_PWM0			
65		V16	GPIO_18	VD0_OUT_6		PWR_ON_CFG6	PHY_TXD_0[2]
66	GPIO	W16	GPIO_19	VD0_OUT_7		PWR_ON_CFG7	PHY_TXD_0[3]
67		Y16	GPIO_20	VD0_OUT_8		PWR_ON_CFG8	
68		AA16	GPIO_21	VD0_OUT_9		PWR_ON_CFG9	

69		AB16	GPIO_22	VD0_OUT_10		PWR_ON_CFG10	
70		V17	GPIO_23	VD0_OUT_11		PWR_ON_CFG11	
71		W17	GPIO_24	VD0_OUT_12		PWR_ON_CFG12	
72		Y17	GPIO_25	VD0_OUT_13		PWR_ON_CFG13	
73		AA17	GPIO_26	VD0_OUT_14		PWR_ON_CFG14	
74		AB17	GPIO_27	VD0_OUT_15		PWR_ON_CFG15	
75		H20	GPIO_32	CF_CD2 (CF chip detect, Initialized to READ only)			
76		AB1	GPIO_35	IR_IN			
77		M19	GPIO_36	IDC3_DATA	STSCHG		
78		H21	GPIO_37	IDC3_CLK	CF_PULL_CTL	CF pccard mode and ide mode pullup/down control	
79		M20	GPIO_38	PWRCYC (CF card power cycling control)			
80		M22	GPIO_39	NAND_WP (WP for NAND)			
81		L22	GPIO_40	SC_A0		PHY_RXDV_I	
82		L21	GPIO_41	SC_A1		PHY_RXER_I	
83		L19	GPIO_42	SC_A2		PHY_CRS_I	
84		L18	GPIO_43	SC_A3		PHY_COL_I	
85		L20	GPIO_44	SC_A4		PHY_RXD_I[0]	
86		K22	GPIO_45	SC_B0	PWM1		
87		K21	GPIO_46	SC_B1	PWM2		
88		K20	GPIO_47	SC_B2	NAND_CE1	PHY_RXD_I[1]	
89		K19	GPIO_48	SC_B3		PHY_RXD_I[2]	
90		J21	GPIO_49	SC_B4		PHY_RXD_I[3]	
91		J20	GPIO_50	SC_C0	PWM3	UART1_TX	SSIs_MISO
92		J19	GPIO_51	SC_C1	PWM4	UART1_RTS	SSIs_EN
93		J18	GPIO_52	SC_C2	NAND_CE2	UART1_RX	SSIs_MOSI
94		K18	GPIO_53	SC_C3	NAND_CE3	UART1_CTS	SSIs_CLK
95		J22	GPIO_54	SC_C4			
96		G19	GPIO_88	SSI2_CLK			
97		F22	GPIO_90	SSI2_MISO			
98		G18	GPIO_89	SSI2_MOSI			
99		F21	GPIO_91	SSI2_OEN			
100	**JTAG**	V4	JTAG_CLK				
101		U1	JTAG_RST_L				
102		W1	JTAG_TDI				
103		W2	JTAG_TDO				

104		V3	JTAG_TEST_MODE				
105	USB	AB2	DETECT_VBUS	3.3V			
106		AB4	USB_DM				
107		AB3	USB_DP				
108		AB5	USB_REXT				
109		AA4	XIN_USB				
110		AA5	XOUT_USB				
111		W4	USB_HVDD				
112		Y5	USB_HVSS				
113		R10	USB_HVSS				
114		Y4	USB_DVDD				
115		W3	USB_DVSS				
116		V5	USB_VDD25				
117	AUDIO	Y6	I2S0_CLK	GPIO_78			
118		W5	I2S0_SO	GPIO_79			
119		V7	I2S0_SI	GPIO_80			
120		W7	I2S0_WS	GPIO_77			
121		H22	CLK_AU	GPIO_81			
122		AA6	I2S1_SO	GPIO_82			
123		AB6	I2S1_SI	GPIO_83			
124		W6	I2S2_SO	GPIO_84			
125		Y7	I2S2_SI	GPIO_85			
126	Video DAC	E21	DAC_RSET	3.3V			
127		E20	DAC_VREFIN				
128		D22	DAC_IO				
129		E22	DAC_COMP				
130		B22	DAC_AHVDD				
131		C22	DAC_AHVSS				
132	Video Out0	AB14	VD0_OUT_0		PWR_ON_CFG0	GMII_MDC_O	GPIO55
133		V15	VD0_OUT_1		PWR_ON_CFG1	GMII_MDO_O	GPIO56
134		W15	VD0_OUT_2		PWR_ON_CFG2	PHY_TXEN_O	GPIO57
135		Y15	VD0_OUT_3		PWR_ON_CFG3	PHY_TXER_O	GPIO58
136		AA15	VD0_OUT_4		PWR_ON_CFG4	PHY_TXD_O[0]	GPIO59
137		AB15	VD0_OUT_5		PWR_ON_CFG5	PHY_TXD_O[1]	GPIO60
138		AA14	VD0_CLK				

139		Y14	VD0_VSYNC			CLK_RX_I	GPIO61
140		W14	VD0_HSYNC			CLK_TX_I	GPIO62
141		AA19	VD1_OUT0		PWR_ON_CFG16		
142		AB19	VD1_OUT1		PWR_ON_CFG17		
143		Y20	VD1_OUT2		PWR_ON_CFG18		
144		AA20	VD1_OUT3		PWR_ON_CFG19		
145		AB20	VD1_OUT4		PWR_ON_CFG20		
146		AA21	VD1_OUT5		PWR_ON_CFG21		
147		AB21	VD1_OUT6		PWR_ON_CFG22		
148		AB22	VD1_OUT7		PWR_ON_CFG23		
149		AA22	VD1_OUT8		PWR_ON_CFG24		
150		Y21	VD1_OUT9		PWR_ON_CFG25		
151		Y22	VD1_OUT10		PWR_ON_CFG26		
152		W20	VD1_OUT11		PWR_ON_CFG27		
153		W21	VD1_OUT12		PWR_ON_CFG28		
154	**Video**	W22	VD1_OUT13		PWR_ON_CFG29		
155	**Out1**	V18	VD1_OUT14		PWR_ON_CFG30		
156		V19	VD1_OUT15		PWR_ON_CFG31		
157		V20	VD1_OUT16	GPIO92			
158		V21	VD1_OUT17	GPIO93			
159		V22	VD1_OUT18	GPIO94			
160		U18	VD1_OUT19	GPIO95			
161		U19	VD1_OUT20	GPIO28			
162		U20	VD1_OUT21	GPIO29			
163		U21	VD1_OUT22	GPIO30			
164		U22	VD1_OUT23	GPIO31			
165		Y19	VD1_CLK				
166		AB18	VD1_VSYNC				
167		AA18	VD1_HSYNC				
168		T18	VD1_HVLD				
169	**HDMI**	A3	HDMI_CH0_P				
170		B3	HDMI_CH0_M				
171		A2	HDMI_CH1_P				
172		B2	HDMI_CH1_M				
173		A1	HDMI_CH2_P				
174		B1	HDMI_CH2_M				

175		A4	HDMI_CLK_P		
176		B4	HDMI_CLK_M		
177		C4	HDMI_REXT		
178		C3	HDMI_VDDA	2.5V	
179		D4	HDMI_VDDA		
180		E7	HDMI_VDD		
181		C5	HDMI_VSSA		
182		D5	HDMI_VSSA		
183		M4	HDMI_CEC		
184		J5	HDMI_HPD		
185	**IDC2**	K5	IDC2_CLK	GPIO_86	
186		L5	IDC2_DATA	GPIO_87	
187	**Sensor**	AB8	SD_LVDS_0_P		
188	**I/F**	Y9	SD_LVDS_1_P		
189		Y10	SD_LVDS_2_P		
190		AB10	SD_LVDS_3_P		
191		Y11	SD_LVDS_4_P		
192		AB11	SD_LVDS_5_P		
193		AB12	SD_LVDS_6_P		
194		Y13	SD_LVDS_7_P		
195		AA8	SD_LVDS_0_N		
196		W9	SD_LVDS_1_N		
197		W10	SD_LVDS_2_N		
198		AA10	SD_LVDS_3_N		
199		W11	SD_LVDS_4_N		
200		AA11	SD_LVDS_5_N		
201		AA12	SD_LVDS_6_N		
202		W13	SD_LVDS_7_N		
203		AB9	SPCLK_LVDS_0_P		
204		Y12	SPCLK_LVDS_1_P		
205		AA9	SPCLK_LVDS_0_N		
206		W12	SPCLK_LVDS_1_N		
207		AB13	SHSYNC		
208		V14	SVSYNC		
209		AA13	CLK_SI		
210		F18	STRIG_0		

211		E19	STRIG_1	
212		V11	VDDA_LVDS	
213		V12	VSSA_LVDS	
214	MIPI VIN	N22	S_DPDATA_0	
215		P22	S_DPDATA_1	
216		P20	S_DPDATA_2	
217		M21	S_DNDATA_0	
218		N21	S_DNDATA_1	
219		P19	S_DNDATA_2	
220		N20	S_DPCLK	
221		N19	S_DNCLK	
222	MIPI	M18	MS_VDD11	
223	Power	N18	MS_VDD18	1.8V
224		P18	MS_VSS	
225	MIPI DSI	R20	MIPI1_MDATA_P	
226		R19	MIPI1_MDATA_N	
227		T22	MIPI1_MCLK_P	
228		R21	MIPI1_MCLK_N	
229		T20	MIPI1_SDATA_P	
230		T19	MIPI1_SDATA_N	
231		R22	MIPI1_SCLK_P	
232		P21	MIPI1_SCLK_N	
233		R18	M_VDD11_PLL	
234		T21	MIPI1_VREG	
235	ADC	Y8	ADC_CH_3	
236		W8	ADC_CH_2	
237		AB7	ADC_CH_1	
238		AA7	ADC_CH_0	
239		V9	ADC_AVDD	
240		V10	ADC_AVSS	
241	Global	V1	XIN	
242		V2	XOUT	
243		V8	TEST_MODE	
244		Y3	POR_L	
245	PWC	V6	PLL_VFLTR	
246	&	C2	XI_RTC	

247	RTC	D3	XO_RTC								
248		F5	PWC_RTC_CP								
249		E1	PWC_PC_VDD								
250		C1	PWC_PC_REF								
251		D2	PWC_WKUP0								
252		E6	PWC_WKUP1								
253		E5	PWC_WKUP2								
254		E4	PWC_WKUP3								
255		D1	PWC_RSTINB								
256		E3	PWC_PSEQ1								
257		F3	PWC_PSEQ2								
258		F4	PWC_PSEQ3								
259		E2	PWC_RSTOB								
						(NAND)	(SD /MMC)	(PC_Mem)	(CFA_IDE)	HIF	MS
260	SMIO	L1	SMIO_0			CE	.	.	.	D0	
261		M3	SMIO_1			R /-B	.	.	.	D1	
262		J3	(NC)								
263		R1	SMIO_3	GPIO_65		.	CLK	.	.		CLK
264		N1	SMIO_4	GPIO_66		.	CMD	.	.		BS
265		N3	SMIO_5	GPIO_67		.	CD	.	.		
266		N2	SMIO_6	GPIO_68		.	WP	.	.		
267		M2	SMIO_7			.	.	CD1	CD1	D7	
268		H3	SMIO_8			.	.	WAIT	IORDY	D8	
269		G2	SMIO_9			.	.	INPACK	DMARQ	D9	
270		G5	SMIO_10			.	.	WP	IOCS16	D10	
271		H2	SMIO_11			.	.	OE	ATASEL	D11	
272		H1	SMIO_12			.	.	RESET	RESET	D12	
273		K1	SMIO_13			.	.	CE1	CS1	D13	
274		J4	SMIO_14			.	.	CE2	CS2	D14	
275		K4	SMIO_15			RE	.	IOWR	IOWR	D15	
276		K2	SMIO_16			.	.	IORD	IORD	RDY	
277		H4	SMIO_17			.	.	REG	DMACK	A0	
278		J1	SMIO_18			.	.	WE	WE	A1	
279		H5	SMIO_19			WE	.	D0	D0	A2	
280		F2	SMIO_20			ALE	.	D1	D1	OE	
281		G3	SMIO_21			D0	.	D2	D2	WE	

282		L3	SMIO_22			D1	.	D3	D3	CS	
283		K3	SMIO_23			D2	.	D4	D4	D2	
284		L2	SMIO_24			D3	.	D5	D5	D3	
285		J2	SMIO_25			D4	.	D6	D6	D4	
286		L4	SMIO_26			D5	.	D7	D7	D5	
287		G1	SMIO_27			D6	.	D8	D8	D6	
288		G4	SMIO_28			D7	.	D9	D9		
289		F1	SMIO_29			CLE	.	D10	D10		
290		R2	SMIO_30			.	D0	D11	D11		D0
291		U3	SMIO_31			.	D1	D12	D12		D1
292		P3	SMIO_32			.	D2	D13	D13		D2
293		P2	SMIO_33			.	D3	D14	D14		D3
294	**SMIO**	R3	SMIO_34			.	D4	D15	D15		D4
295		R4	SMIO_35			.	D5	A0	A0		D5
296		P4	SMIO_36			.	D6	A1	A1		D6
297		P1	SMIO_37			.	D7	A2	A2		D7
298		T4	SMIO_38	GPIO_69		.	SDIO_CLK	A3	.		
299		T3	SMIO_39	GPIO_70		.	SDIO_CMD	A4	.		
300		M1	SMIO_40	GPIO_71		.	SDIO_D0	A5	.		
301		N4	SMIO_41	GPIO_72		.	SDIO_D1	A6	.		
302		T2	SMIO_42	GPIO_73		.	SDIO_D2	A7	.		
303		T1	SMIO_43	GPIO_74		.	SDIO_D3	A8	.		
304		U4	SMIO_44	GPIO_75		.	SDIO_CD	A9	.		
305		U2	SMIO_45	GPIO_76		.	SDIO_WP	A10	.		
306	**POWER**	H8	VDD33	IO Vdd							
307		K8	VDD33								
308		M8	VDD33								
309		P8	VDD33								
310		H15	VDD33_BYP	IO Vdd for when chip is in bypass mode							
311		K15	VDD33_BYP								
312		M15	VDD33_BYP								
313		P15	VDD33_BYP								
314		P5	VDDA_PLL								

315	R5	VDDA_PLL	
316	M5	VDDA18_PLL	
317	N5	VDDA18_PLL	
318	E8	VDD	
319	E13	VDD	
320	E15	VDD	
321	H9	VDD	
322	H10	VDD	
323	H11	VDD	
324	H12	VDD	
325	H13	VDD	
326	H14	VDD	
327	N9	VDD	
328	P9	VDD	
329	P10	VDD	
330	P11	VDD	
331	P12	VDD	
332	P13	VDD	
333	P14	VDD	
334	R11	VDD	
335	R12	VDD	
336	R13	VDD	
337	W19	VDD	
338	V13	VSS	
339	E17	VDD_BYP	Vdd for when chip
340	R9	VDD_BYP	is in bypass mode
341	R14	VDD_BYP	
342	C13	DDR_VDDQ	
343	D6	DDR_VDDQ	
344	D8	DDR_VDDQ	
345	D10	DDR_VDDQ	
346	D12	DDR_VDDQ	
347	D14	DDR_VDDQ	
348	D16	DDR_VDDQ	
349	D18	DDR_VDDQ	
350	D20	DDR_VDDQ	

351		E11	DDR_VDDQ
352	GROUND	E9	VSS
353		E14	VSS
354		E16	VSS
355		E18	VSS
356		J9	VSS
357		J10	VSS
358		J11	VSS
359		J12	VSS
360		J13	VSS
361		J14	VSS
362		K9	VSS
363		K10	VSS
364		K11	VSS
365		K12	VSS
366		K13	VSS
367		K14	VSS
368		L9	VSS
369		L10	VSS
370		L11	VSS
371		L12	VSS
372		L13	VSS
373		L14	VSS
374		M9	VSS
375		M10	VSS
376		M11	VSS
377		M12	VSS
378		M13	VSS
379		M14	VSS
380		N10	VSS
381		N11	VSS
382		N12	VSS
383		N13	VSS
384		N14	VSS
385		J8	VSS33
386		J15	VSS33

387		L8	VSS33	
388		L15	VSS33	
389		N8	VSS33	
390		N15	VSS33	
391		R8	VSS33	
392		R15	VSS33	
393		D7	DDR_VSSQ	
394		D9	DDR_VSSQ	
395		D11	DDR_VSSQ	
396		D13	DDR_VSSQ	
397		D15	DDR_VSSQ	
398		D17	DDR_VSSQ	
399		D19	DDR_VSSQ	
400		D21	DDR_VSSQ	
401		E10	DDR_VSSQ	
402		E12	DDR_VSSQ	
403		T5	VSSA_PLL	
404		U5	VSSA_PLL	