1/4-Inch Color NTSC/PAL Digital Image SOC with Overlay Processor

ASX340/MT9V139 Data Sheet

For the latest data sheet, refer to Aptina's Web site: www.aptina.com or www.sunnywale.com

Features

- Low-power image sensor with integrated image flow processor (IFP) and video encoder
- 1/4-inch optical format, VGA resolution (640H x 480V)
- 2x upscaling zoom and pan control
- ±40 additional columns and ±36 additional rows to compensate for lens alignment tolerances
- Option to use single 2.8V power supply with off-chip bypass transistor
- Overlay generator for dynamic bitmap overlay
- Integrated video encoder for NTSC/PAL with overlay capability and 10-bit I-DAC
- Integrated microcontroller for flexibility
- On-chip image flow processor performs sophisticated processing, such as color recovery and correction, sharpening, gamma, lens shading correction, on-the-fly defect correction, auto white balancing, and auto exposure
- Auto black level calibration
- 10-bit, on-chip analog-to-digital converter (ADC)
- Internal master clock generated by on-chip phase-locked loop (PLL)
- Two-wire serial programming interface
- Interface to low-cost EEPROM and Flash through SPI bus
- High-level host command interface
- Stand-alone operation support
- Comprehensive tool support for overlay generation and lens correction setup
- Development system with DevWare

Applications

- Analog surveillance CCTV
- Surveillance network IP camera

See "Ordering Information" on page 3.
See details of new features on page 3.

Table 1: Key Parameters

Parameter	Typical Value
Pixel size and type	5.6µm x 5.6µm active pinned-photodiode with high-sensitivity mode for low-light conditions
Sensor format	728H x 560V (includes ±36 rows and ±40 columns for lens alignment)
NTSC output	720H x 480V
PAL output	720H x 576V
Imaging area	Total array size: 3.584mm x 2.688mm
Optical format	¼-inch
Frame rate	50/60 fields/sec
Sensor scan mode	Progressive scan
Color filter array	RGB standard Bayer
Shutter type	Electronic rolling shutter (ERS)
Automatic Functions	Exposure, white balance, black level offset correction, flicker detection and avoidance, color saturation control, on-the-fly defect correction, aperture correction
Programmable Controls	Exposure, white balance, horizontal and vertical blanking, color, sharpness, gamma correction, lens shading correction, horizontal and vertical image flip, zoom, windowing, sampling rates, GPIO control

Key parameters are continued on next page.

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Table 2: Key Parameters (continued)

Parameter		Typical Value
Overlay Support		Utilizes SPI interface to load overlay data from external flash/EEPROM memory with the following features: •Available in Analog output and BT656 Digital output •Overlay Size 360 x 480 pixel rendered into 720 x 480 (NTSC) or 720 x 576 (PAL) •Up to four (4) overlays may be blended simultaneously •Selectable readout: Rotating order user selected •Dynamic scenes by loading pre-rendered frames from external memory •Palette of 32 colors out of 64,000 •8 colors per bitmap •Blend factor dynamically programmable for smooth transitions •Fast Update rate of up to 30 fps •Every bitmap object has independent x/y position •Statistic Engine to calibrate optical alignment •Number Generator
Windowing		Programmable to any size
Analog gain range		0.5–80x
ADC		10-bit, on-chip
Output interface		Analog composite video out, single-ended or differential; 8-, 10-bit parallel digital output
Output data formats[1]		Digital: Raw Bayer 8-,10-bit, CCIR656, 565RGB, 555RGB, 444RGB
Data rate		Parallel: 27 MB/s
		NTSC: 60 fields/sec
		PAL: 50 fields/sec
Control interface		Two-wire I/F for register interface plus high-level command exchange. SPI port to interface to external memory to load overlay data, register settings, or firmware extensions.
Input clock for PLL		27 MHz
SPI Clock Frequencies		1.6875 – 18 MHz, programmable
Supply voltage		Analog: 2.8V ±5%
		Core: 1.8V ±5%
		IO: 2.8V ±5%
Power consumption	Analog output only	Full resolution at 60 fps: 236 mW
	Digital output only	Full resolution at 60 fps: 234 mW
Package		63-cBGA, 7 mm x 7 mm 0.65mm pin pitch 63- CSP, 6.198 x 6.178 mm, 0.65mm pin pitch
Ambient temperature		Operating: -30°C to 70°C
		Storage: –50°C to +150°C
Dark Current		< 200e/s at 60°C with a gain of 1
Fixed pattern noise	Column	< 2%
	Row	< 2%
Responsivity		16.5 V/lux-s at 550nm
Signal to noise ratio (S/N)		46 dB
Pixel dynamic range		74.8 dB

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Ordering Information

Table 3: Available Part Numbers

Part Number	Description
ASX340CS2C00SPEA0-E	63-ball cBGA, AS/ES
ASX340CS2C00SPEA0	63-ball cBGA, MP
ASX340CS2C00SPEAH-E	63-ball cBGA, Headboard
ASX340CS2C00SPEAD-E	63-ball cBGA, Demo
MT9V139I83STC ES	CSP ES part number
MT9V139I83STCD ES	Demo kit
MT9V139I83STCH ES	Head Board

New Features

- Automatic 50hz/60hz flicker detection
- 2x upscaling zoom and pan/tilt control
- Independent control of colorburst parameters in the NTSC/PAL encoder
- Horizontal field of view adjustment between 700 and 720 pixels on the analog output
- Option to use single 2.8V power supply with off-chip bypass transistor
- SPI EEPROM support for lower cost system design.

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General Description

The Aptina® ASX340/MT9V139 is a VGA-format, single-chip active-pixel digital image sensor for surveillance applications. It captures high-quality color images at VGA resolution and outputs NTSC or PAL interlaced composite video.

The VGA image sensor features Aptina's breakthrough low-noise imaging technology that achieves superior image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, low power, and integration advantages of Aptina's advanced active pixel process technology.

The ASX340/MT9V139 is a complete camera-on-a-chip. It incorporates sophisticated camera functions on-chip and is programmable through a simple two-wire serial interface or by an attached SPI EEPROM or Flash memory that contains setup information that may be loaded automatically at startup.

The ASX340/MT9V139 performs sophisticated processing functions including color recovery, color correction, sharpening, programmable gamma correction, auto black reference clamping, auto exposure, 50Hz/60Hz flicker detection and avoidance, lens shading correction, auto white balance (AWB), and on-the-fly defect identification and correction.

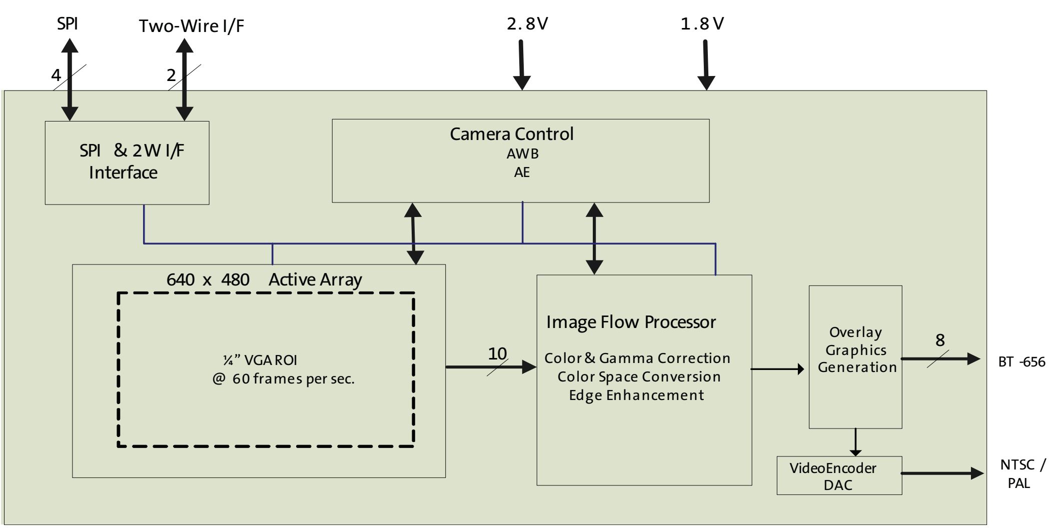
The ASX340/MT9V139 outputs interlaced-scan images at 60 or 50 Fields per Second, supporting both NTSC and PAL video formats. The image data can be output on one or two output ports:

- Composite analog video (single-ended and differential output support)
- Parallel 8-, 10-bit digital

Architecture

Internal Block Diagram

Figure 1: Internal Block Diagram



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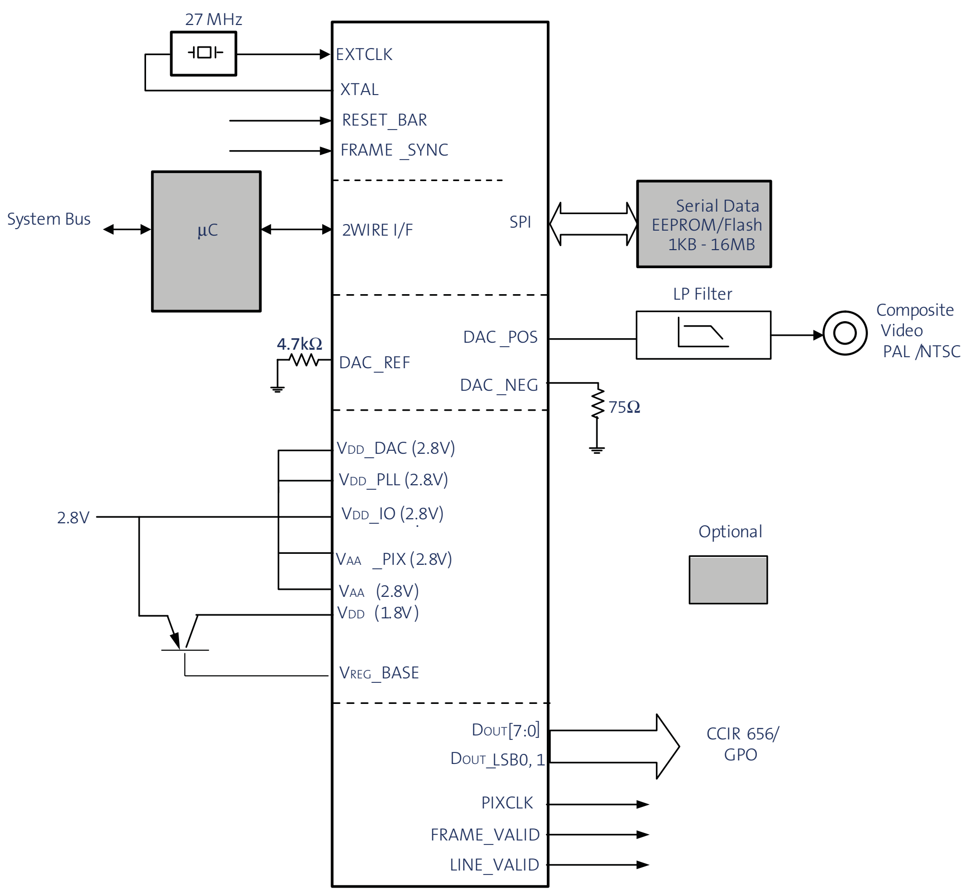
System Block Diagram

The system block diagram will depend on the application. The system block diagram in Figure 2 shows all components; optional peripheral components are highlighted. The optional microcontroller controls the ASX340/MT9V139 sensor using the two-wire serial bus. Optional components will vary by application. For further details, see the ASX340/MT9V139 Register and Variable Reference.

Figure 2: System Block Diagram



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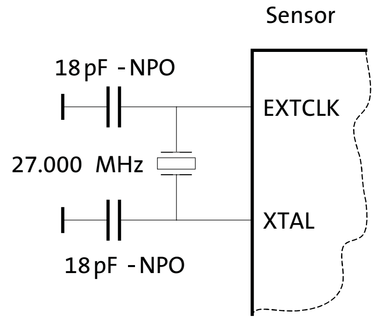
Crystal Usage

As an alternative to using an external oscillator, a fundamental 27 MHz crystal may be connected between EXTCLK and XTAL. Two small loading capacitors of 10–22 pF of NPO dielectric should be added as shown in Figure 3.

Aptina does not recommend using the crystal option for applications above 85°C. A crystal oscillator with temperature compensation is recommended.

Figure 3: Using a Crystal Instead of an External Oscillator



Note: Value of load cap is Xtal dependent. Xtal with small load cap is recommended.

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Pin Descriptions and Assignments

Table 4: Pin Descriptions

Pin Number	Pin Name	Type	Description
Clock and Reset			
A2	EXTCLK	Input	Master input clock (27MHz): This can either be a square-wave generated from an oscillator (in which case the XTAL input must be left unconnected) or connected directly to a crystal.
B1	XTAL	Output	If EXTCLK is connected to one pin of a crystal, this signal is connected to the other pin; otherwise this signal must be left unconnected.
D2	RESET_BAR	Input	Asynchronous active-low reset: When asserted, the device will return all interfaces to their reset state. When released, the device will initiate the boot sequence. This signal has an internal pull-up resistor.
E1	FRAME_SYNC	Input	This input can be used to set the output timing of the ASX340/MT9V139 to a fixed point in the frame. The input buffer associated with this input is permanently enabled. This signal must be connected to GND if not used.
Register Interface			
F1	SCLK	Input	These two signals implement serial communications protocol for access to the internal registers and variables.
F2	SDATA	Input/Output	
E2	SADDR	Input	This signal controls the device ID that will respond to serial communication commands. Two-wire serial interface device ID selection: 0: 0x90 1: 0xBA
SPI Interface			
D4	SPI_SCLK	Output	Clock output for interfacing to an external SPI memory such as Flash/EEPROM. Tristate when RESET_BAR is asserted.
E4	SPI_SDI	Input	Data in from SPI device. This signal has an internal pull-up resistor.
H3	SPI_SDO	Output	Data out to SPI device. Tristate when RESET_BAR is asserted.
H2	SPI_CS_N	Output	Chip selects to SPI device. Tristate when RESET_BAR is asserted.
(Parallel) Pixel Data Output			
F7	FRAME_VALID	Input/Output	Pixel data from the ASX340/MT9V139 can be routed out on this interface and processed externally. To save power, these signals are driven to a constant logic level unless the parallel pixel data output or alternate (GPIO) function is enabled for these pins. For more information see Table 16 on page 33. This interface is disabled by default. The slew rate of these outputs is programmable. These signals can also be used as general purpose input/outputs.
G7	LINE_VALID	Input/Output	
E6	PIXCLK	Output	
F8, D6, D7, C6, C7, B6, B7, A6	DOUT[7:0]	Output	
B3	DOUT_LSB1	Input/Output	When the sensor core is running in bypass mode, it will generate 10 bits of output data per pixel. These two pins make the two LSB of pixel data available externally. Leave DOUT_LSB1 unconnected if not used. To save power, these signals are driven to a constant logic level unless the sensor core is running in bypass mode or the alternate function is enabled for these pins. For more information see Table 16, "GPIO Bit Descriptions," on page 38. The slew rate of these outputs is programmable.
C2	DOUT_LSB0	Input/Output	

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Table 4: Pin Descriptions (continued)

Pin Number	Pin Name	Type	Description
			Composite Video Output
F5	DAC_POS	Output	Positive video DAC output in differential mode. Video DAC output in single-ended mode. This interface is enabled by default using NTSC/PAL signalling. For applications where composite video output is not required, the video DAC can be placed in a power-down state under software control.
G5	DAC_NEG	Output	Negative video DAC output in differential mode.
A4	DAC_REF	Output	External reference resistor for the video DAC.
			Manufacturing Test Interface
D3	TDI	Input	JTAG Test pin (Reserved for Test Mode)
G2	TDO	Output	JTAG Test pin (Reserved for Test Mode)
F3	TMS	Input	JTAG Test pin (Reserved for Test Mode)
C3	TCK	Input	JTAG Test pin (Reserved for Test Mode)
C4	TRST_N	Input	Connect to GND.
G6	ATEST1	Input	Analog test input. Connect to GND in normal operation.
F6	ATEST2	Input	Analog test input. Connect to GND in normal operation.
			GPIO
C1	GPIO12	Input/Output	Dedicated general-purpose input/output pin.
A3	GPIO13	Input/Output	Dedicated general-purpose input/output pin.
			Power
G4	VREG_BASE	Supply	Voltage regulator control. Leave floating if not used.
A5, A7, D8, E7, G1, G3	VDD	Supply	Supply for VDD core: 1.8V nominal. Can be connected to the output of the transistor of the off-chip bypass transistor or a external 1.8V power supply.
B2, B8, C8, E3, E8, G8, H8	VDD_IO	Supply	Supply for digital IOs: 2.8V nominal.
H5	VDD_DAC	Supply	Supply for video DAC: 2.8V nominal.
A8	VDD_PLL	Supply	Supply for PLL: 2.8V nominal.
B4, H6	VAA	Supply	Analog power: 2.8V nominal.
H7	VAA_PIX	Supply	Analog pixel array power: 2.8V nominal. Must be at same voltage potential as VAA.
H4	Reserved		
B5, C5, D1, D5, H1	DGND	Supply	Digital ground.
E5, F4	AGND	Supply	Analog ground.

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Pin Assignments

Pin 1 is not populated with a ball. That allows the device to be identified by an additional marking.

Table 5: Pin Assignments

	1	2	3	4	5	6	7	8
A		EXTCLK	GPIO13	DAC_REF	VDD	DOUT0	VDD	VDD_PLL
B	XTAL	VDD_IO	DOUT_LSB1	VAA	GND	DOUT2	DOUT1	VDD_IO
C	GPIO12	DOUT_LSB0	TCK	TRST_N	GND	DOUT4	DOUT3	VDD_IO
D	GND	RESET_BAR	TDI	SPI_SCLK	GND	DOUT6	DOUT5	VDD
E	FRAME_SYNC	SADDR	VDD_IO	SPI_SDI	AGND	PIXCLK	VDD	VDD_IO
F	SCLK	SDATA	TMS	AGND	DAC_POS	ATEST2	FRAME_VALID	DOUT7
G	VDD	TDO	VDD	VREG_BASE	DAC_NEG	ATEST1	LINE_VALID	VDD_IO
H	GND	SPI_CS_N	SPI_SDO	Reserved	VDD_DAC	VAA	VAA_PIX	VDD_IO

Table 6: Reset/Default State of Interfaces

Name	Reset State	Default State	Notes
EXTCLK	Clock running or stopped	Clock running	Input
XTAL	N/A	N/A	Input
RESET_BAR	Asserted	De-asserted	Input
SCLK	N/A	N/A	Input. Must always be driven to a valid logic level.
SDATA	High impedance	High impedance	Input/Output. A valid logic level should be established by pull-up resistor.
SADDR	N/A	N/A	Input. Must always be driven to a valid logic level. Must be permanently tied to VDD_IO or GND.
SPI_SCLK	High impedance.	Driven, logic 0	Output. Output enable is R0x0032[13].
SPI_SDI	Internal pull-up enabled.	Internal pull-up enabled	Input. Internal pull-up is permanently enabled.
SPI_SDO	High impedance	Driven, logic 0	Output enable is R0x0032[13].
SPI_CS_N	High impedance	Driven, logic 1	Output enable is R0x0032[13].
FRAME_VALID LINE_VALID	High impedance	High impedance	Input/Output. This interface disabled by default. Input buffers (used for GPIO function) powered down by default, so these pins can be left unconnected (floating). After reset, these pins are powered up, sampled, then powered down again as part of the auto-configuration mechanism. See Note 2.
PIXCLK DOUT7 DOUT6 DOUT5 DOUT4 DOUT3 DOUT2 DOUT1 DOUT0	High impedance	Driven, logic 0	Output. This interface disabled by default. See Note 1.

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Table 6: Reset/Default State of Interfaces (continued)

Name	Reset State	Default State	Notes
DOUT_LSB1	High impedance	High impedance	Input/Output. This interface disabled by default. Input buffers (used for GPIO function) powered down by default, so these pins can be left unconnected (floating). After reset, these pins are powered-up, sampled, then powered down again as part of the auto-configuration mechanism.
DOUT_LSB0	High impedance	HIgh impedance	
DAC_POS	High impedance	Driven	Output. Interface disabled by hardware reset and enabled by default when the device starts streaming.
DAC_NEG			
DAC_REF			
TDI	Internal pull-up enabled	Internal pull-up enabled	Input. Internal pull-up means that this pin can be left unconnected (floating).
TDO	High impedance	High impedance	Output. Driven only during appropriate parts of the JTAG shifter sequence.
TMS	Internal pull-up enabled	Internal pull-up enabled	Input. Internal pull-up means that this pin can be left unconnected (floating).
TCK	Internal pull-up enabled	Internal pull-up enabled	Input. Internal pull-up means that this pin can be left unconnected (floating).
TRST_N	N/A	N/A	Input. Must always be driven to a valid logic level. Must be driven to GND for normal operation.
FRAME_SYNC	N/A	N/A	Input. Must always be driven to a valid logic level. Must be driven to GND for normal operation.
GPIO12	High impedance	High impedance	Input/Output. This interface disabled by default. Input buffers (used for GPIO function) powered down by default, so these pins can be left unconnected (floating). After reset, these pins are powered-up, sampled, then powered down again as part of the auto-configuration mechanism.
GPIO13	High impedance	High impedance	Input/Output. This interface disabled by default. Input buffers (used for GPIO function) powered down by default, so these pins can be left unconnected (floating). After reset, these pins are powered-up, sampled, then powered down again as part of the auto-configuration mechanism.
ATEST1	N/A	N/A	Must be driven to GND for normal operation.
ATEST2	N/A	N/A	Must be driven to GND for normal operation.

Notes:
1. The reason for defining the default state as logic 0 rather than high impedance is this: when wired in a system (for example, on our demo boards), these outputs will be connected, and the inputs to which they are connected will want to see a valid logic level. No current drain should result from driving these to a valid logic level (unless there is a pull-up at the system level).
2. These pads have their input circuitry powered down, but they are not output-enabled. Therefore, they can be left floating but they will not drive a valid logic level to an attached device.

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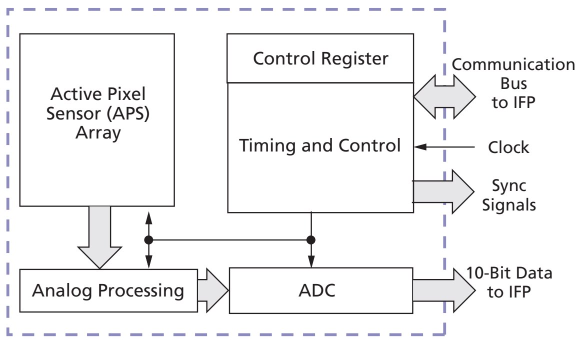
SOC Description

Detailed Architecture Overview

Sensor Core

The sensor consists of a pixel array, an analog readout chain, a 10-bit ADC with programmable gain and black offset, and timing and control as illustrated in Figure 4.

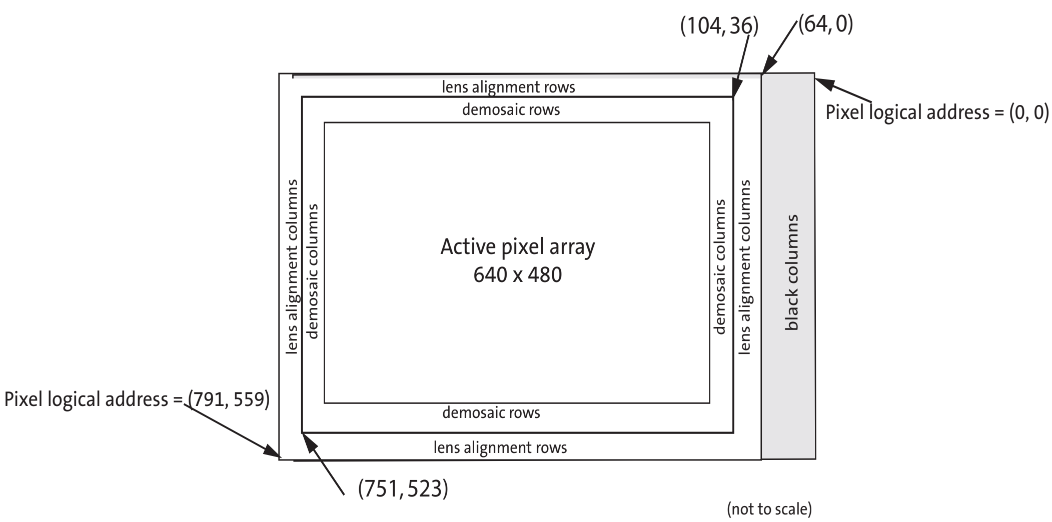
Figure 4: Sensor Core Block Diagram



Pixel Array Structure

The sensor core pixel array is configured as 792 columns by 560 rows, as shown in Figure 5.

Figure 5: Pixel Array Description



Black rows used internally for automatic black level adjustment are not addressed by default, but can be read out in raw output mode via a register setting.

There are 792 columns by 560 rows of optically-active pixels that include a pixel boundary around the VGA (640 x 480) image to avoid boundary effects during color interpolation and correction.

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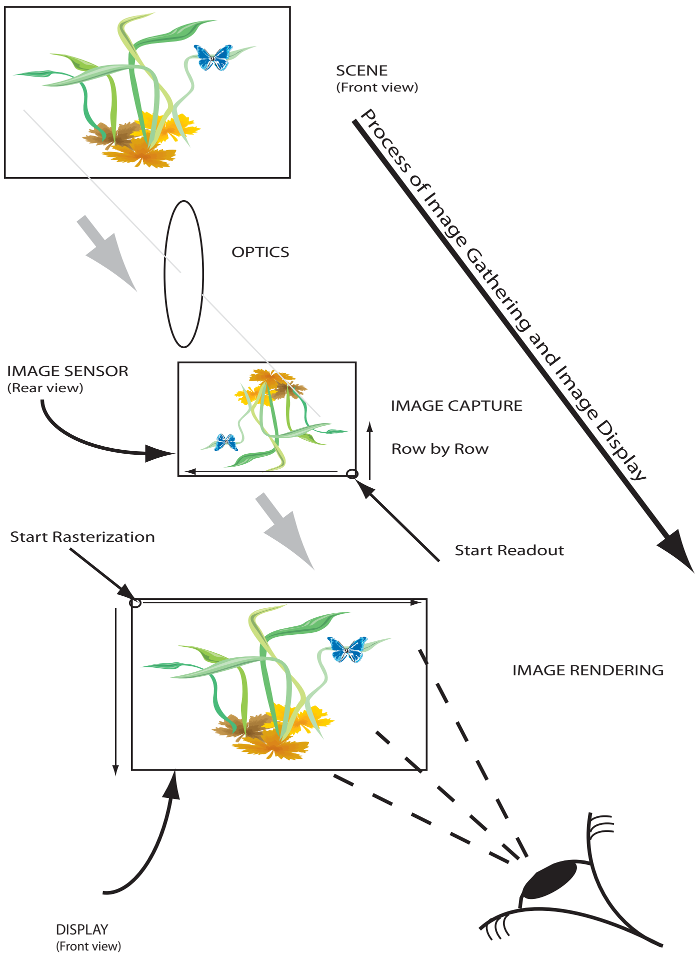
Figure 6 illustrates the process of capturing the image. The original scene is flipped and mirrored by the sensor optics. Sensor readout starts at the lower right corner. The image is presented in true orientation by the output display.

Figure 6: Image Capture Example



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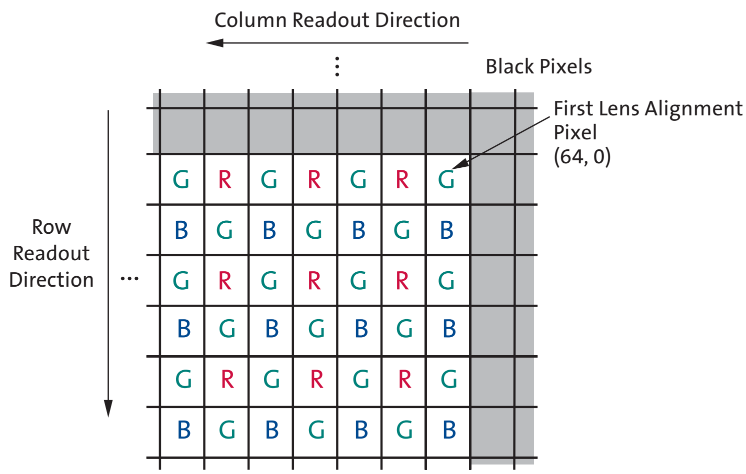
Sensor Pixel Array

The active pixel array is 640 x 480 pixels. In addition, there are 72 rows and 80 columns for lens alignment and 8 rows and 8 columns for demosaic.

Figure 7: Pixel Color Pattern Detail (top right corner)



Output Data Format

The sensor core image data are read out in progressive scan order. Valid image data are surrounded by horizontal and vertical blanking, shown in Figure 8.

For NTSC output, the horizontal size is stretched from 640 to 720 pixels. The vertical size is 243 pixels per field; 240 image pixels and 3 dark pixels that are located at the bottom of the image field.

For PAL output, the horizontal size is also stretched from 640 to 720 pixels. The vertical size is 288 pixels per field.

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Figure 8: Spatial Illustration of Image Readout

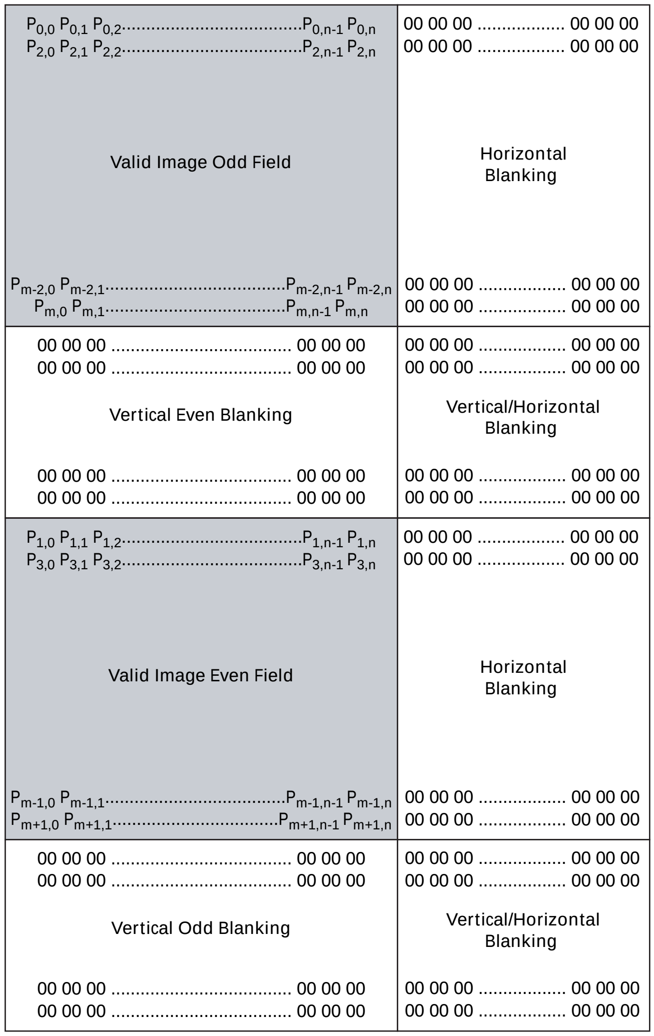

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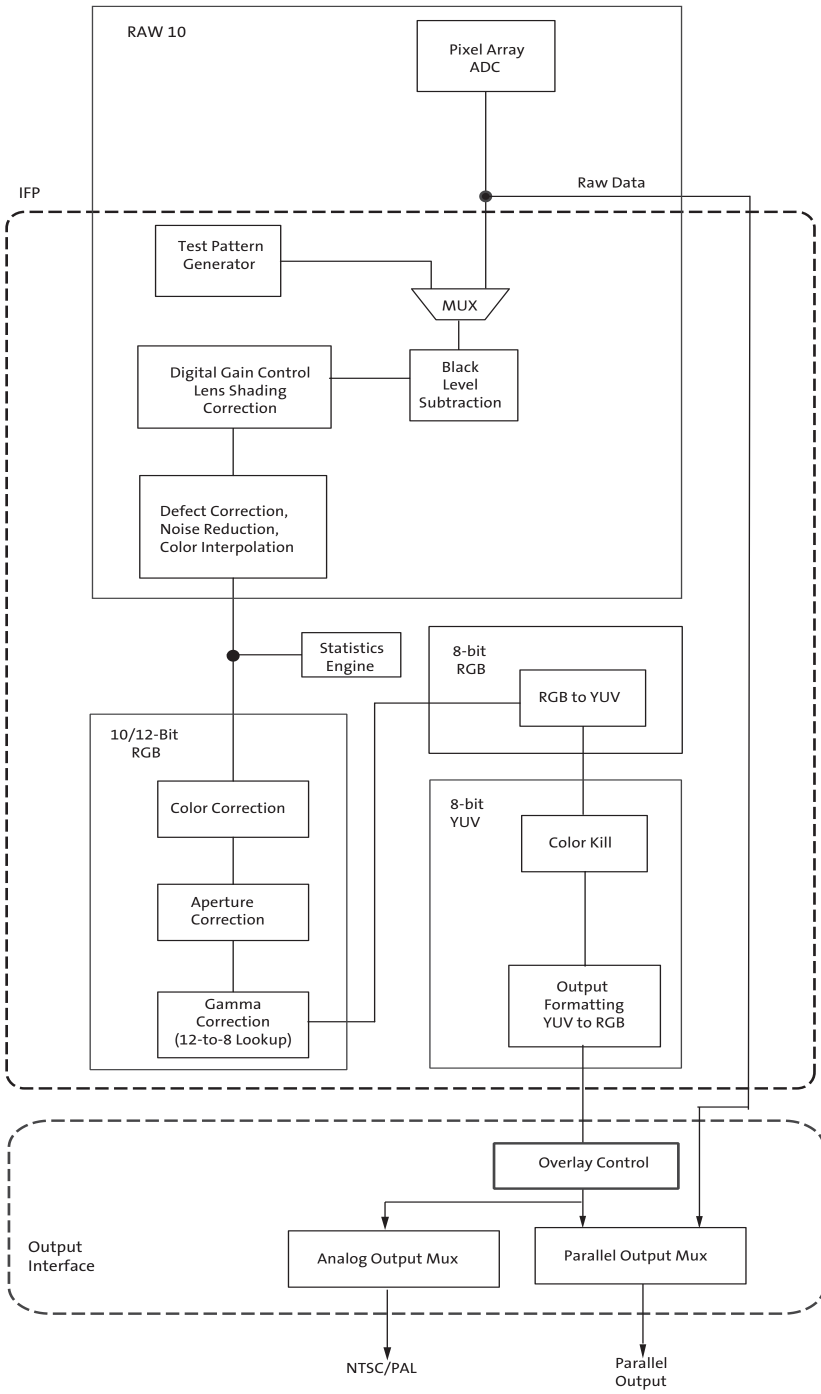
Image Flow Processor

Image and color processing in the ASX340/MT9V139 are implemented as an image flow processor (IFP) coded in hardware logic. During normal operation, the embedded microcontroller will automatically adjust the operation parameters. The IFP is broken down into different sections, as outlined in Figure 9.

Figure 9: Color Pipeline



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Test Patterns

During normal operation of the ASX340/MT9V139, a stream of raw image data from the sensor core is continuously fed into the color pipeline. For test purposes, this stream can be replaced with a fixed image generated by a special test module in the pipeline. The module provides a selection of test patterns sufficient for basic testing of the pipeline.

NTSC/PAL Test Pattern Generation

There is a built-in standard EIA (NTSC) and EBU (PAL) color bars to support hue and color saturation characterization. Each pattern consists of seven color bars (white, yellow, cyan, green, magenta, red, and blue). The Y, Cb and Cr values for each bar are detailed in Tables 7 and 8.

Figure 10: Color Bars

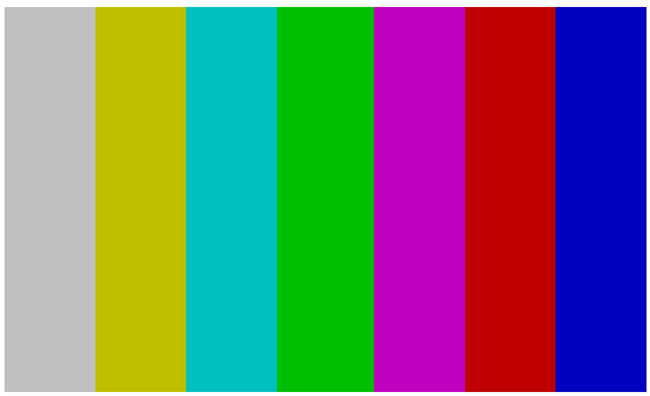

Table 7: EIA Color Bars (NTSC)

	Nominal Range	White	Yellow	Cyan	Green	Magenta	Red	Blue
Y	16 to 235	180	162	131	112	84	65	35
Cb	16 to 240	128	44	156	72	184	100	212
Cr	16 to 240	128	142	44	58	198	212	114

Table 8: EBU Color Bars (PAL)

	Nominal Range	White	Yellow	Cyan	Green	Magenta	Red	Blue
Y	16 to 235	235	162	131	112	84	65	35
Cb	16 to 240	128	44	156	72	184	100	212
Cr	16 to 240	128	142	44	58	198	212	114

CCIR-656 Format

The color bar data is encoded in 656 data streams. The duration of the blanking and active video periods of the generated 656 data are summarized in the following tables.

Table 9: NTSC

Line Numbers	Field	Description
1-3	2	Blanking
4-19	1	Blanking
20-263	1	Active video

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Table 9: NTSC

Line Numbers	Field	Description
264-265	1	Blanking
266-282	2	Blanking
283-525	2	Active Video

Table 10: PAL

Line Numbers	Field	Description
1-22	1	Blanking
23-310	1	Active video
311-312	1	Blanking
313-335	2	Blanking
336-623	2	Active video
624-625	2	Blanking

Black Level Subtraction and Digital Gain

Image stream processing starts with black level subtraction and multiplication of all pixel values by a programmable digital gain. Both operations can be independently set to separate values for each color channel (R, Gr., Gb, B). Independent color channel digital gain can be adjusted with registers. Independent color channel black level adjustments can also be made. If the black level subtraction produces a negative result for a particular pixel, the value of this pixel is set to 0.

Positional Gain Adjustments (PGA)

Lenses tend to produce images whose brightness is significantly attenuated near the edges. There are also other factors causing fixed pattern signal gradients in images captured by image sensors. The cumulative result of all these factors is known as image shading. The ASX340/MT9V139 has an embedded shading correction module that can be programmed to counter the shading effects on each individual R, Gb, Gr., and B color signal.

The Correction Function

The correction functions can then be applied to each pixel value to equalize the response across the image as follows:

$$P_{corrected}(row,col) = P_{sensor}(row,col) * f(row,col) \qquad \text{(EQ 1)}$$

where *P* are the pixel values and *f* is the color dependent correction functions for each color channel.

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Color Interpolation

In the raw data stream fed by the sensor core to the IFP, each pixel is represented by a 10-bit integer number, which can be considered proportional to the pixel's response to a one-color light stimulus, red, green, or blue, depending on the pixel's position under the color filter array. Initial data processing steps, up to and including the defect correction, preserve the one-color-per-pixel nature of the data stream, but after the defect correction it must be converted to a three-colors-per-pixel stream appropriate for standard color processing. The conversion is done by an edge-sensitive color interpolation module. The module pads the incomplete color information available for each pixel with information extracted from an appropriate set of neighboring pixels. The algorithm used to select this set and extract the information seeks the best compromise between preserving edges and filtering out high frequency noise in flat field areas. The edge threshold can be set through register settings.

Color Correction and Aperture Correction

To achieve good color fidelity of the IFP output, interpolated RGB values of all pixels are subjected to color correction. The IFP multiplies each vector of three pixel colors by a 3 x 3 color correction matrix. The three components of the resulting color vector are all sums of three 10-bit numbers. Since such sums can have up to 12 significant bits, the bit width of the image data stream is widened to 12 bits per color (36 bits per pixel). The color correction matrix can be either programmed by the user or automatically selected by the auto white balance (AWB) algorithm implemented in the IFP. Color correction should ideally produce output colors that are corrected for the spectral sensitivity and color crosstalk characteristics of the image sensor. The optimal values of the color correction matrix elements depend on those sensor characteristics and on the spectrum of light incident on the sensor. The color correction variables can be adjusted through register settings.

To increase image sharpness, a programmable 2D aperture correction (sharpening filter) is applied to color-corrected image data. The gain and threshold for 2D correction can be defined through register settings.

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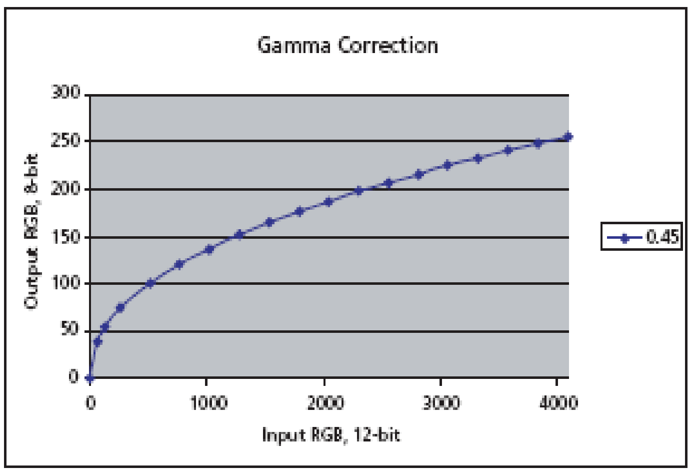
Gamma Correction

The ASX340/MT9V139 includes a block for gamma correction that can adjust its shape based on brightness to enhance the performance under certain lighting conditions. Two custom gamma correction tables may be uploaded corresponding to a brighter lighting condition and a darker lighting condition. At power-up, the IFP loads the two tables with default values. The final gamma correction table used depends on the brightness of the scene and takes the form of an interpolated version of the two tables.

The gamma correction curve (as shown in Figure 11) is implemented as a piecewise linear function with 19 knee points, taking 12-bit arguments and mapping them to 8-bit output. The abscissas of the knee points are fixed at 0, 64, 128, 256, 512, 768, 1024, 1280, 1536, 1792, 2048, 2304, 2560, 2816, 3072, 3328, 3584, 3840, and 4096. The 8-bit ordinates are programmable through registers.

Figure 11: Gamma Correction Curve



RGB to YUV Conversion

For further processing, the data is converted from RGB color space to YUV color space.

Color Kill

To remove high-or low-light color artifacts, a color kill circuit is included. It affects only pixels whose luminance exceeds a certain preprogrammed threshold. The U and V values of those pixels are attenuated proportionally to the difference between their luminance and the threshold.

YUV Color Filter

As an optional processing step, noise suppression by one-dimensional low-pass filtering of Y and/or UV signals is possible. A 3- or 5-tap filter can be selected for each signal.

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YUV-to-RGB/YUV Conversion and Output Formatting

The YUV data stream emerging from the colorpipe can either exit the color pipeline as-is or be converted before exit to an alternative YUV or RGB data format.

Output Format and Timing

YUV/RGB Data Ordering

The ASX340/MT9V139 supports swapping YCbCr mode, as illustrated in Table 11.

Table 11: YCbCr Output Data Ordering

Mode	Data Sequence			
Default (no swap)	Cb_i	Y_i	Cr_i	Y_{i+1}
Swapped CbCr	Cr_i	Y_i	Cb_i	Y_{i+1}
Swapped YC	Y_i	Cb_i	Y_{i+1}	Cr_i
Swapped CbCr, YC	Y_i	Cr_i	Y_{i+1}	Cb_i

The RGB output data ordering in default mode is shown in Table 12. The odd and even bytes are swapped when luma/chroma swap is enabled. R and B channels are bit-wise swapped when chroma swap is enabled.

Table 12: RGB Ordering in Default Mode

Mode (Swap Disabled)	Byte	$D_7D_6D_5D_4D_3D_2D_1D_0$
565RGB	Odd	$R_7R_6R_5R_4R_3G_7G_6G_5$
	Even	$G_4G_3G_2B_7B_6B_5B_4B_3$
555RGB	Odd	$0\ R_7R_6R_5R_4R_3G_7G_6$
	Even	$G_5G_4G_3B_7B_6B_5B_4B_3$
444xRGB	Odd	$R_7R_6R_5R_4G_7G_6G_5G_4$
	Even	$B_7B_6B_5B_4\ 0\ 0\ 0\ 0$
x444RGB	Odd	$0\ 0\ 0\ 0\ R_7R_6R_5R_4$
	Even	$G_7G_6G_5G_4B_7B_6B_5B_4$

Uncompressed 10-Bit Bypass Output

Raw 10-bit Bayer data from the sensor core can be output in bypass mode in two ways:

- Using 8 data output signals (DOUT[7:0]) and GPIO[1:0]. The GPIO signals are the least significant 2 bits of data.
- Using only 8 signals (DOUT[7:0]) and a special 8 + 2 data format, shown in Table 13.

Table 13: 2-Byte Bayer Format

Byte	Bits Used	Bit Sequence
Odd bytes	8 data bits	$D_9D_8D_7D_6D_5D_4D_3D_2$
Even bytes	2 data bits + 6 unused bits	$0\ 0\ 0\ 0\ 0\ 0\ D_1D_0$

Readout Formats

Progressive format is used for raw Bayer output.

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Output Formats

ITU-R BT.656 and RGB Output

TheASX340/MT9V139 can output processed video as a standard ITU-R BT.656 (CCIR656) stream, an RGB stream, or as unprocessed Bayer data. The ITU-R BT.656 stream contains YCbCr 4:2:2 data with embedded synchronization codes. This output is typically suitable for subsequent display by standard video equipment or JPEG/MPEG compression.

Colorpipe data (pre-lens correction and overlay) can also be output in YCbCr 4:2:2 and a variety of RGB formats in 640 by 480 progressive format in conjunction with LINE_VALID and FRAME_VALID.

The ASX340/MT9V139 can be configured to output 16-bit RGB (565RGB), 15-bit RGB (555RGB), and two types of 12-bit RGB (444RGB). Refer to Table 30 and Table 31 on page 56 for details.

Bayer Output

Unprocessed Bayer data are generated when bypassing the IFP completely—that is, by simply outputting the sensor Bayer stream as usual, using FRAME_VALID, LINE_VALID, and PIXCLK to time the data. This mode is called sensor bypass mode.

Output Ports

Composite Video Output

The composite video output DAC is external-resistor-programmable and supports both single-ended and differential output. The DAC is driven by the on-chip video encoder output.

Parallel Output

Parallel output uses either 8-bit or 10-bit output. Eight-bit output is used for ITU-R BT.656 and RGB output. Ten-bit output is used for raw Bayer output.

Zoom Support

The ASX340/MT9V139 supports zoom x1 and x2 modes, in interlaced and progressive scan modes. The progressive support is limited to the VGA at either 60 fps or 50 fps.

In the zoom x2 modes, the sensor is configured for QVGA (320 x 240), and the zoom x2 window can be configured to pan around the VGA window.

FOV Stretch Support

The ASX340/MT9V139 supports the ability to control the active 'width' of the TV output line, between 720 and 700 pixels. The hardware supports two margins, each a maximum of 10 pixels width, and has to be an even number of pixels.

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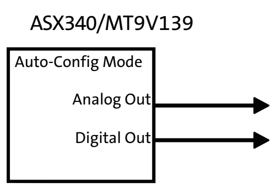
Usage Modes

How a camera based on the ASX340/MT9V139 will be configured depends on what features are used. In the simplest case, an ASX340/MT9V139 operating in Auto-Config Mode with no customized settings might be sufficient. Flash sizes vary depending on the data for registers, firmware, and overlay data—somewhere between 1KB to 16MB. The two-wire bus is adequate since only high-level commands are used to invoke overlays, load registers from memory, or set up lens correction parameters. Overlay data can alternatively be issued by the external µC if the rate of refreshing data is deemed adequate. If there are no commands in the EEPROM or Flash image the device can be in auto configuration mode by which the sensor is set up according to the status of pins FRAME_VALID, LINE_VALID, DOUT_LSB1, and DOUT_LSB0.

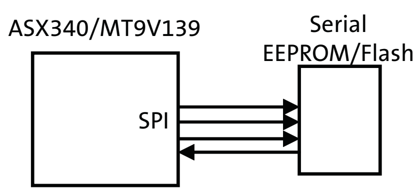
In the simplest case no EEPROM or Flash memory or µC is required, as shown in Figure 12. This is truly a single chip operation.

Figure 12: Auto-Config Mode



The ASX340/MT9V139 can be configured by a serial EEPROM or Flash through the SPI Interface.

Figure 13: Flash Mode



Functions such as overlay or 2x zoom can also be assigned to general purpose inputs. That capability can be employed on all configurations with external EEPROM or Flash memory by mapping overlay images to an input. Alternatively, the µC may poll these inputs to create an action such as a new overlay as shown in Figure 14.

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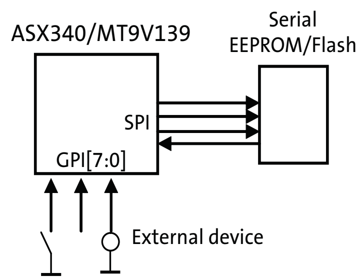
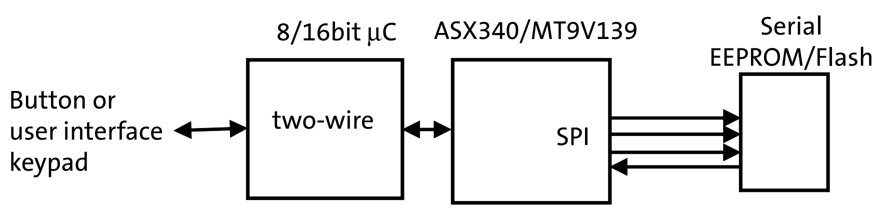
Figure 14: Usage Mode 3



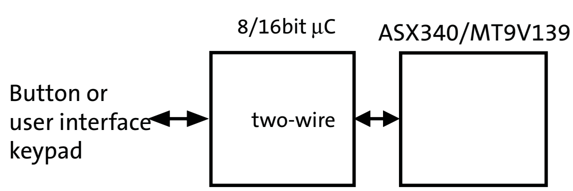
In some applications, button or user interface keypad can trigger overlay images being called by the µC as shown in Figure 15.

Figure 15: Host Mode with Flash



Overlay information may also be passed by the µC without a need for an EEPROM or Flash memory. However, because the data transfer rate is limited over the two-wire serial bus, the update rate may be slower. However, if overlay images are preloaded into the four on-chip buffers, they may be turned on and off or move location at the frame rate as shown in Figure 16.

Figure 16: Host Mode



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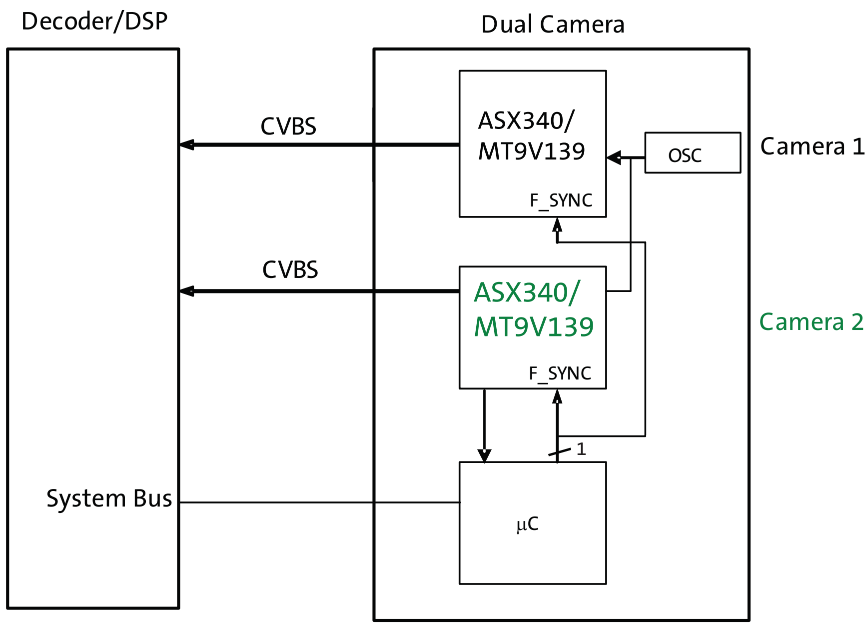
Multicamera Support

Two or more ASX340/MT9V139 sensors may be synchronized to a frame by asserting the FRAME_SYNC signal. At that point, the sensor and video encoder will reset without affecting any register settings. The ASX340/MT9V139 may be triggered to be synchronized with another ASX340/MT9V139 or an external event.

Figure 17: Multicamera System Block Diagram



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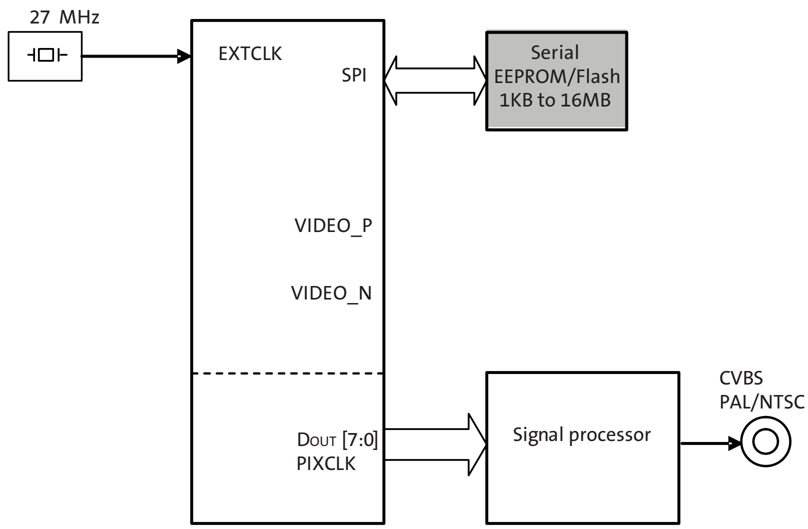
External Signal Processing

An external signal processor can take data from ITU656 or raw Bayer output format and post-process or compress the data in various formats.

Figure 18: External Signal Processing Block Diagram



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Device Configuration

After power is applied and the device is out of reset by de-asserting the RESET_BAR pin, it will enter a boot sequence to configure its operating mode. There are essentially three configuration modes: Flash/EEPROM Config, Auto Config, and Host Config. Figure 19: "Power-Up Sequence – Configuration Options Flow Chart," on page 32 contains more details on the configuration options.

The SOC firmware supports a System Configuration phase at start-up. This consists of five modes of execution:

1. Flash Detection
2. Flash-Config
3. Auto-Config
4. Host-Config
5. Change-Config (commences streaming - completes the System Configuration mode).

The System Configuration phase is entered immediately after the firmware initializes following SOC power-up or reset. By default, the firmware first enters the Flash Detection mode

The Flash Detection mode attempts to detect the presence of an SPI Flash or EEPROM device:

- If no device is detected, the firmware then samples the SPI_SDI pin state to determine the next mode:
  – If SPI_SDI == 0 then it enters the Host-Config mode.
  – If SPI_SDI == 1 then it enters the Auto-Config mode.
- If a device is detected, the firmware switches to the Flash-Config mode.

In the Flash-Config phase, the firmware interrogates the device to determine if it contains valid configuration records:

- If no records are detected, then the firmware enters the Auto-Config mode.
- If records are detected, the firmware processes them. By default, when all Flash records are processed the firmware switches to the Host-Config mode. However, the records encoded into the Flash can optionally be used to instruct the firmware to proceed to one of the other mode (auto-config/change-config).

The Auto-Config mode uses the FRAME_VALID, LINE_VALUE, DOUT_LSB0 and DOUT_LSB1 pins to configure the operation of the device, such as video format and pedestal (see Table 16, "GPIO Bit Descriptions," on page 33). After Auto-Config completes the firmware switches to the Change-Config mode.

In the Host-Config mode, the firmware performs no configuration, and remains idle waiting for configuration and commands from the host. The System Configuration phase is effectively complete and the SOC will take no actions until the host issues commands.

In the Change-Config mode, the firmware performs a 'Change-Config' operation. This applies the current configuration settings to the SOC, and commences streaming. This completes the System Configuration phase.

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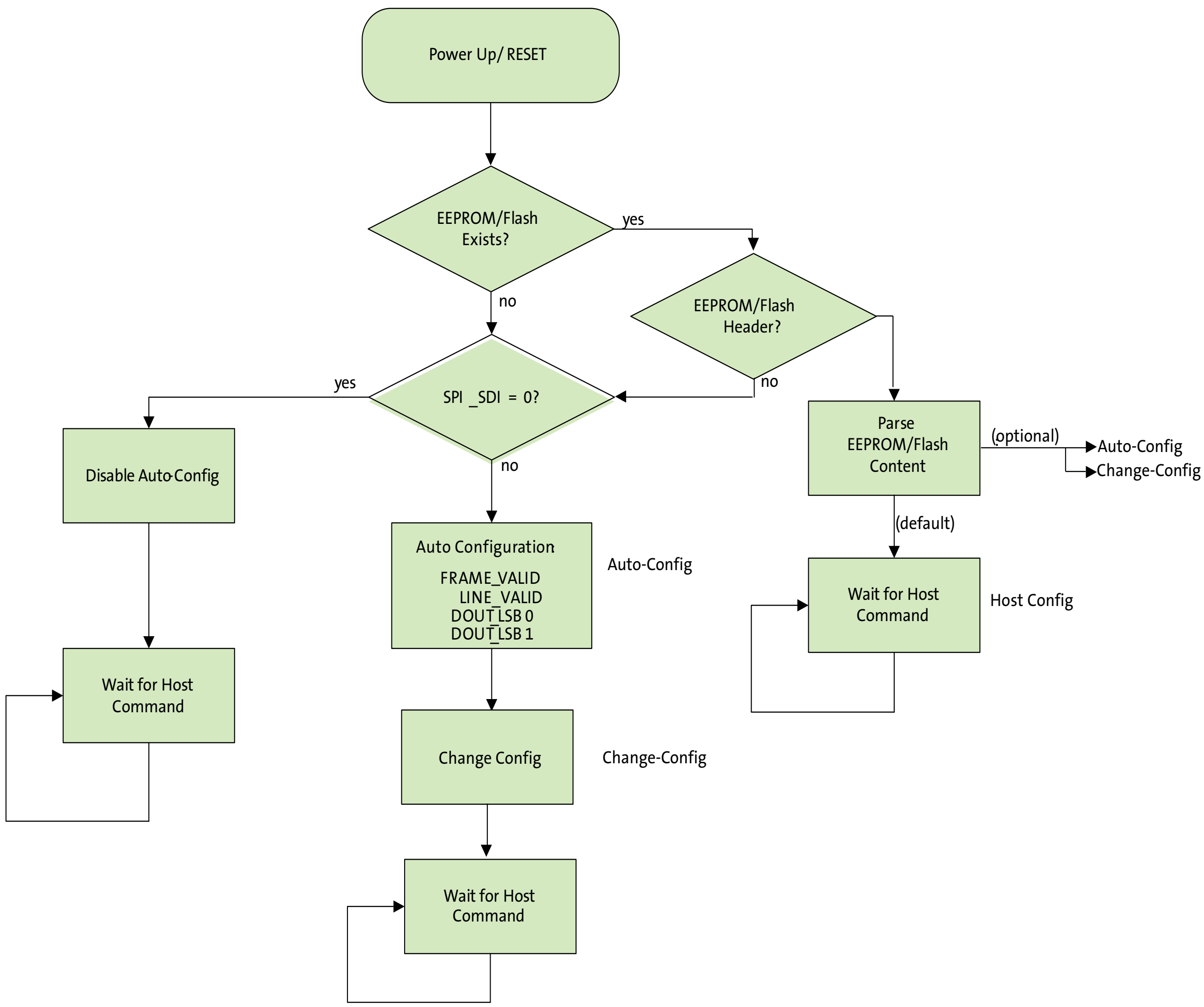
Power Sequence

In power-up, the core voltage (1.8V) must trail the IO (2.8V) by a positive number. All 2.8V rails can be turned on at the same time or follow the power-up sequence in Figure 45: "Power Up Sequence," on page 62.

In power down, the sequence is reversed. The core voltage (1.8V) must be turned off before any 2.8V. Refer to Figure 46: "Power Down Sequence," on page 63 for details.

Figure 19: Power-Up Sequence – Configuration Options Flow Chart



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Supported SPI Devices

Table 14 lists supported EEPROM/Flash devices. Devices not compatible will require a firmware patch. Contact Aptina for additional support.

Table 14: SPI Flash Devices

Type	Density	Manufacturer	Device	Speed (MHz)	Standard	Temp Range (°C)	Supported
Flash	1 MB	ST	M25P10-AVMB3	50		–40 to +125	Yes
Flash	8 MB	Atmel	AT26DF081A	70	JEDEC/Device ID	–20 to +85	Yes
EEPROM	1MB	ST	M95M01-R	5		–40 to +130	Yes
EEPROM	8KB	Microchip	25LC080	2		–40 to +125	Yes

Supported SPI Commands

The SPI commands shown in Table 15 are supported by the ASX340/MT9V139.

Table 15: SPI Commands Supported

Command	Value
Read Array	0x03
Block Erase	0xD8
Chip Erase	0xC7
Read Status	0x05
Write status	0x01
Byte Page Program	0x02
Write Enable	0x06
Write Disable	0x04
Read Manufacturer and Device ID	0x9F
(Fast) Read Array	0x0B

Table 16: GPIO Bit Descriptions

	GPIO[11] (DOUT_LSB1)	GPIO[10] (DOUT_LSB0)	GPIO[9] (FRAME_VALID)	GPI[8] (LINE_VALID)
Low (“0”)	Normal	NTSC	Normal	No pedestal
High (“1”)	Vertical Flip	PAL	Horizontal mirror	Pedestal

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Host Command Interface

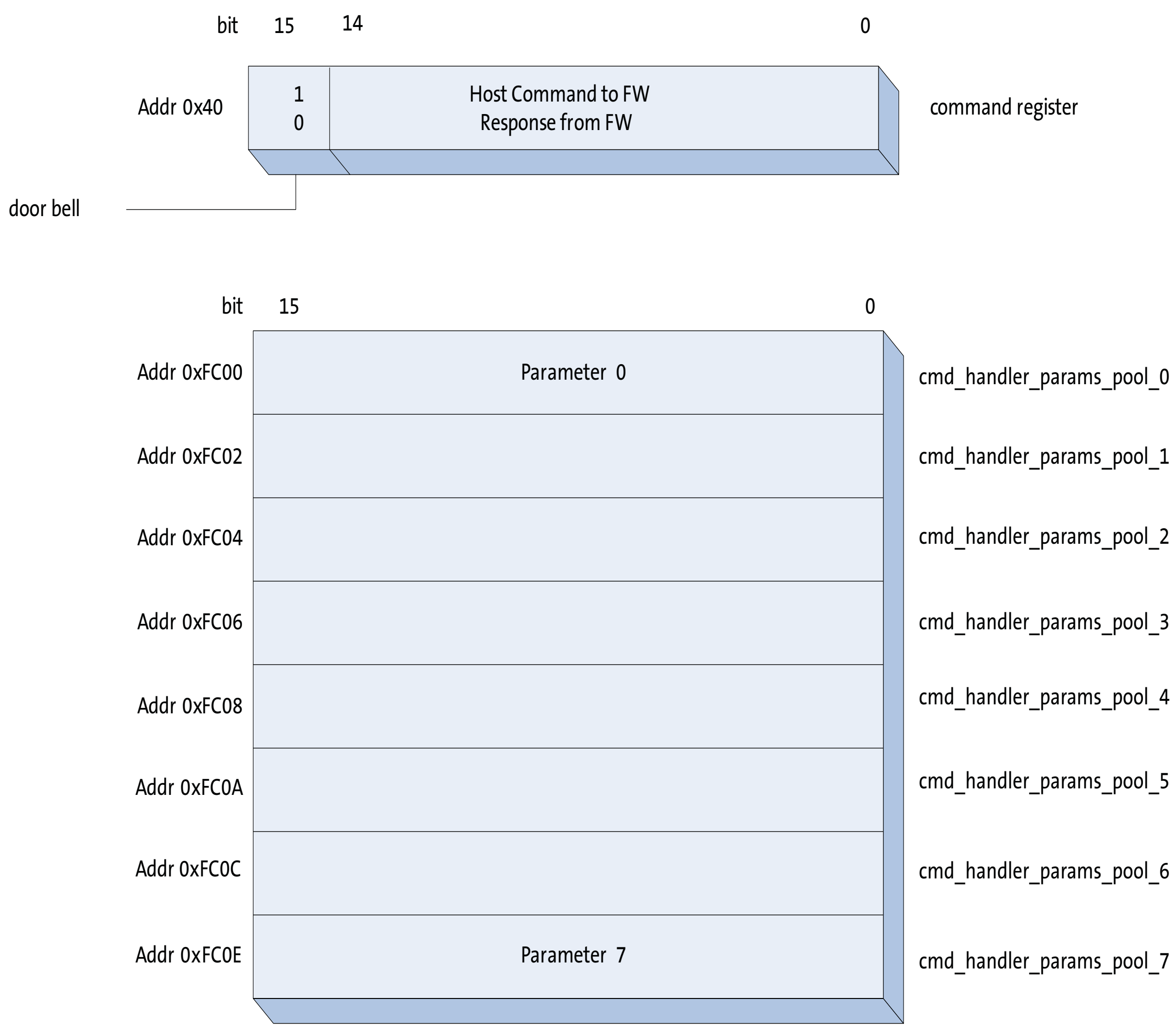
Aptina's sensors and SOCs contain numerous registers that are accessed through a two-wire interface with speeds up to 400 kHz.

The ASX340/MT9V139 in addition to writing or reading straight to/from registers or firmware variables, has a mechanism to write higher level commands, the Host Command Interface (HCI). Once a command has been written through the HCI, it will be executed by on chip firmware and the results are reported back. In general, registers shall not be accessed with the exception of registers that are marked for "User Access."

EEPROM or Flash memory is also available to store commands for later execution. Under DMA control, a command is written into the SOC and executed.

For a complete spec on host commands, refer to the ASX340/MT9V139 Host Command Interface Specification.

Figure 20: Interface Structure



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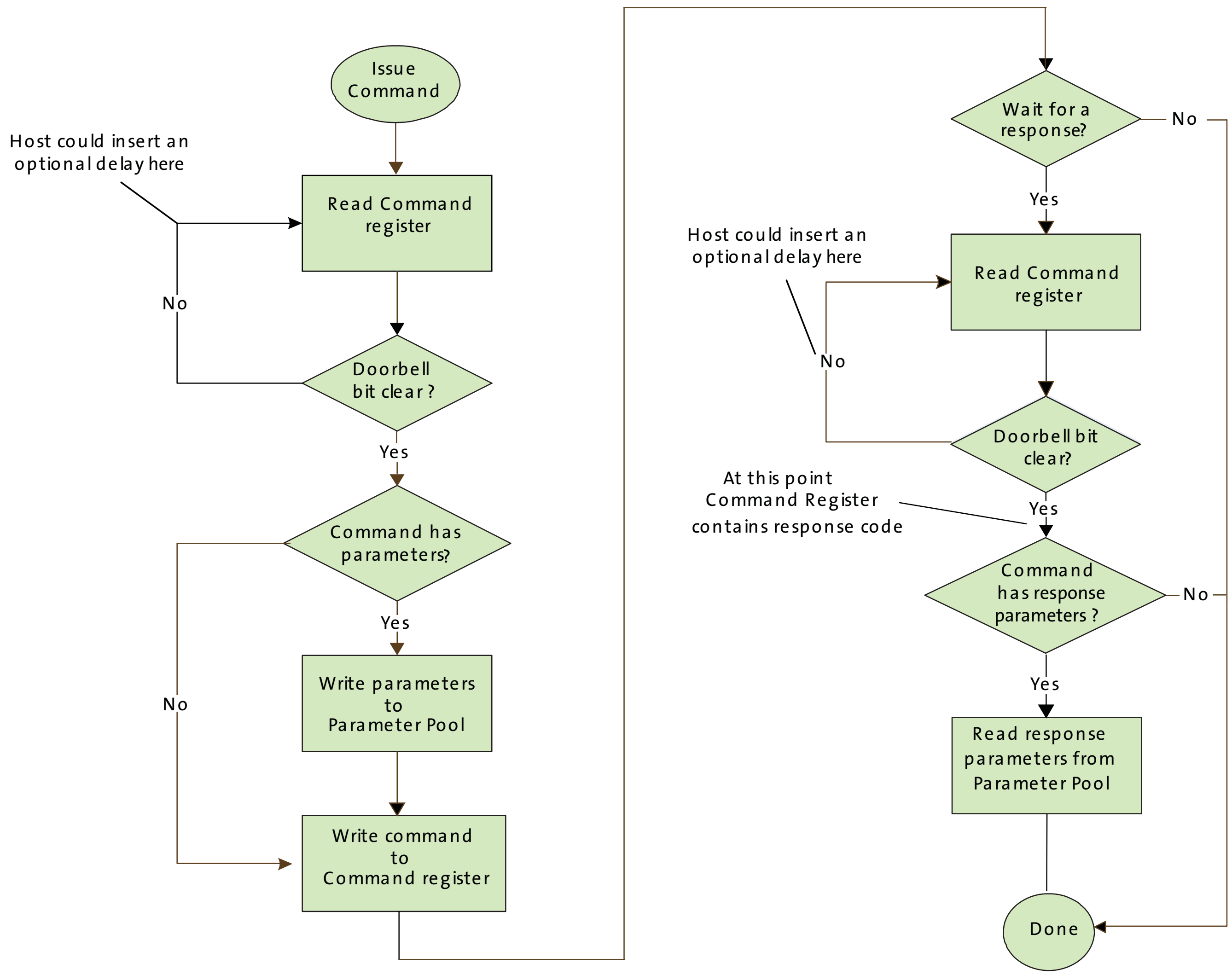
Host Command Process Flow



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Command Flow

The host issues a command by writing (through a two-wire interface bus) to the command register. All commands are encoded with bit 15 set, which automatically generates the host command (doorbell) interrupt to the microprocessor.

Assuming initial conditions, the host first writes the command parameters (if any) to the parameters pool (in the command handler's logical page), then writes the command to command register. The SOC firmware interrupt handler then signals the Command Handler task to process the command.

If the host wishes to determine the outcome of the command, it must poll the command register waiting for the doorbell bit to be cleared. This indicates that the firmware completed processing the command. When the doorbell bit is cleared, the contents of the command register indicate the command's result status. If the command generated response parameters, the host can now retrieve these from the parameters pool.

Note: The host must not write to the parameters pool, nor issue another command, until the previous command completes. This is true even if the host does not care about the result of the previous command. Therefore, the host must always poll the command register to determine the state of the doorbell bit, and ensure the bit is cleared before issuing a command.

For a complete command list and further information consult the Host Command Interface Specification.

An example of how (using DevWare) a command may be initiated in the form of a "Preset" follows.

Issue the SYSMGR_SET_STATE Command

All DevWare presets supplied by Aptina poll and test the doorbell bit after issuing the command. Therefore there is no need to check if the doorbell bit is clear before issuing the next command.

```
# Set the desired next state in the parameters
pool(SYS_STATE_ENTER_CONFIG_CHANGE)

REG= 0xFC00, 0x2800 // CMD_HANDLER_PARAMS_POOL_0


# Issue the HC_SYSMGR_SET_STATE command

REG= 0x0040, 0x8100 // COMMAND_REGISTER


# Wait for the FW to complete the command (clear the Doorbell bit)

POLL_FIELD= COMMAND_REGISTER, DOORBELL, !=0, DELAY=10, TIMEOUT=100


# Check the command was successful

ERROR_IF= COMMAND_REGISTER, HOST_COMMAND, !=0, "Set State command
failed",
```


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Summary of Host Commands

Table 17 on page 37 through Table 24 on page 39 show summaries of the host commands. The commands are divided into the following sections:

- System Manager
- Overlay
- GPIO
- Flash Manager
- Sequencer
- Patch Loader
- Miscellaneous
- Calibration Stats

Following is a summary of the Host Interface commands. The description gives a quick orientation. The “Type” column shows if it is an asynchronous or synchronous command. For a complete list of all commands including parameters, consult the Host Command Interface Specification document.

Table 17: System Manager Commands

System Manager Host Command	Value	Type	Description
Set State	0x8100	Synchronous	Request the system enter a new state
Get State	0x8101	Synchronous	Get the current state of the system

Table 18: Overlay Host Commands

Overlay Host Command	Value	Type	Description
Enable Overlay	0x8200	Synchronous	Enable or disable the overlay subsystem
Get Overlay State	0x8201	Synchronous	Retrieve the state of the overlay subsystem
Set Calibration	0x8202	Synchronous	Set the calibration offset
Set Bitmap Property	0x8203	Synchronous	Set a property of a bitmap
Get Bitmap Property	0x8204	Synchronous	Get a property of a bitmap
Set String Property	0x8205	Synchronous	Set a property of a character string
Load Buffer	0x8206	Asynchronous	Load an overlay buffer with a bitmap (from Flash)
Load Status	0x8207	Synchronous	Retrieve status of an active load buffer operation
Write Buffer	0x8208	Synchronous	Write directly to an overlay buffer
Read Buffer	0x8209	Synchronous	Read directly from an overlay buffer
Enable Layer	0x820A	Synchronous	Enable or disable an overlay layer
Get Layer Status	0x820B	Synchronous	Retrieve the status of an overlay layer
Set String	0x820C	Synchronous	Set the character string
Get String	0x820D	Synchronous	Get the current character string
Load String	0x820E	Asynchronous	Load a character string (from Flash)

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Table 19: GPIO Host Commands

GPIO Host Command	Value	Type	Description
Set GPIO Property	0x8400	Synchronous	Set a property of one or more GPIO pins
Get GPIO Property	0x8401	Synchronous	Retrieve a property of a GPIO pin
Set GPO State	0x8402	Synchronous	Set the state of a GPO pin or pins
Get GPIO State	0x8403	Synchronous	Get the state of a GPI pin or pins
Set GPI Association	0x8404	Synchronous	Associate a GPI pin state with a Command Sequence stored in SPI Flash
Get GPI Association	0x8405	Synchronous	Retrieve an GPIO pin association

Table 20: Flash Manager Host Commands

Flash Manager Host Command	Value	Type	Description
Get Lock	0x8500	Asynchronous	Request the Flash Manager access lock
Lock Status	0x8501	Synchronous	Retrieve the status of the access lock request
Release Lock	0x8502	Synchronous	Release the Flash Manager access lock
Config	0x8503	Synchronous	Configure the Flash Manager and underlying SPI Flash subsystem
Read	0x8504	Asynchronous	Read data from the SPI Flash
Write	0x8505	Asynchronous	Write data to the SPI Flash
Erase Block	0x8506	Asynchronous	Erase a block of data from the SPI Flash
Erase Device	0x8507	Asynchronous	Erase the SPI Flash device
Query Device	0x8508	Asynchronous	Query device-specific information
Status	0x8509	Synchronous	Obtain status of current asynchronous operation
Config Device	0x850A	Synchronous	Configure the attached SPI NVM device

Table 21: Sequencer Host Commands

Sequencer Host Command	Value	Type	Description
Refresh	0x8606	Synchronous	Refresh the automatic image processing algorithm configuration
Refresh Status	0x8607	Synchronous	Retrieve the status of the last Refresh operation

Table 22: Patch Loader Host Commands

Patch Loader Host Command	Value	Type	Description
Load Patch	0x8700	Asynchronous	Load a patch from SPI Flash and automatically apply
Status	0x8701	Synchronous	Get status of an active Load Patch or Apply Patch request
Apply Patch	0x8702	Asynchronous	Apply a patch (already located in Patch RAM)
Reserve RAM	0x8706	Synchronous	Reserve RAM to contain a patch

Table 23: Miscellaneous Host Commands

Miscellaneous Host Command	Value	Type	Description
Invoke Command Seq	0x8900	Synchronous	Invoke a sequence of commands stored in NVM
Config Command Seq Processor	0x8901	Synchronous	Configures the Command Sequencer processor
Wait For Event	0x8902	Synchronous	Wait for a system event to be signalled

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Table 24: Calibration Stats Host Commands

Calibration Stats Host Command	Value	Type	Description
Control	0x8B00	Asynchronous	Start statistics gathering
Read	0x8B01	Synchronous	Read the results back

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Slave Two-Wire Serial Interface

The two-wire serial interface bus enables read/write access to control and status registers within the ASX340/MT9V139. This interface is designed to be compatible with the MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) 1.0, which uses the electrical characteristics and transfer protocols of the two-wire serial interface specification.

The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and used to synchronize transfers.

Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD_IO off-chip by a pull-up resistor in the range of 1.5 to 4.7kΩ resistor.

Protocol

Data transfers on the two-wire serial interface bus are performed by a sequence of low-level protocol elements, as follows:

- a start or restart condition
- a slave address/data direction byte
- a 16-bit register address
- an acknowledge or a no-acknowledge bit
- data bytes
- a stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

The SADDR pin is used to select between two different addresses in case of conflict with another device. If SADDR is LOW, the slave address is 0x90; if SADDR is HIGH, the slave address is 0xBA. See Table 25 below.

Table 25: Two-Wire Interface ID Address Switching

SADDR	Two-Wire Interface Address ID
0	0x90
1	0xBA

Start Condition

A start condition is defined as a HIGH-to-LOW transition on SDATA while SCLK is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a “repeated start” or “restart” condition.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no-acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is low and must be stable while SCLK is HIGH.

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Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A "0" in bit [0] indicates a write, and a "1" indicates a read. The default slave addresses used by the ASX340/MT9V139 are 0x90 (write address) and 0x91 (read address). Alternate slave addresses of 0xBA (write address) and 0xBB (read address) can be selected by asserting the SADDR input signal.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data. The protocol used is outside the scope of the two-wire serial interface specification.

Acknowledge Bit

Each 8-bit data transfer is followed by an acknowledge bit or a no-acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

No-Acknowledge Bit

The no-acknowledge bit is generated when the receiver does not drive SDATA low during the SCLK clock period following a data transfer. A no-acknowledge bit is used to terminate a read sequence.

Stop Condition

A stop condition is defined as a LOW-to-HIGH transition on SDATA while SCLK is HIGH.

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Typical Operation

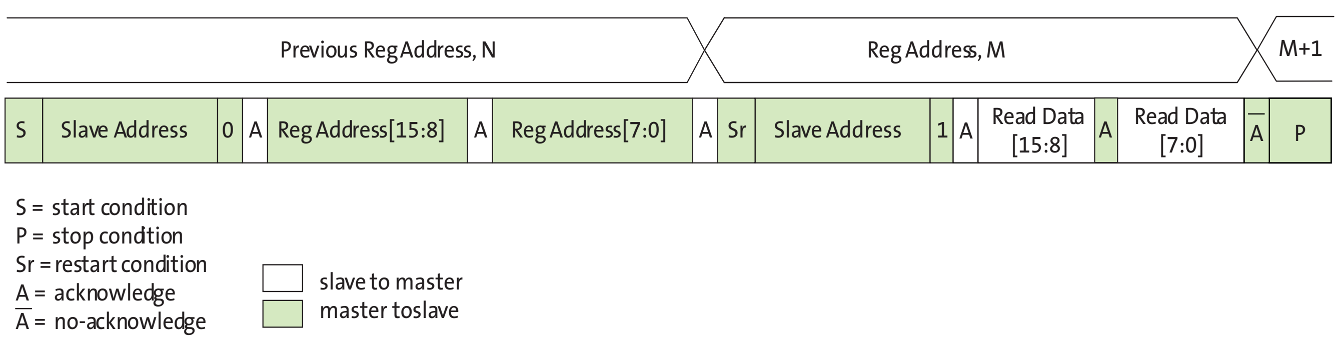
A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8-bit slave address/data direction byte. The last bit indicates whether the request is for a READ or a WRITE, where a “0” indicates a WRITE and a “1” indicates a READ. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16-bit register address to which a WRITE will take place. This transfer takes place as two 8-bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master will then transfer the 16-bit data, as two 8-bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master stops writing by generating a (re)start or stop condition. If the request was a READ, the master sends the 8-bit write slave address/data direction byte and 16-bit register address, just as in the write request. The master then generates a (re)start condition and the 8-bit read slave address/data direction byte, and clocks out the register data, 8 bits at a time. The master generates an acknowledge bit after each 8-bit transfer. The data transfer is stopped when the master sends a no-acknowledge bit.

Single READ from Random Location

Figure 21 shows the typical READ cycle of the host to the ASX340/MT9V139. The first two bytes sent by the host are an internal 16-bit register address. The following 2-byte READ cycle sends the contents of the registers to host.

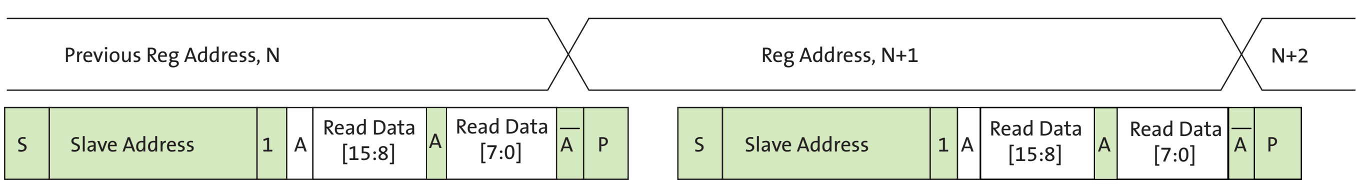
Figure 21: Single READ from Random Location



Single READ from Current Location

Figure 22 shows the single READ cycle without writing the address. The internal address will use the previous address value written to the register.

Figure 22: Single Read from Current Location



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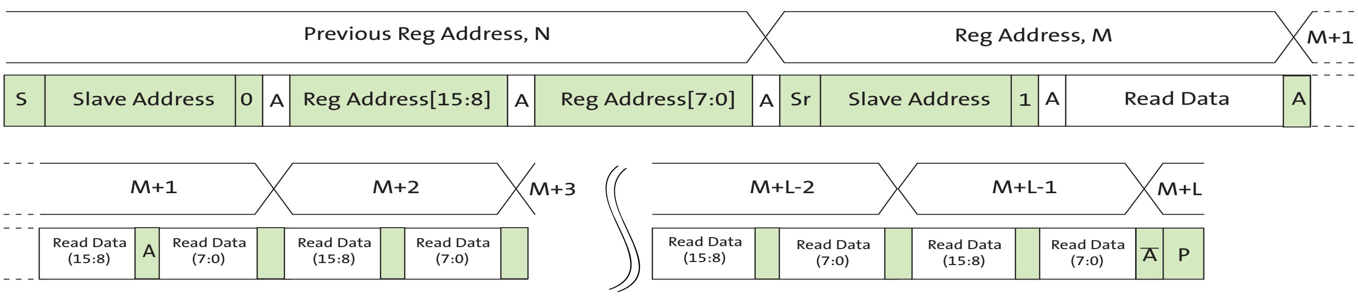
Sequential READ, Start from Random Location

This sequence (Figure 23) starts in the same way as the single READ from random location (Figure 21 on page 42). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until "L" bytes have been read.

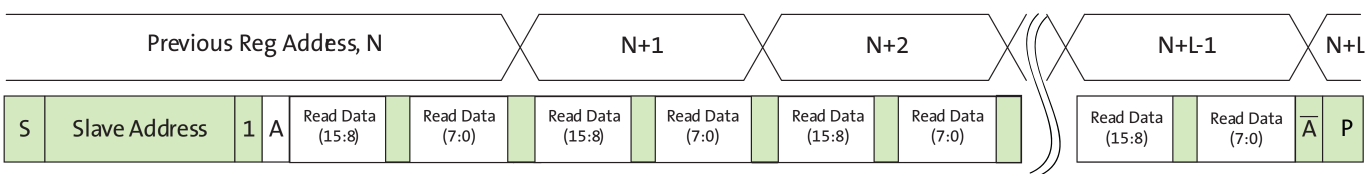
Figure 23: Sequential READ, Start from Random Location



Sequential READ, Start from Current Location

This sequence (Figure 24) starts in the same way as the single READ from current location (Figure 22). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte reads until "L" bytes have been read.

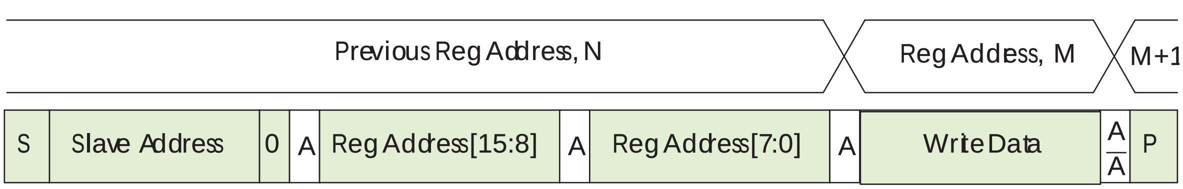
Figure 24: Sequential READ, Start from Current Location



Single Write to Random Location

Figure 25 shows the typical WRITE cycle from the host to the ASX340/MT9V139.The first 2 bytes indicate a 16-bit address of the internal registers with most-significant byte first. The following 2 bytes indicate the 16-bit data.

Figure 25: Single WRITE to Random Location



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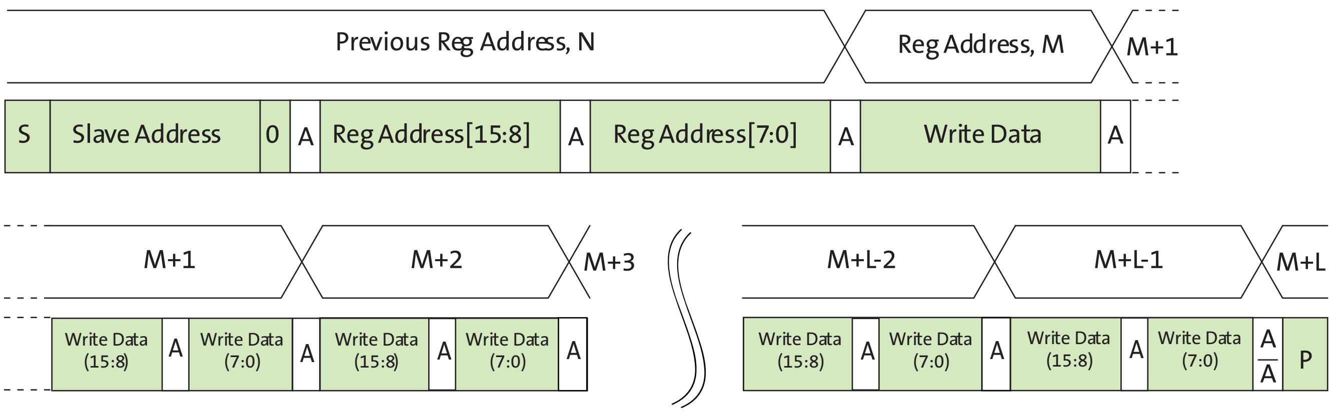
Sequential WRITE, Start at Random Location

This sequence (Figure 26) starts in the same way as the single WRITE to random location (Figure 25). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte writes until "L" bytes have been written. The WRITE is terminated by the master generating a stop condition.

Figure 26: Sequential WRITE, Start at Random Location



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Overlay Capability

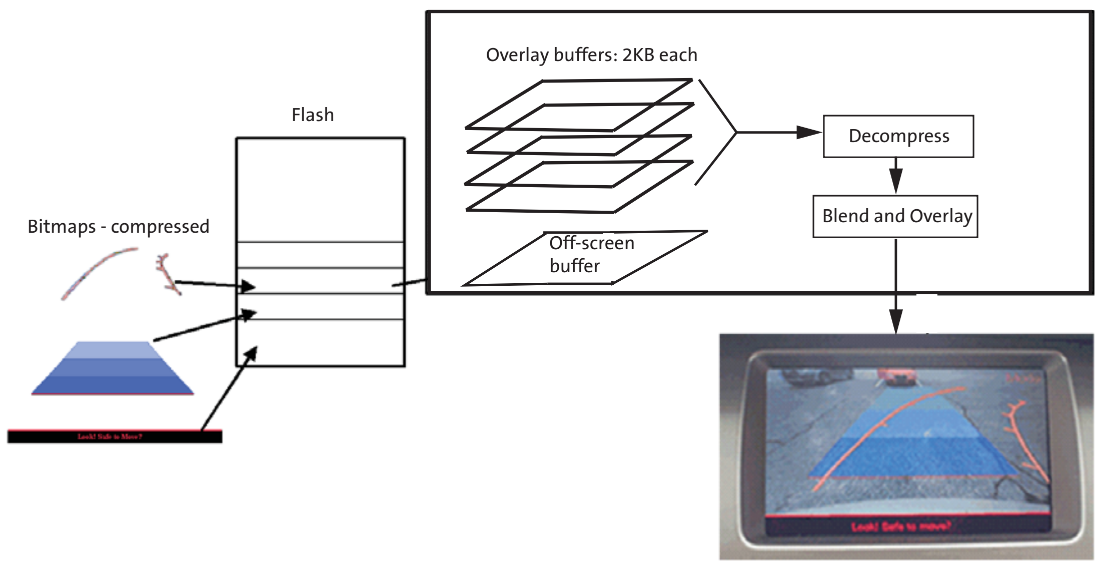
Figure 27 highlights the graphical overlay data flow of theASX340/MT9V139. The images are separated to fit into 2KB blocks of memory after compression.

- Up to four overlays may be blended simultaneously
- Overlay size 360 x 480 pixels rendered into a display area of 720 x 480 pixels (NTSC) or 720 x 576 (PAL)
- Selectable readout: rotating order is user programmable
- Dynamic movement through predefined overlay images
- Palette of 32 colors out of 64,000 with eight colors per bitmap
- Blend factors may be changed dynamically to achieve smooth transitions

The host commands allow a bitmap to be written piecemeal to a memory buffer through the I^2C, and also through DMA direct from SPI Flash memory. Multiple encoding passes may be required to fit an image into a 2KB block of memory; alternatively, the image can be divided into two or more blocks to make the image fit. Every graphic image may be positioned in an x/y direction and overlap with other graphic images.

The host may load an image at any time. Under control of DMA assist, data are transferred to the off-screen buffer in compressed form. This assures that no display data are corrupted during the replenishment of the four active overlay buffers.

Figure 27: Overlay Data Flow



Note: These images are not actually rendered, but show conceptual objects and object blending.

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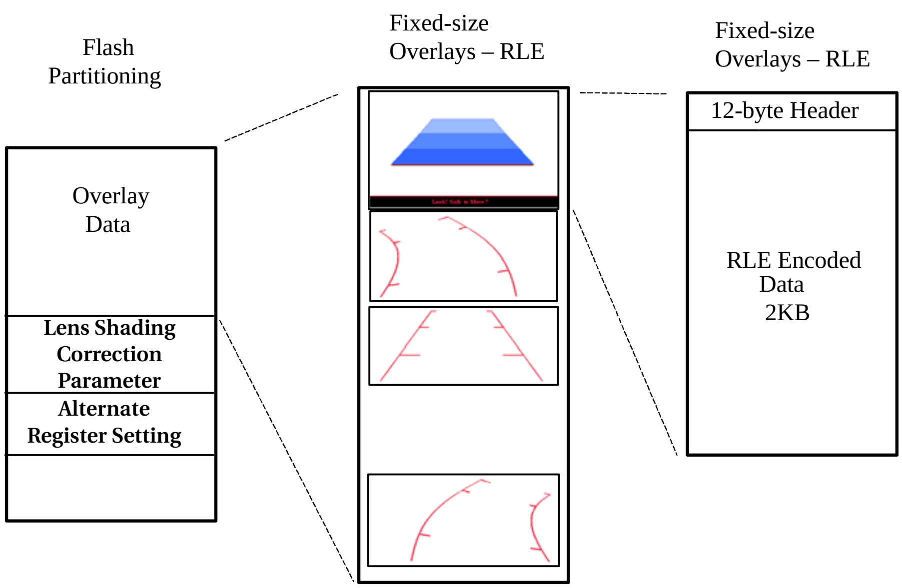
Serial Memory Partition

The contents of the Flash/EEPROM memory partition logically into three blocks (see Figure 28):

- Memory for overlay data and descriptors
- Memory for register settings, which may be loaded at boot-up
- Firmware extensions or software patches; in addition to the on-chip firmware, extensions reside in this block of memory

These blocks are not necessarily contiguous.

Figure 28: Memory Partitioning



External Memory Speed Requirement

For a 2KB block of overlay to be transferred within a frame time to achieve maximum update rate, the serial memory has to be a certain speed.

Table 26: Transfer Time Estimate

Frame Time	SPI Clock	Transfer Time to 2KB
33.3ms	4.5 MHz	1ms

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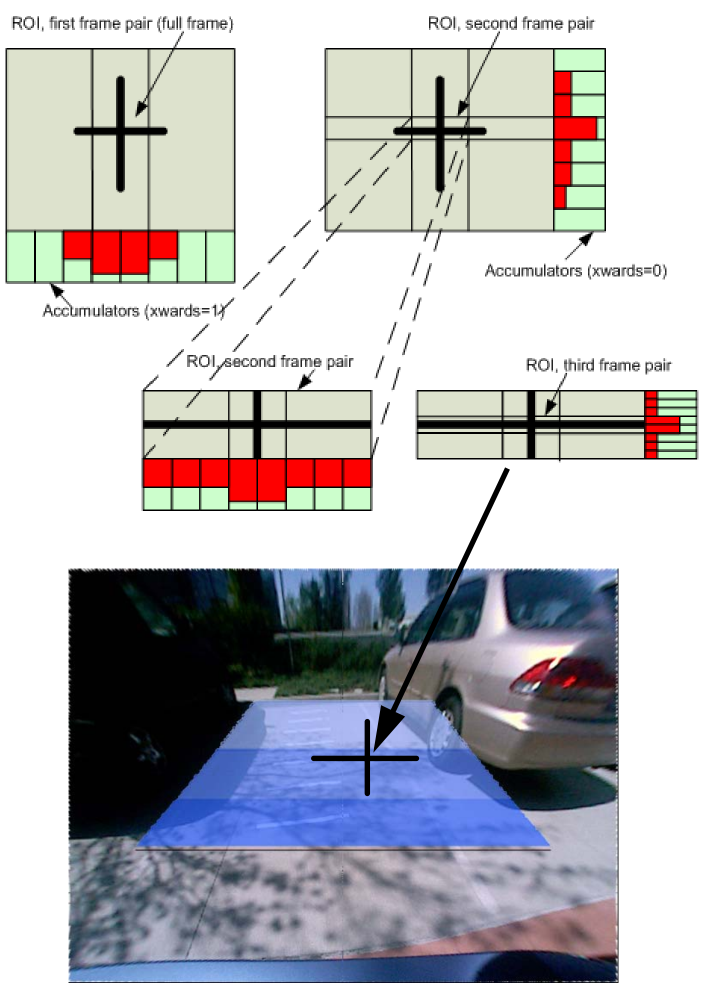
Overlay Adjustment

To ensure a correct position of the overlay to compensate for assembly deviation, the overlay can be adjusted with assistance from the overlay statistics engine:

- The overlay statistics engine supports a windowed 8-bin luma histogram, either row-wise (vertical) or column-wise (horizontal).
- The example calibration statistics can be used to perform an automatic successive-approximation search of a cross-hair target within the scene.
- On the first frame, the firmware performs a coarse horizontal search, followed by a coarse vertical search in the second frame.
- In subsequent frames, the firmware reduces the region-of-interest of the search to the histogram bins containing the greatest accumulator values, thereby refining the search.
- The resultant X, Y location of the cross-hair target can be used to assign a calibration value of offset selected overlay graphic image positions within the output image.
- The calibration statistics patch also supports a manual mode, which allows the host to access the raw accumulator values directly.

Figure 29: Overlay Calibration



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The position of the target will be used to determine the calibration value that shifts the X,Y position of adjustable overlay graphics.

The overlay calibration is intended to be applied on a device by device basis “in system,” which means after the camera has been installed. Aptina provides basic programming scripts that may reside in the SPI Flash memory to assist in this effort.

Overlay Character Generator

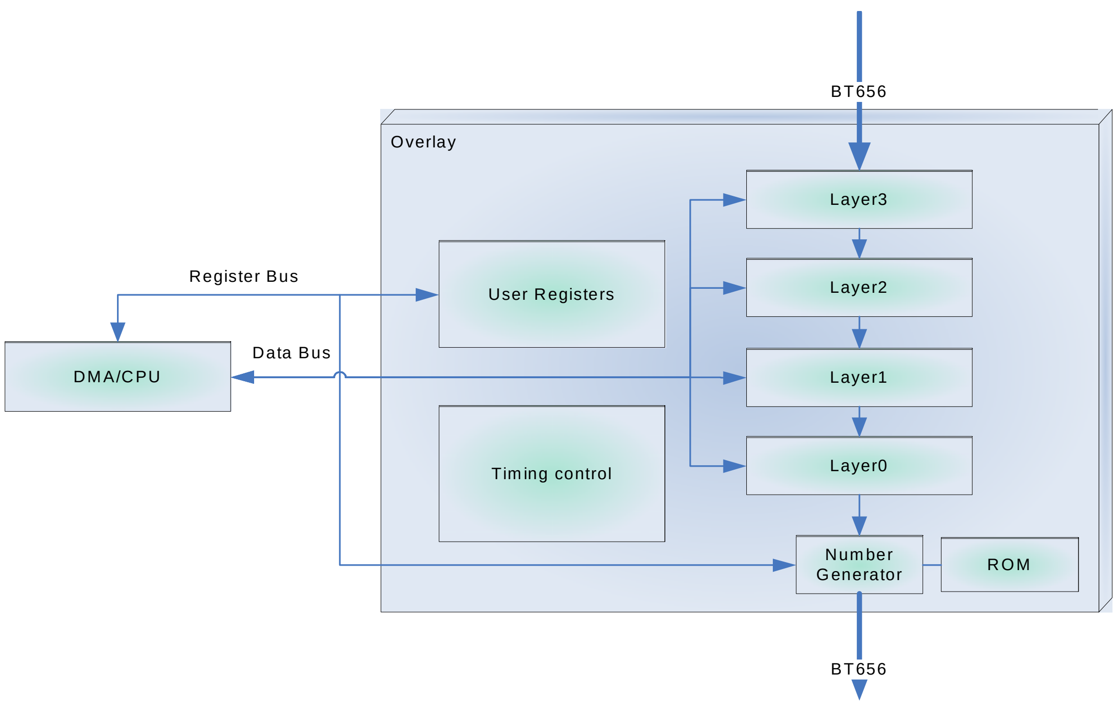
In addition to the four overlay layers, a fifth layer exists for a character generator overlay string.

There are a total of:

- 16 alphanumeric characters available
- 22 characters maximum per line
- 16 x 32 pixels with 1-bit color depth

Any update to the character generator string requires the string to be passed in its entirety with the Host Command. Character strings have their own control properties aside from the Overlay bitmap properties.

Figure 30: Internal Block Diagram Overlay



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Character Generator

The character generator can be seen as the fifth top layer, but instead of getting the source from RLE data in the memory buffers, it has a predefined 16 characters stored in ROM.

All the characters are 1-bit depth color and are sharing the same YCbCr look up table.

Figure 31: Example of Character Descriptor 0 Stored in ROM

ROM	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x02	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0x06	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0
0x08	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
0x0a	0	0	0	1	1	1	1	0	0	1	1	1	1	0	0	0
0x0c	0	0	0	1	1	1	0	0	0	0	1	1	1	1	0	0
0x0e	0	0	1	1	1	1	0	0	0	0	0	1	1	1	0	0
0x10	0	0	1	1	1	0	0	0	0	0	0	1	1	1	0	0
0x12	0	0	1	1	1	0	0	0	0	0	0	1	1	1	1	0
0x14	0	1	1	1	1	0	0	0	0	0	0	0	1	1	1	0
0x16	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x18	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x1a	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x1c	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x1e	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x20	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x22	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x24	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x26	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x28	0	0	1	1	1	0	0	0	0	0	0	0	1	1	1	0
0x2a	0	0	1	1	1	0	0	0	0	0	0	1	1	1	1	0
0x2c	0	0	1	1	1	0	0	0	0	0	0	1	1	1	0	0
0x2e	0	0	1	1	1	1	0	0	0	0	0	1	1	1	0	0
0x30	0	0	0	1	1	1	0	0	0	0	1	1	1	0	0	0
0x32	0	0	0	1	1	1	1	0	0	1	1	1	1	0	0	0
0x34	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
0x36	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0
0x38	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0x3a	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3c	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3e	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
…																

It can show a row of up to 22 characters of 16 x 32 pixels resolution (32 x 32 pixels when blended with the BT 656 data).

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Character Generator Details

Table 27 shows the characters that can be generated.

Table 27: Character Generator Details

Item	Quantity	Description
16-bit character	22	Coder for one of these characters: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, /, (space), :, –, (comma), (period)
1 bpp color	1	Depth of the bit map is 1 bpp

It is the responsibility of the user to set up proper values in the character positioning to fit them in the same row (that is one of the reasons that 22 is the maximum number of characters).

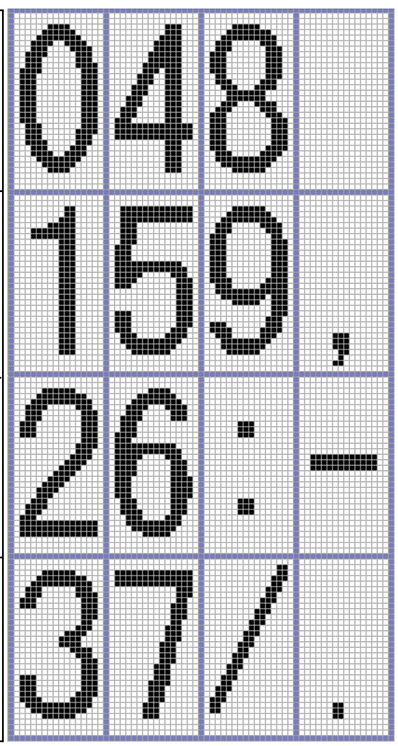
Note: No error is generated if the character row overruns the horizontal or vertical limits of the frame.

Full Character Set for Overlay

Figure 32 shows all of the characters that can be generated by theASX340/MT9V139.

Figure 32: Full Character Set for Overlay

0x0	0x4	0x8	0xC
0x1	0x5	0x9	0xD
0x2	0x6	0xA	0xE
0x3	0x7	0xB	0xF



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Modes and Timing

This section provides an overview of the typical usage modes and related timing information for theASX340/MT9V139.

Composite Video Output

The external pin DOUT_LSB0 can be used to configure the device for default NTSC or PAL operation (auto-config mode). This and other video configuration settings are available as register settings accessible through the serial interface.

NTSC

Both differential and single-ended connections of the full NTSC format are supported. The differential connection that uses two output lines is used for low noise or long distance applications. The single-ended connection is used for PCB tracks and screened cable where noise is not a concern. The NTSC format has three black lines at the bottom of each image for padding (which most LCDs do not display).

PAL

The PAL format is supported with 576 active image rows.

Single-Ended and Differential Composite Output

The composite output can be operated in a single-ended or differential mode by simply changing the external resistor configuration. For single-ended termination, see Figure 33 on page 51. The differential schematic is shown in Figure 34 on page 52.

Figure 33: Single-Ended Termination

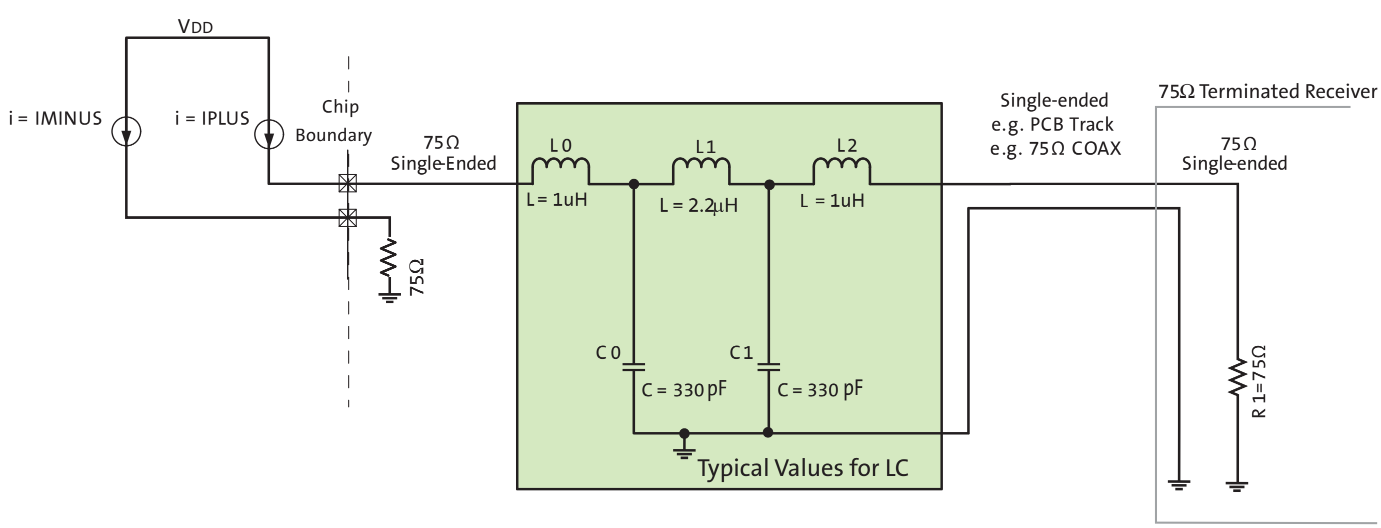

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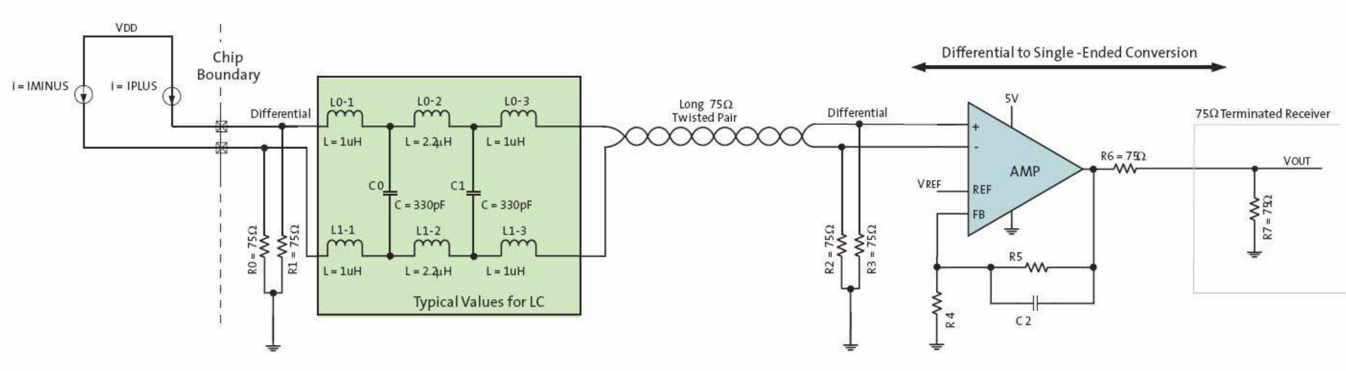
Figure 34: Differential Connection—Grounded Termination



Parallel Output (DOUT)

The DOUT[7:0] port supports both progressive and Interlaced mode. Progressive mode (with FV and LV signal) include raw bayer(8 or 10 bit), YCbCr, RGB. Interlaced mode is CCIR656 compliant.

Figure 35 shows the data that is output on the parallel port for CCIR656. Both NTSC and PAL formats are displayed. The blue values in Figure 35 represent NTSC (525/60). The red values represent PAL (625/50).

Figure 35: CCIR656 8-Bit Parallel Interface Format for 525/60 (625/50) Video Systems

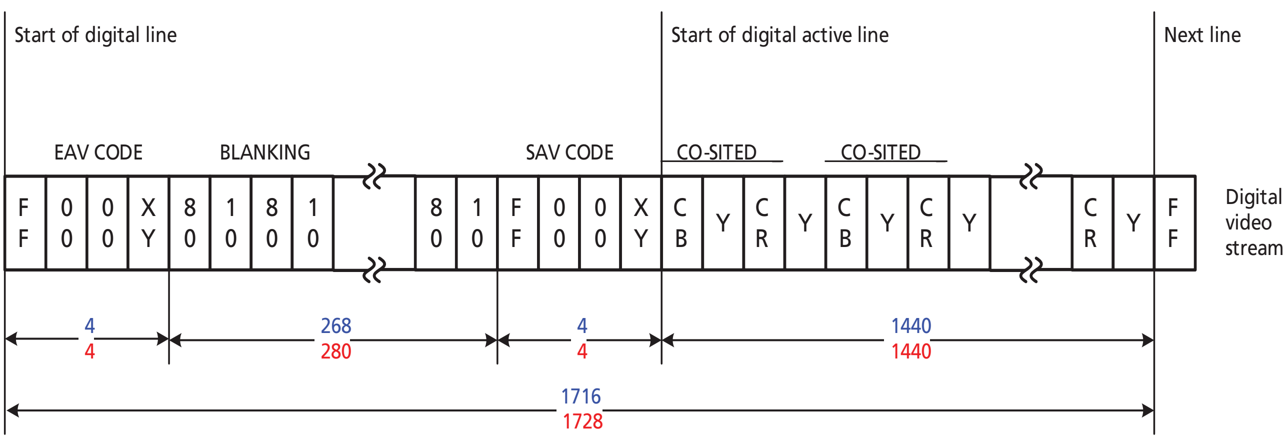


Figure 36 on page 53 shows detailed vertical blanking information for NTSC timing. See Table 28 on page 53 for data on field, vertical blanking, EAV, and SAV states.

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Figure 36: Typical CCIR656 Vertical Blanking Intervals for 525/60 Video System

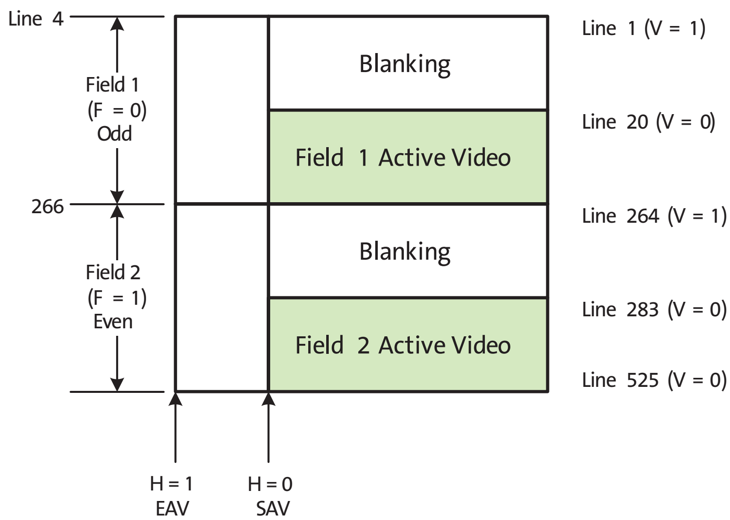

Table 28: Field, Vertical Blanking, EAV, and SAV States 525/60 Video System

Line Number	F	V	H (EAV)	H (SAV)
1–3	1	1	1	0
4–9	0	1	1	0
20–263	0	0	1	0
264–265	0	1	1	0
266–282	1	1	1	0
283–525	1	0	1	0

Figure 37 shows detailed vertical blanking information for PAL timing. See Table 29 on page 54 for data on field, vertical blanking, EAV, and SAV states.

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Figure 37: Typical CCIR656 Vertical Blanking Intervals for 625/50 Video System

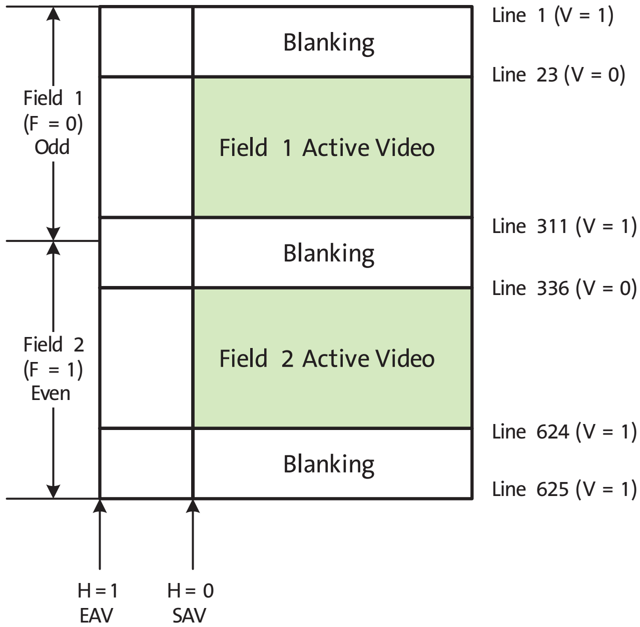

Table 29: Field, Vertical Blanking, EAV, and SAV States for 625/50 Video System

Line Number	F	V	H (EAV)	H (SAV)
1–22	0	1	1	0
23–310	0	0	1	0
311–312	0	1	1	0
313–335	1	1	1	0
336–623	1	0	1	0
624–625	1	1	1	0

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Reset and Clocks

Reset

Power-up reset is asserted or de-asserted with the RESET_BAR pin, which is active LOW. In the reset state, all control registers are set to default values. See "Device Configuration" on page 31 for more details on Auto, Host, and Flash configurations.

Soft reset is asserted or de-asserted by the two-wire serial interface program. In soft-reset mode, the two-wire serial interface and the register bus are still running. All control registers are reset using default values.

Clocks

The ASX340/MT9V139 has two primary clocks:

- A master clock coming from the EXTCLK signal.
- In default mode, a pixel clock (PIXCLK) running at 2 * EXTCLK. In raw Bayer bypass mode, PIXCLK runs at the same frequency as EXTCLK.

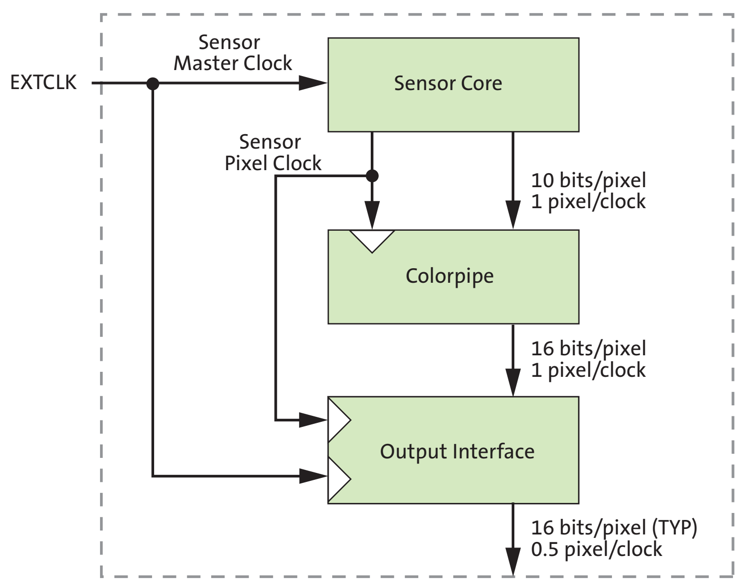
When the ASX340/MT9V139 operates in sensor stand-alone mode, the image flow pipeline clocks can be shut off to conserve power.

The sensor core is a master in the system. The sensor core frame rate defines the overall image flow pipeline frame rate. Horizontal blanking and vertical blanking are influenced by the sensor configuration, and are also a function of certain image flow pipeline functions. The relationship of the primary clocks is depicted in Figure 38.

The image flow pipeline typically generates up to 16 bits per pixel—for example, YCbCr or 565RGB—but has only an 8-bit port through which to communicate this pixel data.

To generate NTSC or PAL format images, the sensor core requires a 27 MHz clock.

Figure 38: Primary Clock Relationships



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Floating Inputs

The following ASX340/MT9V139 pins cannot be floated:

- SDATA–This pin is bidirectional and should not be floated
- FRAME_SYNC
- TRST_N
- SCLK
- SADDR
- ATEST1
- ATEST2

Output Data Ordering

Table 30: Output Data Ordering in DOUT RGB Mode

Mode (Swap Disabled)	Byte	D7	D6	D5	D4	D3	D2	D1	D0
565RGB	First	R7	R6	R5	R4	R3	G7	G6	G5
	Second	G4	G3	G2	B7	B6	B5	B4	B3
555RGB	First	0	R7	R6	R5	R4	R3	G7	G6
	Second	G5	G4	G3	B7	B6	B5	B4	B3
444xRGB	First	R7	R6	R5	R4	G7	G6	G5	G4
	Second	B7	B6	B5	B4	0	0	0	0
x444RGB	First	0	0	0	0	R7	R6	R5	R4
	Second	G7	G6	G5	G4	B7	B6	B5	B4

Note: PIXCLK is 54 MHz when EXTCLK is 27 MHz.

Table 31: Output Data Ordering in Sensor Stand-Alone Mode

Mode	D7	D6	D5	D4	D3	D2	D1	D0	DOUT_LSB1	DOUT_LSB0
10-bit Output	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

Note: PIXCLK is 27 MHz when EXTCLK is 27 MHz.

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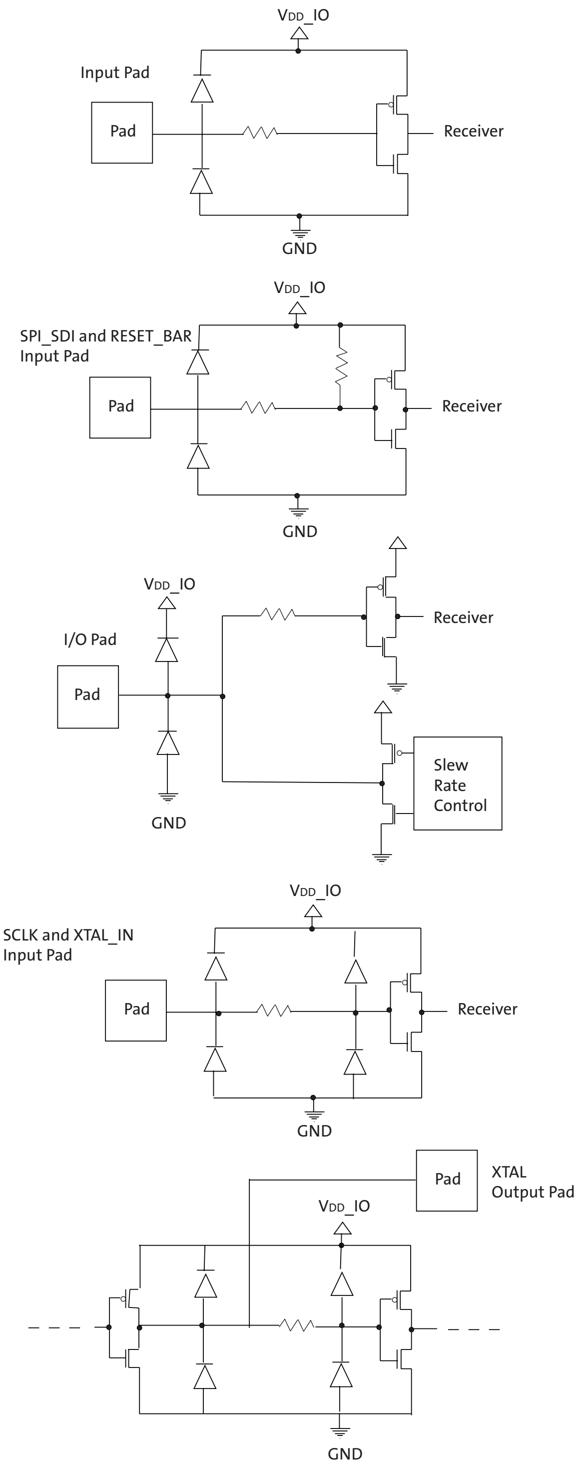
I/O Circuitry

Figure 39 illustrates typical circuitry used for each input, output, or I/O pad.

Figure 39: Typical I/O Equivalent Circuits



Note: All I/O circuitry shown above is for reference only. The actual implementation may be different.

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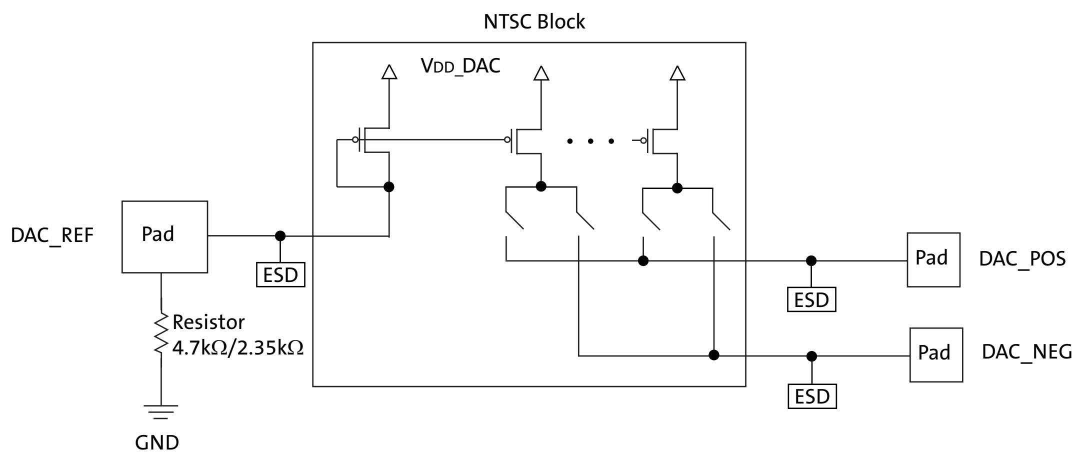
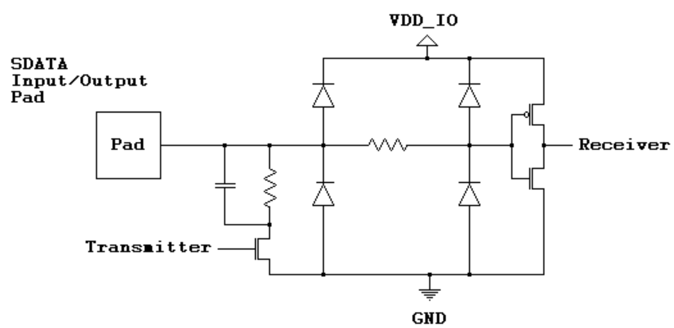
Figure 40: NTSC Block



Note: All I/O circuitry shown above is for reference only. The actual implementation may be different.

Figure 41: Serial Interface



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I/O Timing

Digital Output

By default, the ASX340/MT9V139 launches pixel data, FV, and LV synchronously with the falling edge of PIXCLK. The expectation is that the user captures data, FV, and LV using the rising edge of PIXCLK. The timing diagram is shown in Figure 42.

As an option, the polarity of the PIXCLK can be inverted from the default by programming R0x0016[14].

Figure 42: Digital Output I/O Timing

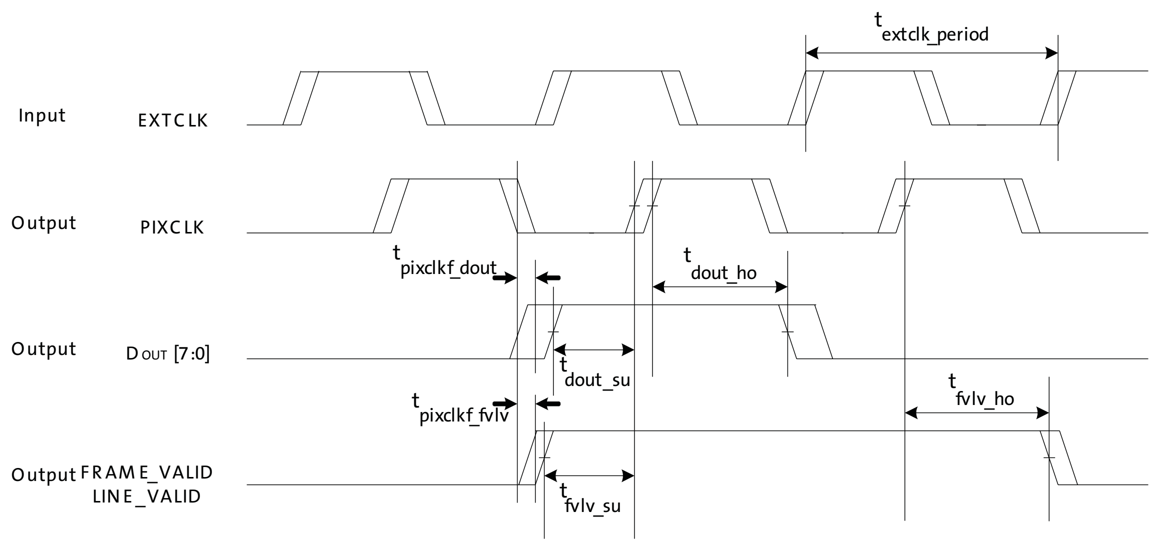

Table 32: Parallel Digital Output I/O Timing

f_{EXTCLK} = 27 MHz; VDD = 1.8V; VDD_IO = 2.8V; VAA = 2.8V; VAA_PIX = 2.8V; VDD_PLL = 2.8V; VDD_DAC = 2.8V; Default slew rate

Signal	Parameter	Conditions	Min	Typ	Max	Unit
EXTCLK	f_{extclk}	max ±100 ppm	6	27	54	MHz
	t_{extclk_period}		18.52	37	166.67	ns
	Duty cycle		45	50	55	%
PIXCLK[1]	f_{pixclk}		6	27	54	MHz
	t_{pixclk_period}		18.52	37.04	166.67	ns
	Duty cycle		45	50	55	%
DATA[7:0]	$t_{pixclkf\_dout}$		0.97	–	2.42	ns
	t_{dout_su}		6.83	–	8.28	ns
	t_{dout_ho}		2.74	–	6.32	ns
FV/LV	$t_{pixclkf\_fvlv}$		1.15	–	2.53	ns
	t_{fvlv_su}		6.72	–	8.1	ns
	t_{fvlv_ho}		5.74	–	7.62	ns

Note: PIXCLK can be inverted from the default by programming R0x0016[14].

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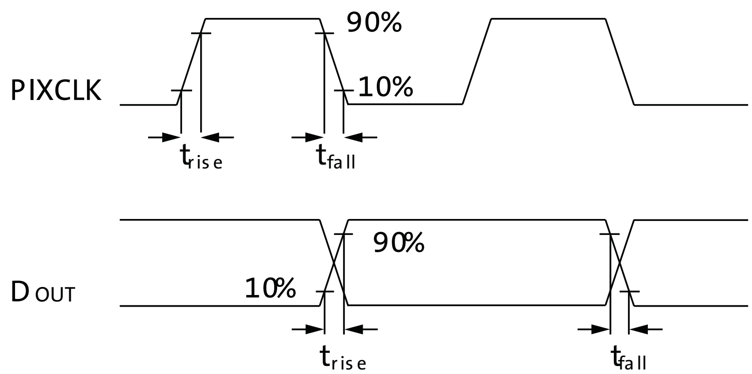
Slew Rate

Table 33: Slew Rate for PIXCLK and DOUT

f_{EXTCLK} = 27 MHz; VDD = 1.8V; VDD_IO = 2.8V; VAA = 2.8V; VAA_PIX = 2.8V;
VDD_PLL = 2.8V; VDD_DAC = 2.8V; T = 25°C; CLOAD = 40 pF

PIXCLK			DOUT[7:0]			
R0x30 [10:8]	Typical Rise Time	Typical Fall Time	R0x30 [2:0]	Typical Rise Time	Typical Fall Time	Unit
000	6.5	6.3	000	6.5	6.3	ns
001	4.8	4.6	001	4.8	4.6	ns
010	3.9	3.8	010	3.9	3.8	ns
011	3.7	3.7	011	3.7	3.7	ns
100	3.6	3.6	100	3.6	3.6	ns
101	3.5	3.5	101	3.5	3.5	ns
110	3.4	3.4	110	3.4	3.4	ns
111	3.3	3.3	111	3.3	3.3	ns

Figure 43: Slew Rate Timing



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Configuration Timing

During start-up, the Dout_LSB0, LV and FV are sampled. Setup and hold timing for the RESET_BAR signal with respect to DOUT_LSB0, LV, and FV are shown in Figure 44 and Table 34. These signals are sampled once by the on-chip firmware, which yields a long ^{t}Hold time.

Figure 44: Configuration Timing

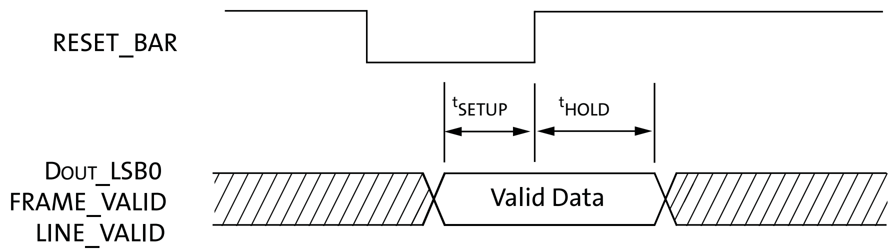

Table 34: Configuration Timing

Signal	Parameter	Min	Typ	Max	Unit
DOUT_LSB0, FRAME_VALID, LINE_VALID	^{t}SETUP	0			µs
	^{t}HOLD	50			µs

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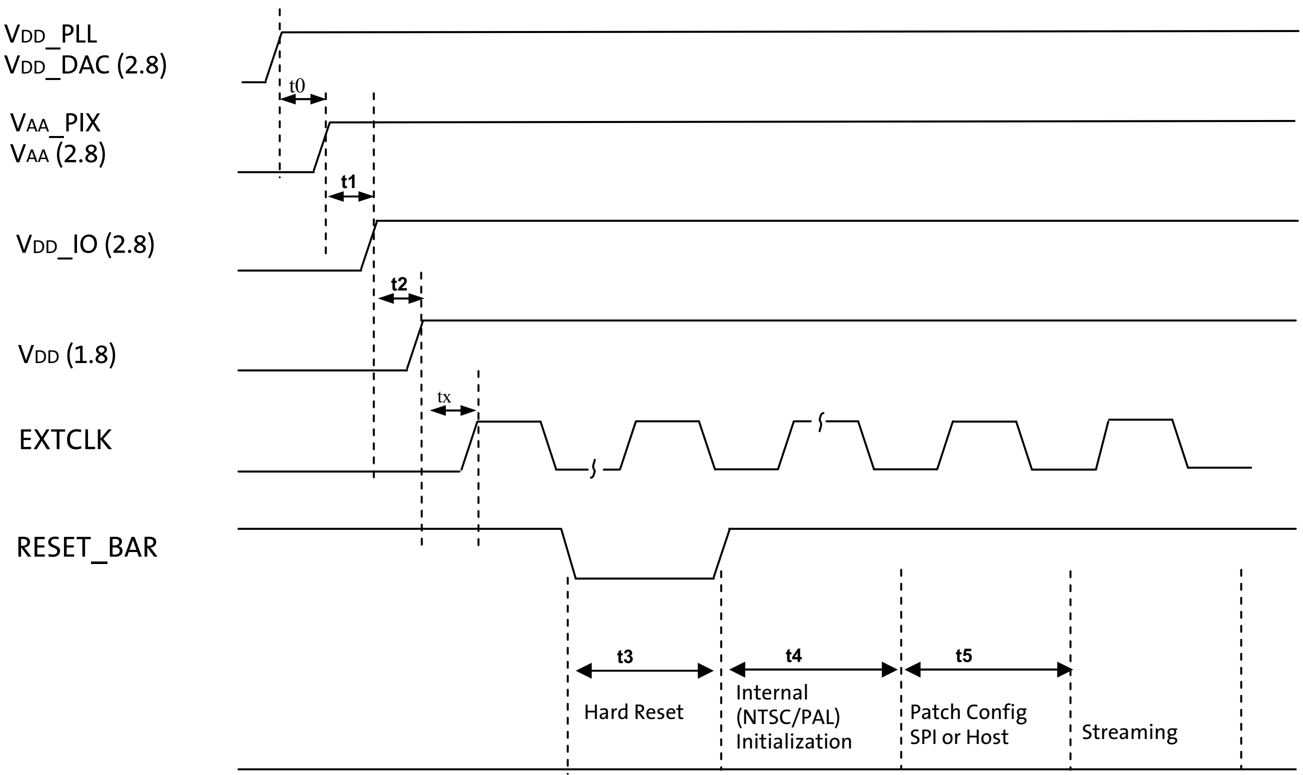
Figure 45: Power Up Sequence



Notes:
1. RESET_BAR may not exceed VDD_IO + 0.3V.
2. The 2.8V plane (VAA, VAA_PIX, VDD_PLL, VDD_DAC, VDD_IO) must remain at a higher voltage than the 1.8V core voltage at all times.

Table 35: Power Up Sequence

Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD_PLL to VAA/VAA_PIX	t0	0	–	–	µS
VAA/VAA_PIX to VDD_IO	t1	0	–	–	µS
VDD_IO to VDD	t2	0	–	–	µS
Xtal settle time	tx	–	30[1]	–	mS
Hard Reset	t3	10[2]	–	–	Clock cycle
Internal Initialization	t4	50	–	–	mS
Patch Load (SPI or I2C)	t5	–	400[3]	–	mS

Notes:
1. Xtal settling time is component-dependent (Xtal, Oscillator, and so on) and usually takes about 10mS ~100mS.
2. Hard reset time is the minimum time required after power rails are settled. Ten clock cycles are required for the sensor itself, assuming all power rails are settled. In a circuit where Hard reset is performed by the RC circuit, then the RC time must include the all power rail settle time and Xtal
3. This is required to load necessary patches using Flash mode (SPI) or Host mode (two-wire serial interface). Loading time varies depending on the number of patches and bus speed.

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Figure 46: Power Down Sequence

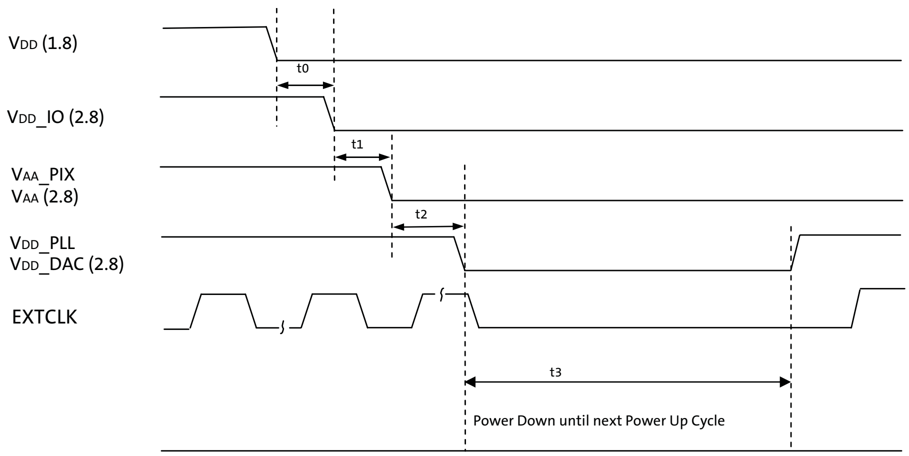

Table 36: Power Down Sequence

Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD to VDD_IO	t0	0	–	–	µS
VDD_IO to VAA/VAA_PIX	t1	0	–	–	µS
VAA/VAA_PIX to VDD_PLL/DAC	t2	0	–	–	µS
Power Down until Next Power Up Time	t3	100[1]	–	–	ms

(1) t3 is required between power down and next power up time, all decoupling caps from regulators must completely discharged before next power up.

Figure 47: FRAME_SYNC to FRAME_VALID/LINE_VALID

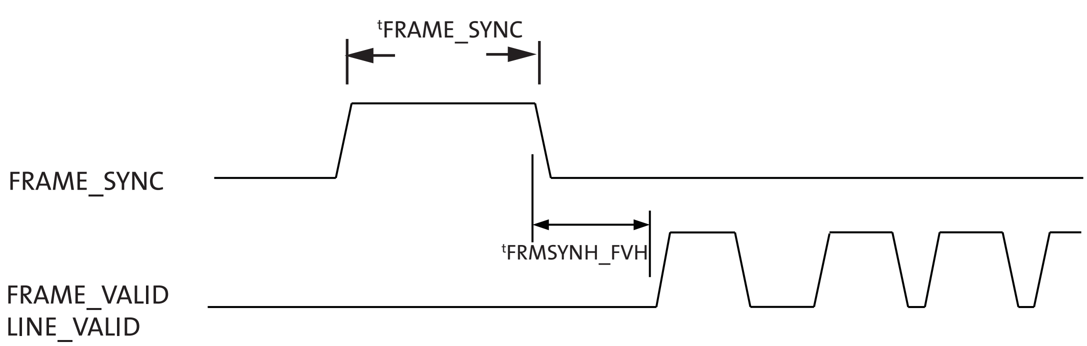

Table 37: FRAME_SYNC to FRAME_VALID/LINE_VALID Parameters

Parameter	Name	Conditions	Min	Typ	Max	Unit
FRAME_SYNC to FV/LV	tFRMSYNC_FVH	Auto Config mode	4	–	–	ms
tFRAME_SYNC	tFRAMESYNC		30			ms

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Figure 48: Reset to SPI Access Delay

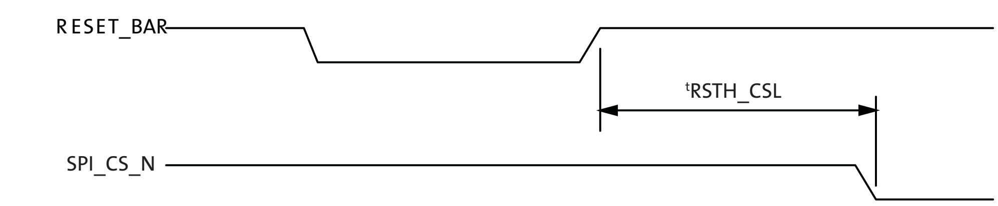

Figure 49: Reset to Serial Access Delay

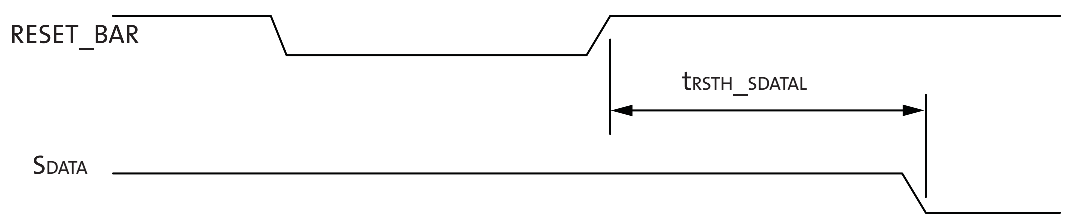

Figure 50: Reset to AE/AWB Image

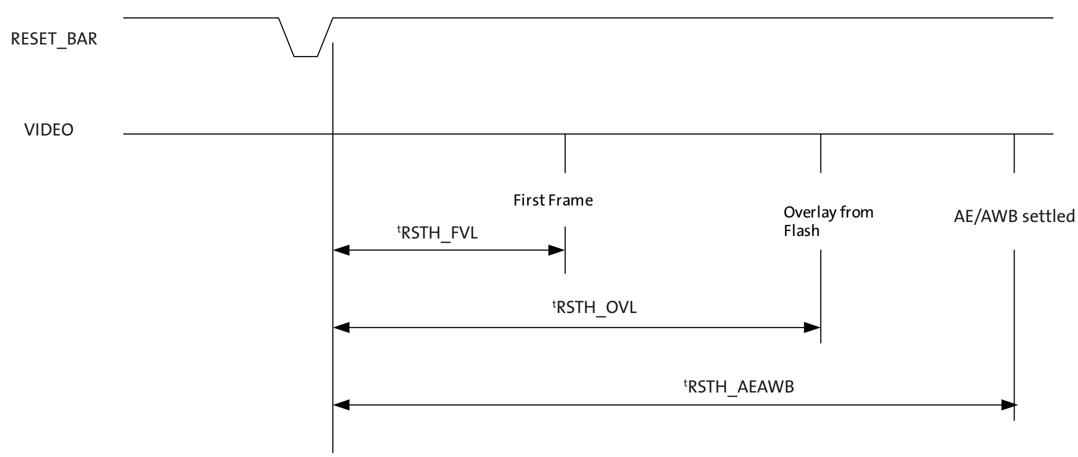

Table 38: RESET_BAR Delay Parameters

Parameter	Name	Condition	Min	Typ	Max	Unit
Power up delay 2.8V to 1.8V			0.1	–	–	ms
RESET_BAR HIGH to SPI_CS_N LOW	tRSTH_CSL		18	–	–	ms
RESET_BAR HIGH to SDATA LOW	tRSTH_SDATAL		1.8	–	–	ms
RESET_BAR HIGH to FRAME_VALID	tRSTH_FVL		235	–	–	ms
RESET_BAR HIGH to first Overlay	tRSTH_OVL		235	–	–	ms
RESET_BAR HIGH to AE/AWB settled	tRSTH_AEAWB		–	400	–	ms

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Electrical Specifications

Figure 51: SPI Output Timing

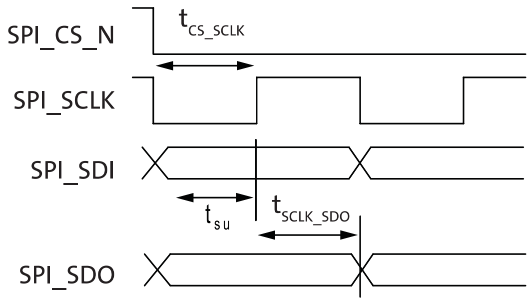

Table 39: SPI Data Setup and Hold Timing

Parameter	Description	Min	Typ	Max	Units
^{f}SPI_SCLK	SPI_SCLK Frequency	1.6875	4.5	18	MHz
^{t}su	Setup time	–	–	110	ns
^{t}SCLK_SDO	Hold time			110	ns
^{t}CS_SCLK	Delay from falling edge of SPI_CS_N to rising edge of SPI_SCLK	–	230	–	ns

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Caution **Stresses greater than those listed in Table 40 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**

Table 40: Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit
		Min	Max	
VDD	Digital power (1.8V)	-0.3	2.4	V
VDD_IO	I/O power (2.8v)	-0.3	4	V
VAA	VAA Analog power (2.8V)	-0.3	4	V
VAA_PIX	Pixel array power (2.8v)	-0.3	4	V
VDD_PLL	PLL power (2.8V)	-0.3	4	V
VDD_DAC	DAC power (2.8V)	-0.3	4	V
VIN	DC Input Voltage	-0.3	VDD_IO+0.3	V
VOUT	DC Output Voltage	-0.3	VDD_IO+0.3	V
TSTG	Storage temperature	-50	150	°C

Table 41: Electrical Characteristics and Operating Conditions

Parameter[1]	Condition	Min	Typ	Max	Unit
Core digital voltage (VDD)	–	1.7	1.8	1.9	V
IO digital voltage (VDD_IO)	–	2.66	2.8	2.94	V
Video DAC voltage (VDD_DAC)	–	2.66	2.8	2.94	V
PLL Voltage (VDD_PLL)	–	2.66	2.8	2.94	V
Analog voltage (VAA)	–	2.66	2.8	2.94	V
Pixel supply voltage (VAA_PIX)	–	2.66	2.8	2.94	V
Leakage current	EXTCLK: HIGH or LOW			10	µA
Imager operating temperature	–	–30		+70	°C
Storage temperature	–	–50		+150	°C

Notes: 1. VAA and VAA_PIX must all be at the same potential to avoid excessive current draw. Care must be taken to avoid excessive noise injection in the analog supplies if all three supplies are tied together.

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Table 42: Video DAC Electrical Characteristics–Single-Ended Mode

^{f}EXTCLK = 27 MHz; VDD = 1.8V; VDD_IO = 2.8V; VAA = 2.8V; VAA_PIX = 2.8V; VDD_PLL = 2.8V; VDD_DAC = 2.8V

Parameter	Condition	Min	Typ	Max	Unit
Resolution		–	10	-	bits
DNL		–	0.2	0.4	bits
INL		–	0.7	3.5	bits
Output local load	Output pad (DAC_POS)	–	75	-	Ω
	Unused output (DAC_NEG)	–	0	-	Ω
Output voltage	Single-ended mode, code 000h	–	.02	-	V
	Single-ended mode, code 3FFh	–	1.30	-	V
Output current	Single-ended mode, code 000h	–	0.26	-	mA
	Single-ended mode, code 3FFh	–	17.33	-	mA
Supply current	Estimate	–	-	25.0	mA
DAC_REF	DAC Reference	–	1.15 +/-0.2	-	V
R DAC_REF	DAC Reference	–	4.7	-	KΩ

Table 43: Video DAC Electrical Characteristics–Differential Mode

^{f}EXTCLK = 27 MHz; VDD = 1.8V; VDD_IO = 2.8V; VAA = 2.8V; VAA_PIX = 2.8V; VDD_PLL = 2.8V; VDD_DAC = 2.8V

Parameter	Condition	Min	Typ	Max	Unit
DNL		–	0.2	0.25	Bits
INL		–	0.8	2.5	Bits
Output local load	Differential mode per pad (DAC_POS and DAC_NEG)	–	37.5	–	Ω
Output voltage	Differential mode, code 000h, pad dacp	–	.02	–	V
	Differential mode, code 000h, pad dacn	–	1.30	–	V
	Differential mode, code 3FFh, pad dacp	–	1.30	–	V
	Differential mode, code 3FFH, pad dacn	–	.02	–	V
Output current	Differential mode, code 000h, pad dacp	–	.53	–	mA
	Differential mode, code 000h, pad dacn	–	34.7	–	mA
	Differential mode, code 3FFh, pad dacp	–	34.7	–	mA
	Differential mode, code 3FFH, pad dacn	–	.53	–	mA
Differential output, midlevel		–	0.65	–	V
Supply current	Estimate	–	–	50	mA
DAC_REF	DAC Reference	–	1.15 +/-0.2		V
R DAC_REF	DAC Reference		2.35		KΩ

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Table 44: Digital I/O Parameters
T_A = Ambient = 25°C; All supplies at 2.8V

Signal	Parameter	Definitions	Condition	Min	Typ	Max	Unit
All Outputs		Load capacitance		5	–	30	pF
		Output signal slew	2.8V, 30pF load	–	–	–	V/ns
			2.8V, 5pF load	–	–	–	V/ns
	V_{OH}	Output high voltage		–	V_{DD}_IO	–	V
	V_{OL}	Output low voltage		–0.3	–	–	V
	I_{OH}	Output high current	V_{DD} = 2.8V, V_{OH} = 2.4V	–	–	8	mA
	I_{OL}	Output low current	V_{DD} = 2.8V, V_{OL} = 0.4V	–	–	8	mA
All Inputs	V_{IH}	Input high voltage	V_{DD} = 2.8V	0.7 * V_{DD}_IO	–	V_{DD}_IO + 0.3	V
	V_{IL}	Input low voltage	V_{DD} = 2.8V	–0.3	–	0.3 * V_{DD}_IO	V
	I_{IN}	Input leakage current		–2	–	2	µA
	Signal CAP	Input signal capacitance		–	3.5	–	pF

Notes: 1. All inputs are protected and may be active when All supplies (2.8V and 1.8V) are turned off.

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Power Consumption, Operating Mode

Table 45: Power Consumption – Condition 1

fEXTCLK = 27 MHz; VDD = 1.8V; VDD _IO = 2.8V; VAA =2.8V;VAA_PIX=2.8V;
VDD _PLL = 2.8V; VDD _DAC = 2.8V

Power Plane	Supply	Condition 1	Typ Power	Max Power	Unit
VDD	1.8		55	65	mW
VDD_IO	2.8	Parallel off	5	10	mW
VAA	2.8		95	112	mW
VAA_PIX	2.8		2.5	5	mW
VDD_DAC	2.8	Single 75Ω	65	70	mW
VDD_PLL	2.8		20	25	mW
		Total	242.5	287	mW

Analog output uses single-ended mode: DAC_Pos = 75Ω, DAC_Neg = open, parallel output is disabled.

Table 46: Power Consumption – Condition 2

fEXTCLK = 27 MHz; VDD = 1.8V; VDD _IO = 2.8V; VAA =2.8V;VAA_PIX=2.8V;
VDD _PLL = 2.8V; VDD _DAC = 2.8V

Power Plane	Supply	Condition 2	Typ Power	Max Power	Unit
VDD	1.8		55	65	mW
VDD_IO	2.8	Parallel on	30	50	mW
VAA	2.8		95	112	mW
VAA_PIX	2.8		2.5	5	mW
VDD_DAC	2.8	VDAC off	2	5	mW
VDD_PLL	2.8		20	25	mW
		Total	204.5	262	mW

Analog output is disabled; parallel output is enabled.

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NTSC Signal Parameters

Table 47: NTSC Signal Parameters

f_{EXTCLK} = 27 MHz; V_{DD} = 1.8V; V_{DD_IO} = 2.8V; V_{AA} = 2.8V; V_{AA_PIX} = 2.8V; V_{DD_PLL} = 2.8V; V_{DD_DAC} = 2.8V

Parameter	Conditions	Min	Typ	Max	Units	Notes
Line Frequency		15734.25	15734.27	15734.28	Hz	
Field Frequency		59.94	59.94	59.94	Hz	
Sync Rise Time		148	148	148	ns	
Sync Fall Time		148	148	148	ns	
Sync Width		4.74	4.74	4.74	µs	
Sync Level		38	39.9	42	IRE	2, 4
Burst Level		38	39.7	42	IRE	2, 4
Sync to Setup (with pedestal off)		9.44	9.44	9.44	µs	
Sync to Burst Start		5.33	5.33	5.33	µs	
Front Porch		1.33	1.33	1.33	µs	
Black Level		6.5	7.5	8.5	IRE	1, 2, 4
White Level		90	100	110	IRE	1, 2, 3, 4

Notes:
1. Black and white levels are referenced to the blanking level.
2. NTSC convention standardized by the IRE (1 IRE = 7.14mV).
3. Encoder contrast setting R0x011 = R0x001 = 0.
4. DAC ref = 2.8kΩ, load = 37.5Ω.

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Figure 52: Video Timing

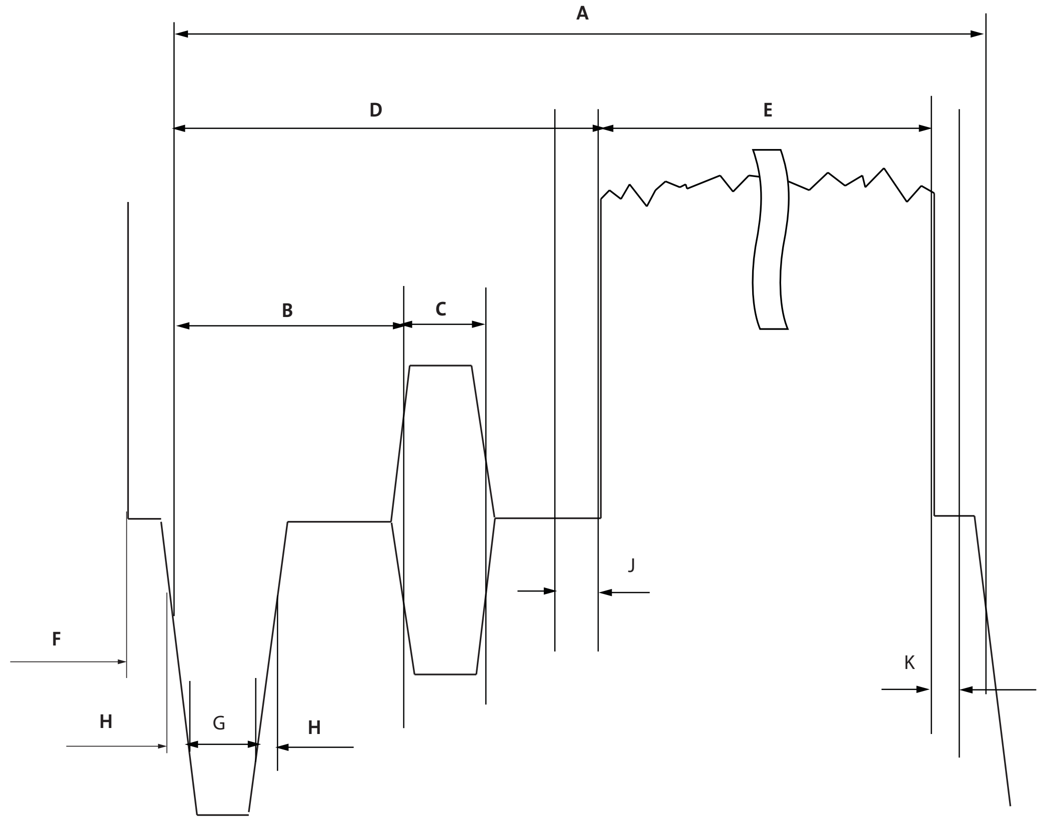

Table 48: Video Timing

	Signal	NTSC 27 MHz	PAL 27 MHz	Units
A	H Period	1716	1728	Clocks
B	Hsync to burst	144	153	Clocks
C	burst	63	66	Clocks
D	Hsync to Signal	255	279	Clocks
E	Video Signal	1423	1413	Clocks
F	Front	36	39	Clocks
G	Hsync Period	128	128	Clocks
H	Sync rising/falling edge	4	4	Clocks
J	Back overscan (BOS)	9	14	Clocks
K	Front overscan (FOS)	8	13	Clocks

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Figure 53: Equivalent Pulse

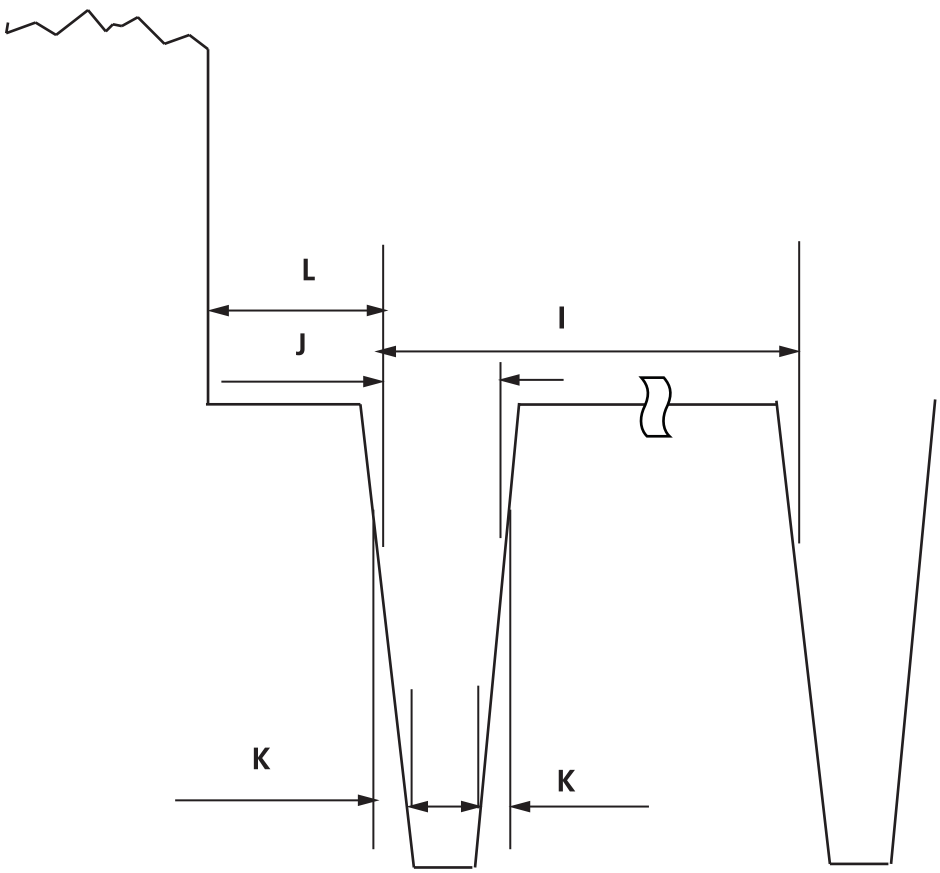

Table 49: Equivalent Pulse

	Signal	NTSC 27 MHz	PAL 27 MHz	Units
I	H/2 Period	858	864	Clocks
J	Pulse width	64	64	Clocks
K	Pulse rising/falling edge	4	4	Clocks
L	Signal to pulse	38	41	Clocks

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Figure 54: V Pulse

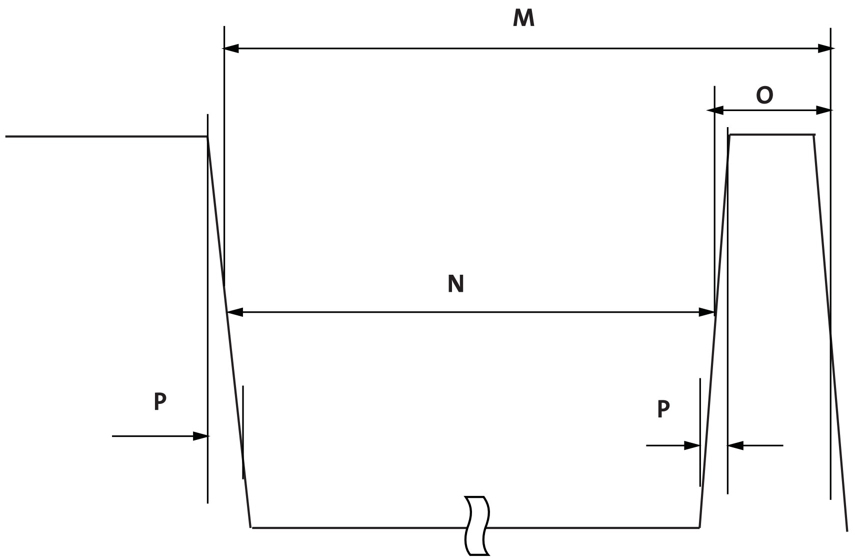

Table 50: V Pulse

	Signal	NTSC 27 MHz	PAL 27 MHz	Units
M	H/2 Period	858	864	Clocks
N	Pulse width	730	736	Clocks
O	V pulse interval	128	128	Clocks
P	Pulse rising/falling edge	4	4	Clocks

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Two-Wire Serial Bus Timing

Figure 55 and Table 51 describe the timing for the two-wire serial interface.

Figure 55: Two-Wire Serial Bus Timing Parameters

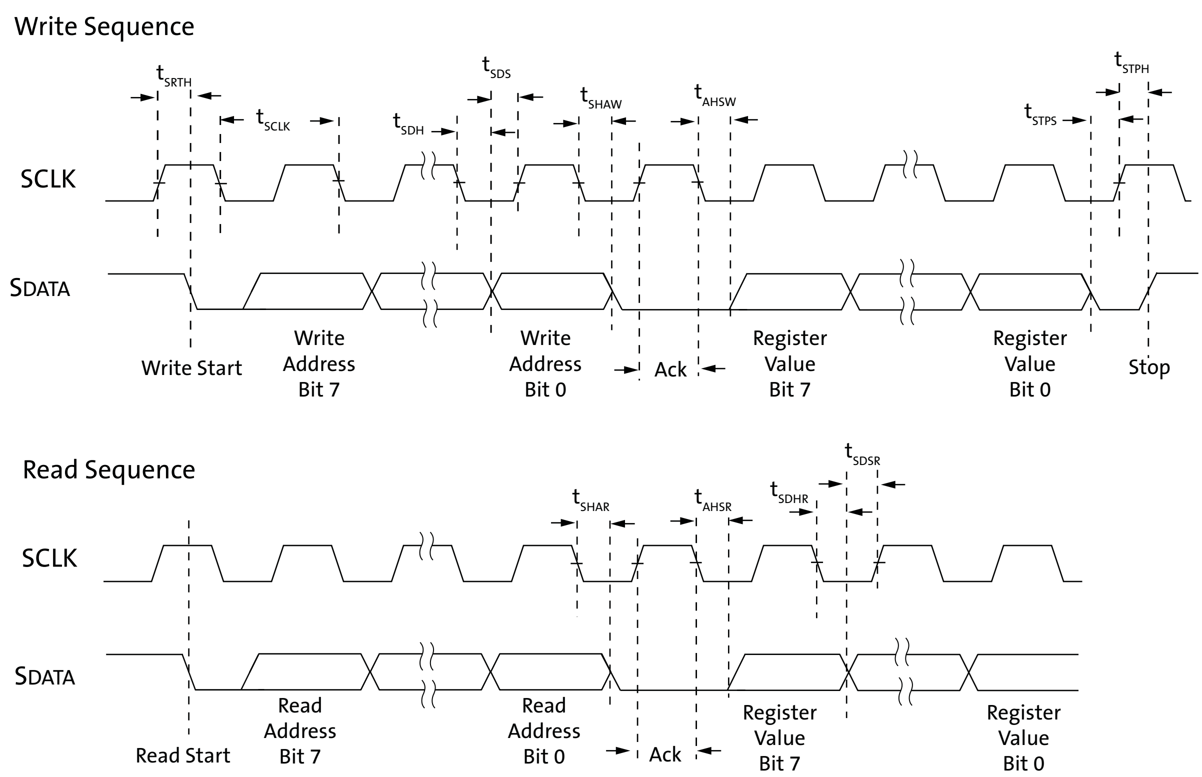

Table 51: Two-Wire Serial Bus Characteristics

f_{EXTCLK} = 27 MHz; VDD = 1.8V; VDD_IO = 2.8V; VAA = 2.8V; VAA_PIX = 2.8V; VDD_PLL = 2.8V; VDD_DAC = 2.8V; T_A = 25°C

		Standard-Mode		Fast-Mode		
Parameter	Symbol	Min	Max	Min	Max	Unit
SCLK Clock Frequency	f_{SCL}	0	100	0	400	KHz
Hold time (repeated) START condition.						
After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	-	0.6	-	µS
LOW period of the SCLK clock	t_{LOW}	4.7	-	1.3	-	µS
HIGH period of the SCLK clock	t_{HIGH}	4.0	-	0.6	-	µS
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	µS
Data hold time:	$t_{HD;DAT}$	0[4]	3.45[5]	0[6]	0.9[5]	µS
Data set-up time	$t_{SU;DAT}$	250	-	100[6]	-	nS
Rise time of both SDATA and SCLK signals	t_r	-	1000	20 + 0.1Cb[7]	300	nS
Fall time of both SDATA and SCLK signals	t_f	-	300	20 + 0.1Cb[7]	300	nS
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	µS

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Table 51: Two-Wire Serial Bus Characteristics

^{f}EXTCLK = 27 MHz; VDD = 1.8V; VDD_IO = 2.8V; VAA = 2.8V; VAA_PIX = 2.8V;
VDD_PLL = 2.8V; VDD_DAC = 2.8V; T_A = 25°C

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
Bus free time between a STOP and START condition	^{t}BUF	4.7	-	1.3	-	µS
Capacitive load for each bus line	Cb	-	400	-	400	pF
Serial interface input pin capacitance	CIN_SI	-	3.3	-	3.3	pF
SDATA max load capacitance	CLOAD_SD	-	30	-	30	pF
SDATA pull-up resistor	RSD	1.5	4.7	1.5	4.7	KΩ

Notes:
1. This table is based on I^2C standard (v2.1 January 2000). Philips Semiconductor.
2. Two-wire control is I^2C-compatible.
3. All values referred to V_{IHmin} = 0.9 VDD and V_{ILmax} = 0.1VDD levels. Sensor EXCLK = 27 MHz.
4. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
5. The maximum ^{t}HD;DAT has only to be met if the device does not stretch the LOW period (^{t}LOW) of the SCLK signal.
6. A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, but the requirement ^{t}SU;DAT 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line ^{t}r max + ^{t}SU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCLK line is released.
7. Cb = total capacitance of one bus line in pF.

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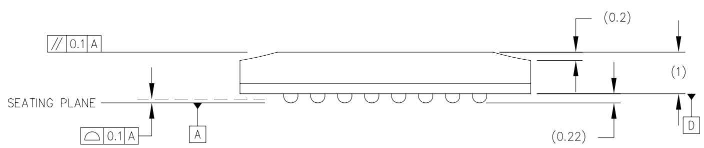
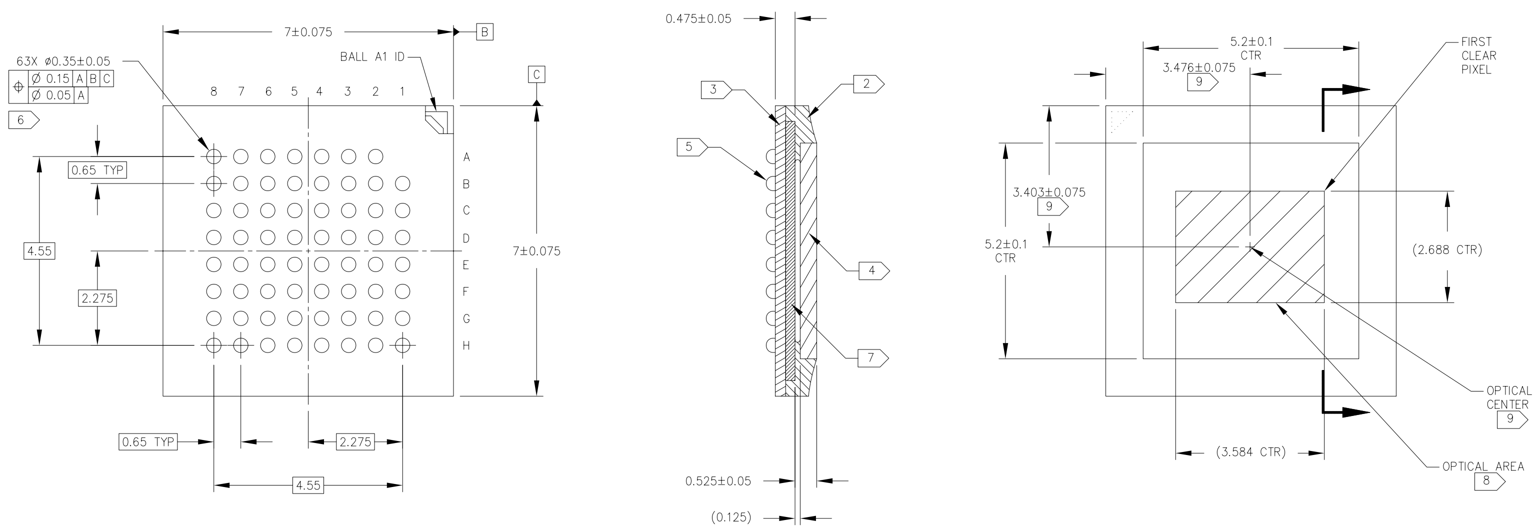
Package and Die Dimensions

Figure 56: 63-Ball cBGA Package Outline Drawing



	NOTES
1	DIMENSIONS IN MM. DIMENSIONS IN ( ) ARE FOR REFERENCE ONLY. DO NOT MEASURE PRINTED DRAWING.
2	ENCAPSULANT: EPOXY.
3	SUBSTRATE MATERIAL: PLASTIC LAMINATE 0.25 THICKNESS.
4	LID MATERIAL: BOROSILICATE GLASS 0.4 THICKNESS REFRACTIVE INDEX AT 20°C = 1.5255 @ 546nm & 1.5231 @ 588nm.
5	SOLDER BALL MATERIAL: SAC305.
6	DIMENSIONS APPLY TO SOLDER BALLS POST REFLOW. PRE-REFLOW BALL IS ø0.33 ON A ø0.27 SMD PAD.
7	IMAGE SENSOR DIE 0.2 THICKNESS.
8	MAXIMUM ROTATION OF OPTICAL AREA RELATIVE TO PACKAGE EDGES: 1°. MAXIMUM TILT OF OPTICAL AREA RELATIVE TO D : 25 MICRONS. MAXIMUM TILT OF OPTICAL AREA RELATIVE TO TOP OF COVER GLASS: 50 MICRONS.
9	DIE CENTER = PACKAGE CENTER. OPTICAL CENTER OFFSET FROM PACKAGE CENTER: X=-0.023555, Y=0.09696



PDF: 1719814179/Source: 8304342517Source:8304342517
-ASX340/MT9V139_DS Rev. B Pub. 3/11 EN

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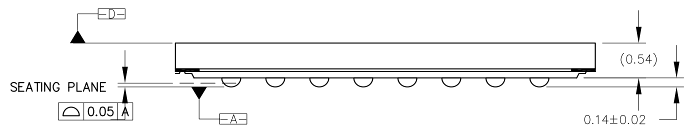
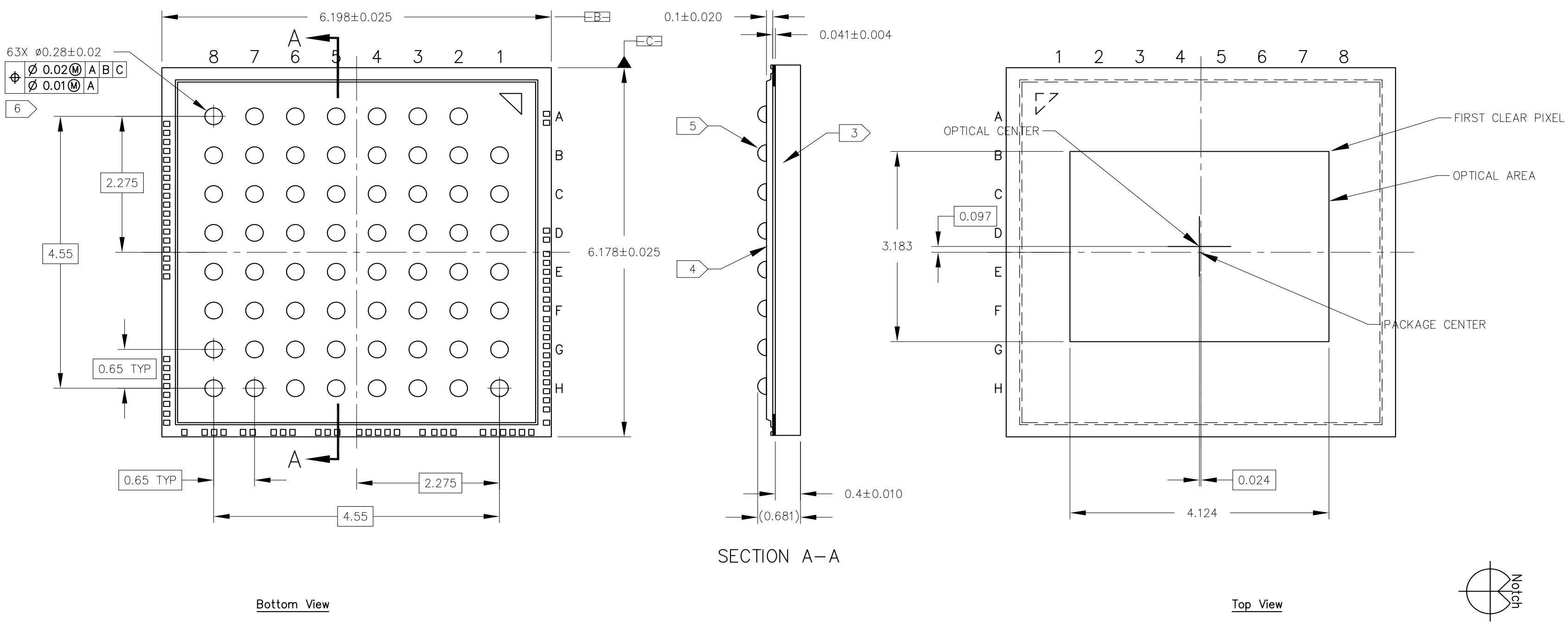
Figure 57: 63-Ball CSP Package Outline Drawing

NOTES	
1	DIMENSIONS IN MM. DIMENSIONS IN ( ) ARE FOR REFERENCE ONLY. DO NOT MEASURE PRINTED DRAWING.
2	ALL CONSTRUCTION MATERIAL COMPONENTS ARE ROHS COMPLIANT.
3	LENS MATERIALS: BOROSILICATE GLASS
4	IMAGE SENSOR DIE
5	SOLDER BALL MATERIAL: SAC305 (96.5% SN, 3% AG, 0.5% CU)
6	DIMENSIONS APPLY TO SOLDER BALLS POST REFLOW ON ⌀0.31 SMD BALL PADS.





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Revision History

Rev. C 3/14/11

- Changed Part number to ASX340
- Updated "Features" on page 1
- Updated Table 1, "Key Parameters," on page 1
- Updated Table 3, "Available Part Numbers," on page 3
- Updated "New Features" on page 3
- Updated Table 4, "Pin Descriptions," on page 12
- Updated Table 5, "Pin Assignments," on page 14
- Updated "Device Configuration" on page 31
- Updated Figure 19: "Power-Up Sequence – Configuration Options Flow Chart," on page 32
- Added Figure 56: "63-Ball cBGA Package Outline Drawing," on page 76

Rev. B 10/11/10

- Remove note from Table 2, "Key Parameters (continued)," on page 2
- Updated Table 4, "Pin Descriptions," on page 12
- Updated Table 35, "Power Up Sequence," on page 62 and Table 36, "Power Down Sequence," on page 63
- Updated Table 45, "Power Consumption – Condition 1," on page 69, Table 46, "Power Consumption – Condition 2," on page 69 on, and Table 47, "NTSC Signal Parameters," on page 70
- Changed 15–33 pF to 15-22 pF in"Crystal Usage" on page 11
- UpdatedTable 20, "Interface Structure," on page 34
- UpdatedTable 38, "RESET_BAR Delay Parameters," on page 64
- UpdatedTable 41, "Electrical Characteristics and Operating Conditions," on page 66

Rev. A 10/6/10

- Initial release

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Preliminary: This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.

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